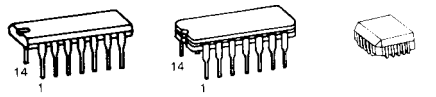
o41938

PRELIMINARY DATA

DUAL J-K FLIP FLOP WITH CLEAR

DESCRIPTION

The M54/74HC73 is a high speed CMOS DUAL J-K FLIP FLOP WITH CLEAR fabricated in silicon gate C²MOS technology. It has the same high speed performance of LSTTL combined with true CMOS low power consumption. In accordance with the logic level applied to J and K inputs, this device changes state on the negative going transition of clock input pulse ($\overline{CK}$). The clear function is accomplished independently of the clock condition when the clear input ($\overline{CLR}$) is taken low. All inputs are equipped with protection circuits against static discharge or transient excess voltage.



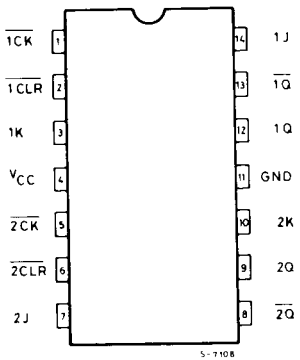
B1 Plastic Package | **F1** Ceramic Package | **C1** Chip Carrier

ORDERING NUMBERS: M54HC73 F1
M74HC73 B1
M74HC73 F1
M74HC73 C1

FEATURES

- High Speed
  f_{MAX} = 70 MHz (Typ.) at V_{CC} = 5V
- Low Power Dissipation
  I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity
  $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Capability
  10 LSTTL Loads
- Symmetrical Output Impedance
  $|I_{OH}| = I_{OL}$ = 4 mA (Min.)
- Balanced Propagation Delays
  $t_{PLH} = t_{PHL}$
- Wide Operating Voltage Range
  V_{CC} (opr) = 2V to 6V
- Pin and Function compatible with 54/74LS73

PIN CONNECTIONS
(top view)



Dual in line

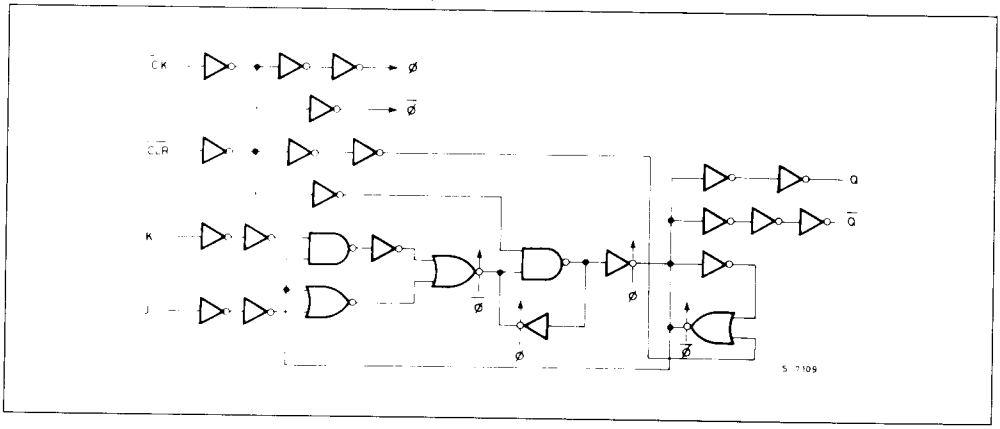
FOR CHIP CARRIER INFORMATION CONTACT SGS

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{CLR}$	J	K	$\overline{CK}$	Q	$\overline{Q}$	
L	X	X	X	L	H	CLEAR
H	L	L	↓	Qn	$\overline{Qn}$	NO CHANGE
H	L	H	↓	L	H	—
H	H	L	↓	H	L	—
H	H	H	↓	$\overline{Qn}$	Qn	TOGGLE
H	X	X	↑	Qn	$\overline{Qn}$	NO CHANGE

X: Don't care

LOGIC DIAGRAM (1/2 of device show)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	−0.5 to 7	V
V_I	DC Input Voltage	−0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Source Sink Current Per Output Pin	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	500 (*)	mW
T_{stg}	Storage Temperature	−65 to 150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≅ 65°C derate to 300 mW by 10 mW/°C: 65°C to 85°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limit		Unit
V_{CC}	Supply Voltage		2 to 6		V
V_I	Input Voltage		0 to V_{CC}		V
V_O	Output Voltage		0 to V_{CC}		V
T_A	Operating Temperature	74HC Series 54HC Series	− 40 to 85 −55 to 125		°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2 V V_{CC} = 4.5V V_{CC} = 6 V	0 to 1000 0 to 500 0 to 400		ns

DC SPECIFICATIONS

Symbol	Parameter	V_{CC}	Test Condition		T_A = 25°C 54HC and 74HC			-40 to 85°C 74HC		-55 to 125°C 54HC		Unit
					Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0			1.5	—	—	1.5	—	1.5	—	V
		4.5			3.15	—	—	3.15	—	3.15	—	
		6.0			4.2	—	—	4.2	—	4.2	—	
V_{IL}	Low Level Input Voltage	2.0			—	—	0.5	—	0.5	—	0.5	V
		4.5			—	—	1.35	—	1.35	—	1.35	
		6.0			—	—	1.8	—	1.8	—	1.8	
V_{OH}	High Level Output Voltage	2.0	V_I	I_O	1.9	2.0	—	1.9	—	1.9	—	V
		4.5	V_{IH}	−20 μA	4.4	4.5	—	4.4	—	4.4	—	
		6.0	or		5.9	6.0	—	5.9	—	5.9	—	
		4.5	V_{IL}	−4.0 mA	4.18	4.31	—	4.13	—	4.10	—	
		6.0		−5.2 mA	5.68	5.8	—	5.63	—	5.60	—	
V_{OL}	Low Level Output Voltage	2.0			—	0	0.1	—	0.1	—	0.1	V
		4.5	V_{IH}	20 μA	—	0	0.1	—	0.1	—	0.1	
		6.0	or		—	0	0.1	—	0.1	—	0.1	
		4.5	V_{IL}	4.0 mA	—	0.17	0.26	—	0.33	—	0.40	
		6.0		5.2 mA	—	0.18	0.26	—	0.33	—	0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND		—	—	±0.1	—	±1		±1	μA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND		—	—	2	—	20		40	μA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C, C_L = 15pF, Input $t_r = t_f$ = 6ns)

Symbol	Parameter	54HC and 74HC			Unit
		MIN.	TYP.	MAX.	
t_{TLH} t_{THL}	Output Transition Time		4	8	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)		17	27	ns
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)		21	33	ns
f_{MAX}	Maximum Clock Frequency	35	71		MHz
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width ($\overline{CK}$)		8	15	ns
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)		8	15	ns
t_s	Minimum Set-up Time		10	20	ns
t_h	Minimum Hold Time		—	0	ns
t_{REM}	Minimum Removal Time ($\overline{CLR}$)		1	10	ns

AC ELECTRICAL CHARACTERISTICS ($C_L = 50pF$, Input $t_r = t_f = 6ns$)

Symbol	Parameter	V_{CC}	Test Condition	T_A = 25°C 54HC and 74HC			−40 to 85°C 74HC		−55 to 125°C 54HC		Unit
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_{PLH} t_{PHL}	Propagation Delay Time ($\overline{CK}$ - Q, $\overline{Q}$)	2.0		—	75	160	—	195			ns
		4.5		—	20	32	—	39			
		6.0		—	17	28	—	34			
t_{PLH} t_{PHL}	Progation Delay Time ($\overline{CLR}$ - Q, $\overline{Q}$)	2.0		—	95	195	—	235			ns
		4.5		—	25	39	—	47			
		6.0		—	22	34	—	40			
f_{MAX}	Maximum Clock Frequency	2.0		6	15	—	5	—			ns
		4.5		30	65	—	25	—			
		6.0		35	80	—	29	—			
$t_{W(L)}$ $t_{W(H)}$	Minimum Pulse Width ($\overline{CK}$)	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
$t_{W(L)}$	Minimum Pulse Width ($\overline{CLR}$)	2.0		—	30	75	—	90			ns
		4.5		—	8	15	—	18			
		6.0		—	7	13	—	16			
t_s	Minimum Set-up Time	2.0		—	45	100	—	120			ns
		4.5		—	10	20	—	24			
		6.0		—	9	17	—	21			
t_h	Minimum Hold Time	2.0		—	—	0	—	0			ns
		4.5		—	—	0	—	0			
		6.0		—	—	0	—	0			
t_{REM}	Minimum Removal Time ($\overline{CLR}$)	2.0		—	5	50	—	60			ns
		4.5		—	1	10	—	12			
		6.0		—	1	9	—	11			
C_{IN}	Input Capacitance			—	5	10	—	10			pF
C_{PD} (*)	Power Dissipation Capacitance			—	42	—	—	—			pF

Note (*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the following equation.
$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2$ (per FF)