Siliconix
incorporated

Si7541
CMOS 12-Bit Multiplying DAC

FEATURES

- 12-Bit Linearity (INL < 1/2 LSB)
- Four Quadrant Multiplication
- Fast Settling (600 ns)
- Monotonic (DNL < 1/2 LSB)
- TTL/CMOS Compatible

BENEFITS

- Improves System Absolute Accuracy
- Allows Bipolar Reference Inputs
- Increases Data Throughput
- Closed-Loop Servo Stability
- Simplifies Logic Interfacing

APPLICATIONS

- ATE Systems
- Digitally Controlled Gain/Attenuation
- Function Generators
- Closed-Loop Servo Systems
- Hybrid/Custom A/D Converters

DESCRIPTION

The Si7541 is a 12-Bit multiplying digital-to-analog converter which features true 12-bit integral linearity and monotonicity, fast settling time (600 ns), TTL-compatible logic inputs, and low gain drift of 5 ppm/°C (max). The 1/2 LSB differential nonlinearity specification guarantees monotonicity, thus eliminating instability in closed-loop systems.

Multiplying applications for the Si7541 include digitally controlled amplifiers, attenuators, filters and power supplies. The fast settling time makes the Si7541 ideal for high speed data conversion and hybrid or custom A/D converters.

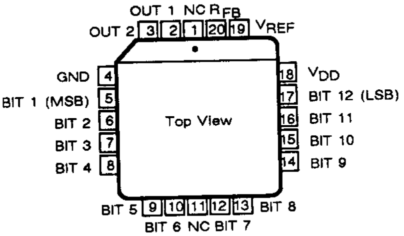
The Si7541 is built using the Siliconix advanced 5-micron CMOS process known as PolyMOS™, allowing fast settling time and low glitch impulse. Highly-stable thin film resistors are included on the chip for low drift over temperature and time. These are laser-trimmed to achieve 1/2 LSB integral nonlinearity (INL) and reduced gain error. An epitaxial layer prevents latch up.

The Si7541 is available in 18-pin PDIP, CerDIP and side braze DIP packages for commercial, J, K suffix (0 to 70°C), industrial, A, B suffix (-40 to 85°C) and military, S, T suffix (-55 to 125°C) operation, respectively. For surface mount applications, the Si7541 is available in the PLCC-20 (0 to 70°C) and the hermetic LCC-20 (-55 to 125°C). Each package and temperature range is available in two linearity grades.

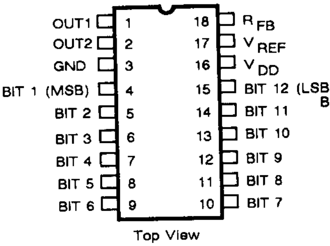
For more information on the Si7541, please refer to Siliconix Application Note AN87-3.

PIN CONFIGURATION & ORDERING INFORMATION

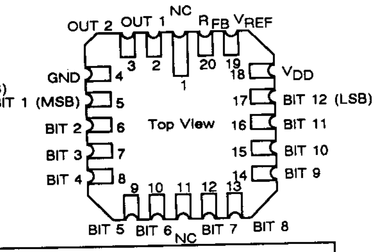
PLCC Package



Dual-In-Line Package

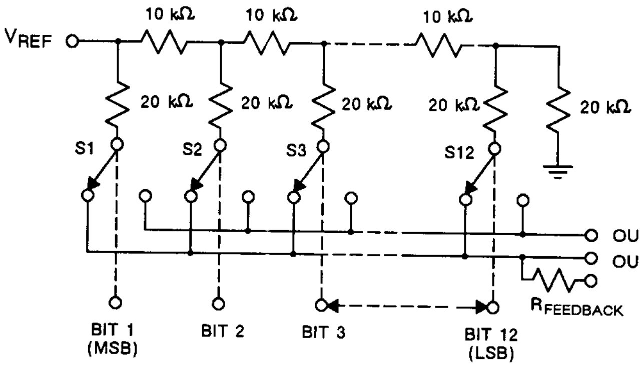


LCC Package



INL Tmin - Tmax (LSB)	GAIN ERROR Ta = 25° C (LSB)	TEMPERATURE RANGE AND PACKAGE				
		PLCC 0 to 70°C	PDIP 0 to 70°C	CerDIP -40 to 85°C	SIDE BRAZE -55 to 125°C	LCC -55 to 125°C
± 1	± 12.5	SI7541JP	SI7541JN	SI7541AQ	SI7541SD	SI7541SE
± 1/2	± 12.5	SI7541KP	SI7541KN	SI7541BQ	SI7541TD	SI7541TE

FUNCTION BLOCK DIAGRAM



DEFINITION OF TERMS

GAIN ERROR

Gain error or full-scale error is a measure of the difference between an ideal DAC's and the actual device output. For the Si7541, ideal full-scale output is $-(4095/4096) \cdot (V_{REF})$. Gain error is adjustable to zero using external trims as shown in Figures 5 and 6.

OUTPUT LEAKAGE CURRENT

This is the current that appears at OUT1 with the DAC loaded to all 0s or at OUT2 with the DAC loaded to all 1s.

MULTIPLYING FEEDTHROUGH ERROR

This is the AC error due to capacitive feedthrough from V_{REF} to OUT1 with DAC loaded to all 0's.

OUTPUT CURRENT SETTLING TIME

This is the time required for the output current of the DAC to settle to within 1/2 LSB into 100 Ω, and is specified for a zero to full scale digital input change.

PROPAGATION DELAY

This is a measure of the internal circuit delay from the time a digital input changes to the point when the analog output at OUT1 reaches 90% of its final value.

DIGITAL TO ANALOG GLITCH IMPULSE

This is a measure of the area of the impulse injected to the analog outputs when the digital inputs change state. It is usually specified as the area of the impulse in nV-secs. It is measured with V_{REF} = GND and an LH0032 as the output op amp, and phase compensation capacitor = 0 pF.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	17 V
V_{REF} to GND	25 V
V_{RFB} to GND	25 V
Digital Input Voltage to GND	−0.3 V to V_{DD}
V_{OUT1}, V_{OUT2} to GND	−0.3 V to V_{DD}
Storage Temperature (D, Q, E Suffix)	−65 to 150°C
(N, P Suffix)	−65 to 125°C
Operating Temperature (S, T Suffix)	−55 to 125°C
(A, B Suffix)	−40 to 85°C
(J, K Suffix)	0 to 70°C
Power Dissipation (Package)*	
N, P Suffixes **	470 mW
D, E, Q Suffixes ***	900 mW

* All leads welded or soldered to PC board.

** Derate 6.5 mW/°C above 25°C

*** Derate 12 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS[a]

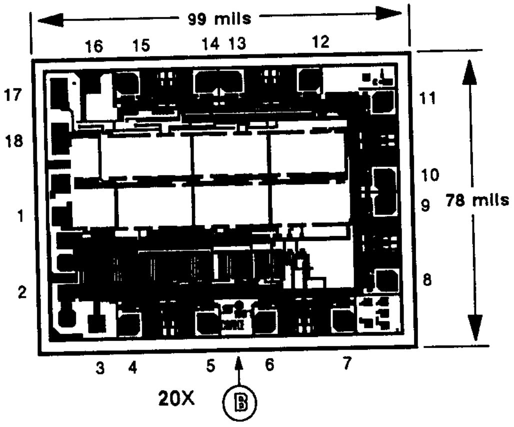
PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{DD} = +15 V, V_{REF} = +10 V V_{OUT1} = V_{OUT2} = 0V Output Amplifier: OP-07	LIMITS						UNIT
			1=25°C 2=125,85,70°C 3=-55,-40,0°C		B, K, T GRADE		A, J, S GRADE		
			TEMP	TYP[d]	MIN[b]	MAX[b]	MIN[b]	MAX[b]	
ACCURACY									
Resolution	N		1,2,3		12		12		LSB
Relative Accuracy (Integral Non-Linearity)	INL	(1LSB = 0.024% of Full Scale)	1,2,3		-1/2	1/2	-1	1	
Differential Nonlinearity	DNL		1,2,3		-1/2	1/2	-1	1	
Gain Error	G_{FSE}	Measured Using Internal R_{FB}	1 2,3		-12.5 -16.7	12.5 16.7	-12.5 -16.7	12.5 16.7	
Gain Temp Coefficient[c]	TCG_{FS}	Δ Gain / Δ Temperature	1,2,3	2	-5	5	-5	5	ppm/ °C
Output Leakage Current	I_{OUT1}	V_{REF} = ±10 V, All Digital Inputs = 0 V	1		-5	5	-5	5	nA
			2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200	
	I_{OUT2}	V_{REF} = ±10 V, All Digital Inputs = V_{DD}	1		-5	5	-5	5	
			2,3		B: -10 K: -10 T: -200	10 10 200	A: -10 J: -10 S: -200	10 10 200	
REFERENCE									
Reference Input Resistance (Pin 17 to GND)	R_{REF}		1,2,3	10	7	18	7	18	kΩ
INPUT									
Input HIGH Voltage	V_{IH}		1,2,3		2.4		2.4		V
Input LOW Voltage	V_{IL}		1,2,3			0.8		0.8	
Input Current	I_{IN}		1,2,3		-1	1	-1	1	µA
Input Capacitance[c]	C_{IN}	V_{IN} = 0 V				8		8	pF
SUPPLY									
Power Supply Rejection	PSRR	Δ Gain / Δ V_{DD}, Δ V_{DD} = ±5%	1 2,3		-0.01 -0.02	0.01 0.02	-0.01 -0.02	0.01 0.02	%per%
V_{DD} Range[e]			1,2,3		5	16	5	16	V

ELECTRICAL CHARACTERISTICS [a]

PARAMETER	SYMBOL	Test Conditions Unless Otherwise Specified: V_{DD} = +15 V, V_{REF} = +10 V V_{OUT1} = V_{OUT2} = 0V Output Amplifier: OP-07	LIMITS 1=25°C 2=125,85,70°C 3=-55,-40,0°C		LIMITS B, K, T GRADE		LIMITS A, J, S GRADE		UNIT
			TEMP	TYP [d]	MIN [b]	MAX [b]	MIN [b]	MAX [b]	
SUPPLY (Cont'd)									
Supply Current	I_{DD}	All Digital Inputs V_{IL} or V_{IH}	1,2,3			2		2	mA
		All Digital Inputs 0 V or V_{DD}	1 2,3			100 500		100 500	µA
DYNAMIC									
Propagation Delay	t_{PD}	From 50% of Digital Input to 90% of Final Analog Output OUT1 load = 100Ω, C_{EXT} = 13 pF Digital Inputs = 0 V to V_{DD} or V_{DD} to 0V	1	100					ns
Digital-to-Analog Glitch Impulse	I_S	Output Amplifier: LH0032 V_{REF} = 0 V, C_F = 0 pF Digital Inputs = 0 V to V_{DD} or V_{DD} to 0V	1	1000					nV-s
Multiplying Feedthrough Error (V_{REF} to OUT1)	MF_{ER}	V_{REF} = 20 V_{p-p}, Sinewave @ 10 kHz	1	1					mV p-p
Output Current Settling Time	t_S	To 0.01% of Full Scale Range OUT1 load = 100Ω, C_{EXT} = 13 pF Digital Inputs = 0 V to V_{DD} or V_{DD} to 0V	1	0.6					µs
Output Capacitance [c]	C_{OUT1}	Digital Inputs = V_{IH} V_{IL}	1,2,3			200 70		200 70	pF
	C_{OUT2}					70 200		70 200	

NOTES:
a. Refer to PROCESS OPTION FLOWCHART for additional information.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Guaranteed by design, not subject to production test.
d. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
e. Accuracy is not guaranteed over this range.

DIE TOPOGRAPHY



Pad No.	Function
1	Out 1
2	Out 2
3	GND
4	Bit 1 (MSB)
5	Bit 2
6	Bit 3
7	Bit 4
8	Bit 5
9	Bit 6
10	Bit 7
11	Bit 8
12	Bit 9
13	Bit 10
14	Bit 11
15	Bit 12 (LSB)
16	V_{DD}(substrate)
17	V_{REF}
18	R_{FB}

CSAK-IB

48 PMOS Transistors
68 NMOS Transistors
12 NPN Transistors
7 Polysilicon Resistors
12 400 N+ Resistors
10 10 kΩ Thin Film Resistors
13 20 kΩ Thin Film Resistors

CAUTION

ESD (Electro-Static-Discharge-Sensitive) device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DETAILED DESCRIPTION

The Si7541 is a 12-bit multiplying Digital-to-Analog Converter consisting of a highly stable thin film R-2R ladder network and twelve single-pole double-throw current steering NMOS analog switches on a monolithic chip. The binarily weighted CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most applications.

The binary weighted currents are switched between the OUT1 and OUT2 bus lines, thus maintaining a constant current in each leg of the ladder regardless of switch states.

The input resistance at V_{REF} (Figure 1) is always equal to the value "R_{REF}" and is the R-2R ladder characteristic resistance. Since R_{REF} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, be it positive, negative or AC. If a current source is used, a low TC external feedback resistor RFB is recommended to define the scale factor.

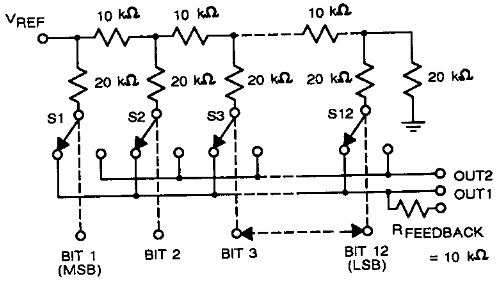


Figure 1. Si7541 Functional Diagram (All Inputs HIGH)

DETAILED DESCRIPTION

Figure 2 illustrates the typical NMOS SPDT switch with its associated CMOS level shifter/driver.

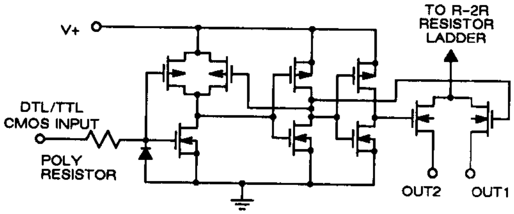


Figure 2. Simplified Schematic Single SPDT Switch

EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows the equivalent circuit for all digital inputs LOW. All reference current is switched to OUT2. The current sources $I_{LEAKAGE}$ are composed of surface and junction leakages to the substrate. The 1/4096 current source represents the constant 1 LSB current drain through the ladder termination resistor. The output capacitance on OUT2 (with all its switches ON) is 200 pF, whereas on OUT1 it is only 70 pF.

The output capacitances are dependent upon the digital input code and vary between the LOW and HIGH values.

Analysis of the circuit for all digital inputs HIGH, as shown in Figure 4 is similar to Figure 3; however the "ON" switches are now on OUT1, hence the 200 pF at that terminal.

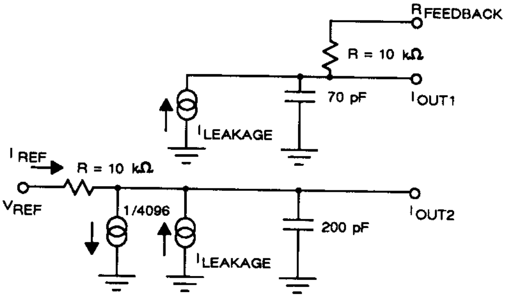


Figure 3. Si7541 Equivalent Circuit (All Inputs LOW)

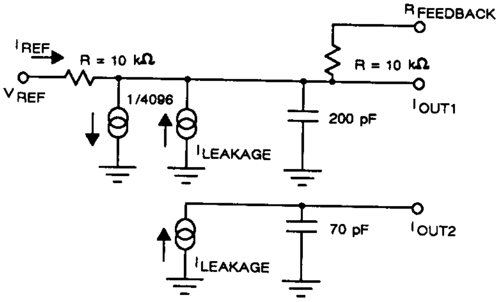


Figure 4. Si7541 Equivalent Circuit (All Inputs HIGH)

APPLICATIONS

APPLICATIONS HINTS

Static linearity of the Si7541 depends upon the potential of OUT1 and OUT2 (pins 1 and 2) being exactly equal to GND (pin 3). In most applications the DAC is connected to an external output op amp with its non-inverting input tied to ground, which converts its current output into a voltage output signal. The op amp selected should have a low input bias current (typically less than 75 nA) and low drift over the operating temperature range. The amplifier's input offset voltage should be nulled to less than 10% of 1 LSB (typically less than ±200 μV). The non-inverting input should be connected directly to GND without the usual input bias current compensation resistor. This resistor can cause variable offsets which would create

APPLICATIONS (Cont'd)

errors. Ground loops should be avoided by taking all pins going to GND to a common point.

The V_{DD} power supply should have a low noise level and not have transients greater than +17 V.

Unused digital inputs must be grounded or taken to V_{DD}. It is also recommended that all digital inputs be taken to ground via a high value (1 MΩ) resistor to prevent the accumulation of static charges whenever the PC board is not connected to the system.

OUTPUT OFFSET: CMOS DACs exhibit a code dependent output resistance which can cause a code dependent error voltage at the output of the amplifier. The maximum value of this error is $0.67 V_{OS}$, where V_{OS} is the amplifier input offset voltage.

To maintain monotonicity it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the operating temperature range. It is also important that V_{OS} be nulled, either by using the op amp's nulling pins or an external network.

DIGITAL GLITCHES: One cause of glitches is capacitive coupling from the digital lines to the OUT1 and OUT2 terminals. This can be minimized by guarding the analog pins of the Si7541 (pins 1, 2, 17, 18) from the digital input pins by a ground track run between pins 2 and 3 and between pins 16 and 17. Note that the analog pins are at one end of the package separated from the digital inputs by V_{DD} and GND to aid guarding.

TEMPERATURE COEFFICIENTS: The Gain temperature coefficient of the Si7541 has a maximum value of 5 ppm/°C and a typical of 2 ppm/°C. This corresponds to worst case gain shifts of 2 LSBs and 0.8 LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are required to adjust full scale range, low temperature coefficient (approximately 50 ppm/°C) resistors or trim-pots should be selected.

OUTPUT AMPLIFIER: For low speed applications the AC specifications of the op amp are not critical. In high-speed applications, however, slew rate, settling time, open-loop gain, gain/phase margin specifications of the amplifier should be selected for the desired performance. As mentioned before, the usual bias current compensation resistor at the inverting input of the op amp should not be used. Instead, the amplifier should have a low input bias current over the operating temperature range.

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 5 shows the circuit configuration required for unipolar binary (2-quadrant multiplication) operation. With a DC voltage or current-reference (positive or negative) applied at pin 17, the circuit is a unipolar Digital-to-Analog converter. With an AC reference this circuit provides 2-quadrant multiplication (digitally controlled attenuation). The reference input voltage can range between −20 V and +20 V due to the ability of V_{REF} to exceed V_{DD}.

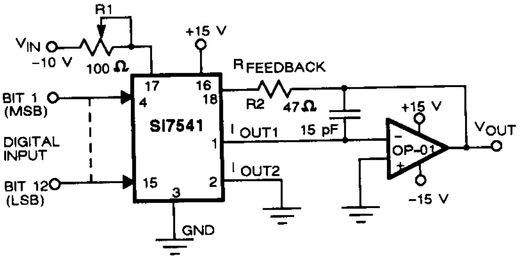


Figure 5. Unipolar Binary Operation (2 - Quadrant)

Table 1 shows the digital code input analog voltage correspondence. R1 provides full-scale trimming (load the DAC with 1111 1111 1111 , adjust R1 for $V_{OUT} = -V_{REF}(4095/4096)$. Full-scale can also be adjusted by omitting R1 and R2 and trimming the magnitude of V_{REF}.

TABLE 1

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT})
1111 1111 1111	$-(4095/4096)\ V_{IN}$
1000 0000 0000	$-(2048/4096)\ V_{IN}$
0000 0000 0001	$-(1/4096)\ V_{IN}$
0000 0000 0000	0 V

Unipolar Binary Code Table for Circuit of Figure 5

BIPOLAR BINARY OPERATION (4-QUADRANT MULTIPLICATION)

Figure 6 illustrates the recommended circuit for bipolar operation. With a DC reference of either polarity the circuit provides offset binary operation. With an AC reference, the eleven LSBs provide digitally controlled attenuation of the reference input while the MSB provides polarity control.

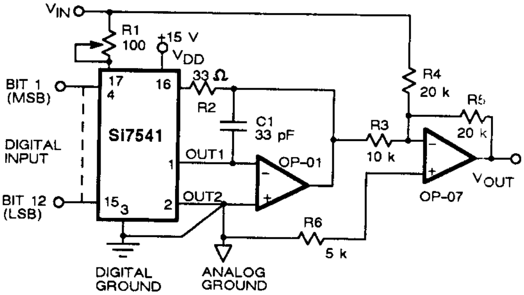


Figure 6. Bipolar Operation (4 - Quadrant Multiplication)

With the DAC loaded to 1000 0000 0000, adjust R1 for V_{OUT} = 0 V (alternatively, R1 and R2 can be omitted and the ratio of R3 to R4 can be adjusted for V_{OUT} = 0 V). Full-scale trimming can be performed by adjusting V_{REF} or by adjusting the value of R5.

As in unipolar operation the amplifiers must be chosen for low input offset voltage and low input bias current. The input offset voltage of both amplifiers should be adjusted to less than 0.1 mV and be better than 0.5 mV over the operating temperature range of interest. R3, R4 and R5 must be matched. Mismatches of R5 to R4 and (2 X R3) cause full-scale error. Mismatch of (2 X R3) to R4 causes both offset and full-scale errors.

Table 2 illustrates the relationship between the offset binary digital codes and the analog output voltage.

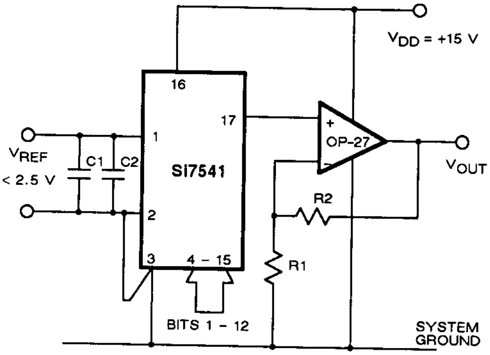
TABLE 2

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT})
1111 1111 1111	+(2047/2048) V_{IN}
1000 0000 0001	+(1/2048) V_{IN}
1000 0000 0000	0 V
0111 1111 1111	-(1/2048)V
0000 0000 0000	$-V_{IN}$

Bipolar Binary Code Table for Circuit of Figure 6

SINGLE SUPPLY OPERATION

The circuit of Figure 7 shows the Si7541 connected in a voltage switching configuration. The reference voltage is applied to OUT1 and OUT2 is connected to ground. The DAC output is available at pin 17 (V_{REF} pin) and has a constant output impedance equal to R_{REF}. The internal feedback resistor (pin 18) is not used. For better linearity in the voltage switching mode, the Si7240 should be specified.



C1 = 10 µF ELECTROLYTIC
C2 = 0.1µF CERAMIC

R1 || R2 = 10 kΩ

Figure 7. Single Supply Operation Using Voltage Switching

The reference voltage must always be positive in the voltage switching mode. If pin 1 goes below -0.3 V an internal diode will be turned on. If not limited a large current will flow and may cause device damage. Since the Si7541 is protected for SCR latch-up, removing the abnormally negative reference voltage will restore normal operation

APPLICATIONS (Cont'd)

provided the maximum current handling capacity (20 mA) has not been exceeded.

Loading on the reference voltage source is code dependent and the response time of the circuit is often determined by the ability of the reference voltage source to handle the changing load conditions. For this reason bypassing of the reference source is required. To maintain linearity the reference voltage at pin 1 should remain within 2.5 V of GND, for a V_{DD} = 15 V. If V_{DD} is reduced or the reference voltage increased, the DAC's linearity and differential nonlinearity will be degraded.

PIN DESCRIPTION

PIN NUMBER	DESCRIPTION	PIN NUMBER	DESCRIPTION
1	Current OUTPUT 1	10	Digital Input (Bit 7)
2	Current OUTPUT 2	11	Digital Input (Bit 8)
3	Digital Ground	12	Digital Input (Bit 9)
4	Digital Input (Bit 1) (MSB)	13	Digital Input (Bit 10)
5	Digital Input (Bit 2)	14	Digital Input (Bit 11)
6	Digital Input (Bit 3)	15	Digital Input (Bit 12) (LSB)
7	Digital Input (Bit 4)	16	Positive Power Supply
8	Digital Input (Bit 5)	17	Reference Input Voltage
9	Digital Input (Bit 6)	18	Internal Feedback Resistor

BURN-IN CIRCUITS