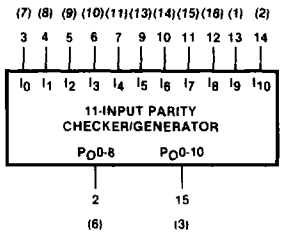
F10170 • F10570
11-INPUT PARITY CHECKER/GENERATOR

DESCRIPTION — The F10170 and F10570 are very high-speed 11-Input Parity Checker/Generators. It is useful for data processing, memory and data transmission applications. Two outputs are provided; P_O0-8 is HIGH when there is an odd number of HIGH inputs on I_0, I_1 to I_8. The output P_O0-10 will be HIGH if there is an odd number of HIGH inputs on I_0, I_1, to I_{10}. Unused inputs are held LOW by internal load resistors. Note from the logic diagram that there is only a single gate delay from inputs I_9 and I_{10} to the output P_O0-10 making them ideal for expansion when more than 11 inputs are required. Typical propagation delays are 4 ns from inputs I_0-I_8 to output P_O0-8, and 6 ns to output P_O0-10. Typical delay from I_9 and I_{10} to P_O0-10 is 2 ns.

PIN NAMES

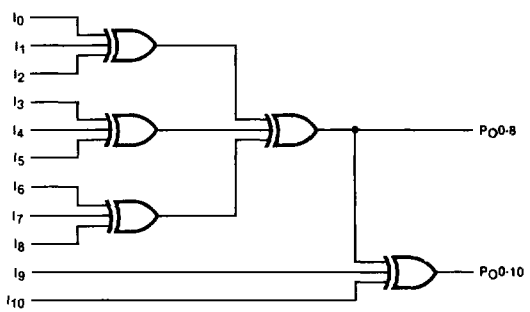
I_n	Inputs
P_O	Parity Odd

LOGIC SYMBOL

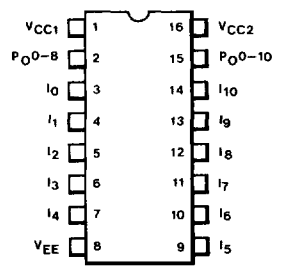


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)
( ) = Flatpak

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)
PACKAGE OUTLINE 6B



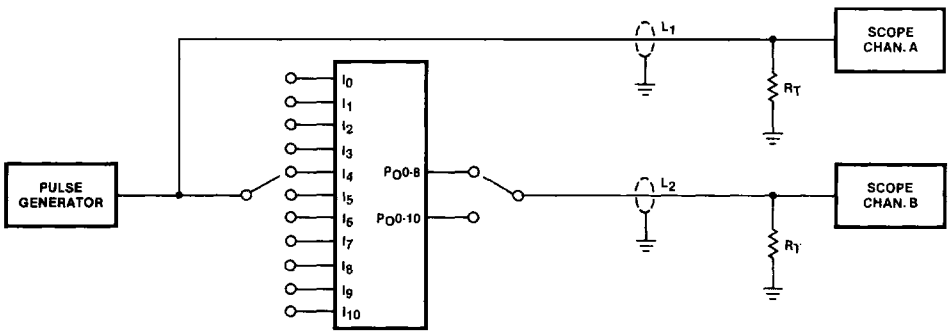
DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH (All Inputs)			220	μA	25°C	$V_{IN} = V_{IHA}$
I_{EE}	Power Supply Current	−68	−53		mA	25°C	Inputs and Outputs Open

SWITCHING CHARACTERISTICS: V_{EE} = −5.2 V, T_A = 25°C

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PLH}, t_{PHL}	Propagation Delay, HIGH to LOW LOW to HIGH Z (I_n to P_O0-8)	2.0	4.0	7.5	ns	See Figure 1
t_{THL}, t_{TLH}	Output Transition Time LOW to HIGH, HIGH to LOW 20% to 80%, 80% to 20%	1.5	2.0	3 3	ns	
t_{PLH}, t_{PHL}	Propagation Delay, HIGH to LOW LOW to HIGH (I_{10} to P_O0-10)	3.0		11.0	ns	

SWITCHING CIRCUIT AND WAVEFORM



L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance < 5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
$V_{CC1} = V_{CC2}$ = 2.0 V
V_{EE} = −3.2 V

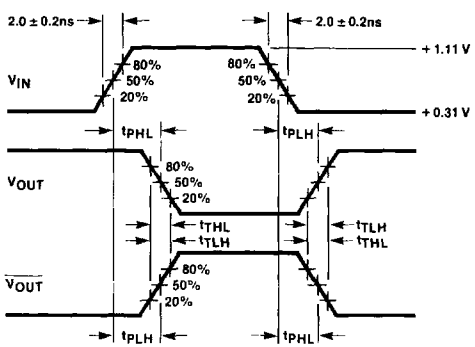


Fig. 1.