DRV8848 Dual H-Bridge Motor Driver

1 Features

- Dual H-Bridge Motor Driver
  - Single/Dual Brushed DC
  - Stepper
- PWM Control Interface
- Optional Current Regulation With 20-μs Fixed Off-Time
- High Output Current per H-Bridge
  - 2-A Maximum Driver Current at 12 V and T_A = 25°C
  - Parallel Mode Available Capable of 4-A Maximum Driver Current at 12 V and T_A = 25°C
- 4- to 18-V Operating Supply Voltage Range
- Low-Current 3-μA Sleep Mode
- Thermally-Enhanced Surface Mount Package
- Protection Features
  - VM Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)
  - Fault Condition Indication Pin (nFAULT)

2 Applications

- Appliances
- General Brushed and Stepper Motors
- Printers

3 Description

The DRV8848 provides a dual H-bridge motor driver for home appliances and other mechatronic applications. The device can be used to drive one or two DC motors, a bipolar stepper motor, or other loads. A simple PWM interface allows easy interfacing to controller circuits.

The output block of each H-bridge driver consists of N-channel and P-channel power MOSFETs configured as full H-bridges to drive the motor windings. Each H-bridge includes circuitry to regulate the winding current using a fixed off-time chopping scheme. The DRV8848 is capable of driving up to 2 A of current from each output or 4 A of current in parallel mode (with proper heat sinking, at 12 V and T_A = 25°C).

A low-power sleep mode is provided, which shuts down internal circuitry to achieve very-low quiescent current draw. This sleep mode can be set using a dedicated nSLEEP pin.

Internal protection functions are provided for UVLO, OCP, short-circuit protection, and overtemperature. Fault conditions are indicated by a nFAULT pin.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8848	HTSSOP (16)	5.00 mm × 6.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

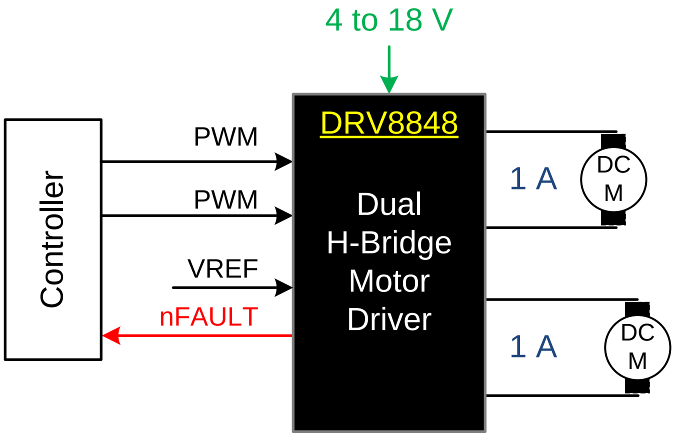


Table of Contents

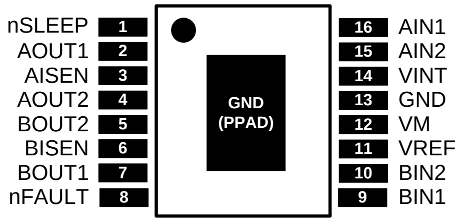
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (October 2014) to Revision A	Page
• Updated unit for $R_{DS(ON)}$	5
• Corrected lines for Figure 6	10
• Added *Community Resources*	19

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION	
NAME	NO.			
AIN1	16	I	Bridge A input 1	Controls AOUT1; tri-level input
AIN2	15	I	Bridge A input 2	Controls AOUT2; tri-level input
AISEN	3	O	Winding A sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
AOUT1	2	O	Winding A output	
AOUT2	4			
BIN1	9	I	Bridge B input 1	Controls BOUT1; internal pulldown
BIN2	10	I	Bridge B input 2	Controls BOUT2; internal pulldown
BISEN	6	O	Winding B sense	Connect to current sense resistor for bridge A, or GND if current regulation is not required
BOUT1	7	O	Winding B output	
BOUT2	5			
GND	13	PWR	Device ground	Both the GND pin and device PowerPAD must be connected to ground
	PPAD			
nFAULT	8	OD	Fault indication pin	Pulled logic low with fault condition; open-drain output requires external pullup
nSLEEP	1	I	Sleep mode input	Logic high to enable device; logic low to enter low-power sleep mode; internal pulldown
VINT	14	—	Internal regulator	Internal supply voltage; bypass to GND with 2.2-µF, 6.3-V capacitor
VM	12	PWR	Power supply	Connect to motor power supply; bypass to GND with a 0.1- and 10-µF (minimum) ceramic capacitor rated for VM
VREF	11	I	Full-scale current reference input	Voltage on this pin sets the full scale chopping current; short to VINT if not supplying an external reference voltage

External Components

COMPONENT	PIN 1	PIN 2	RECOMMENDED
C_{VM}	VM	GND	10-µF (minimum) ceramic capacitor rated for VM
C_{VM}	VM	GND	0.1-µF ceramic capacitor rated for VM
C_{VINT}	VINT	GND	6.3-V, 2.2-µF ceramic capacitor
R_{nFAULT}	VCC(1)	nFAULT	>1 kΩ
R_{AISEN}	AISEN	GND	Sense resistor, see *Typical Application* for sizing
R_{BISEN}	BISEN	GND	Sense resistor, see *Typical Application* for sizing

(1) VCC is not a pin on the DRV8848, but a VCC supply voltage pullup is required for open-drain output nFAULT; nFAULT may be pulled up to VINT

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range referenced with respect to GND (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Power supply voltage (VM)	–0.3	20	V
	Power supply voltage ramp rate (VM)	0	2	V/µs
	Internal regulator voltage (VINT)	–0.3	3.6	V
	Analog input pin voltage (VREF)	–0.3	3.6	V
	Control pin voltage (AIN1, AIN2, BIN1, BIN2, nSLEEP, nFAULT)	–0.3	7	V
	Continuous phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.3	V_{VM} + 0.6	V
	Continuous shunt amplifier input pin voltage (AISEN, BISEN) (2)	–0.6	0.6	V
	Peak drive current (AOUT1, AOUT2, BOUT1, BOUT2, AISEN, BISEN)	Internally limited		A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transients of ±1 V for less than 25 ns are acceptable.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{VM}	Power supply voltage range (1)	4	18	V
V_{VREF}	Reference rms voltage range (2)	1	3.3	V
f_{PWM}	Applied STEP signal	0	250	kHz
I_{VINT}	VINT external load current		1	mA
I_{rms}	Motor rms current per H-bridge (3)	0	1	A
T_A	Operating ambient temperature	–40	85	°C

(1) Note that $R_{DS(ON)}$ increases and maximum output current is reduced at VM supply voltages below 5 V.
(2) Operational at VREF between 0 and 1 V, but accuracy is degraded.
(3) Power dissipation and thermal limits must be observed.

6.4 Thermal Information

THERMAL METRIC (1)		DRV8848 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	28.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VM, VINT)						
V_{VM}	VM operating voltage		4		18	V
I_{VM}	VM operating supply current	V_{VM} = 12 V, excluding winding current, nSLEEP = 1	2.5	3.8	5.5	mA
I_{VMQ}	VM sleep mode supply current	V_{VM} = 12 V, nSLEEP = 0	0.5	1.2	3	μA
t_{SLEEP}	Sleep time	nSLEEP = 0 to sleep mode			1	ms
t_{WAKE}	Wake time	nSLEEP = 1 to output transition			1	ms
t_{ON}	Power-on time	$V_{VM} > V_{UVLO}$ rising to output transition			1	ms
V_{INT}	VINT voltage	V_{VM} > 4 V, I_{OUT} = 0 A to 1 mA	3.13	3.3	3.47	V
LOGIC-LEVEL INPUTS (BIN1, BIN2, NSLEEP)						
V_{IL}	Input logic low voltage		0		0.7	V
V_{IH}	Input logic high voltage		1.6		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	μA
I_{IH}	Input logic high current	V_{IN} = 5 V	1		30	μA
R_{PD}	Pulldown resistance	BIN1, BIN2		200		kΩ
		nSLEEP		500		
t_{DEG}	Input deglitch time	AIN1 or AIN2		400		ns
		BIN1 or BIN2		200		ns
t_{PROP}	Propagation delay	AIN1 or AIN2 edge to output change		800		ns
		BIN1 or BIN2 edge to output change		400		ns
TRI-LEVEL INPUTS (AIN1, AIN2)						
V_{IL}	Tri-level input logic low voltage		0		0.7	V
V_{IZ}	Tri-level input Hi-Z voltage			1.1		V
V_{IH}	Tri-level input logic high voltage		1.6		5.5	V
V_{HYS}	Tri-level input hysteresis		100			mV
I_{IL}	Tri-level input logic low current	V_{IN} = 0 V	–30		–1	μA
I_{IH}	Tri-level input logic high current	V_{IN} = 5 V	1		30	μA
R_{PD}	Tri-level pulldown resistance	To GND		170		kΩ
R_{PU}	Tri-level pullup resistance	To VINT		340		kΩ
CONTROL OUTPUTS (NFAULT)						
V_{OL}	Output logic low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output logic high leakage	V_O = 3.3 V	–1		1	μA
MOTOR DRIVER OUTPUTS (AOUT1, AOUT2, BOUT1, BOUT2)						
$R_{DS(ON)}$	High-side FET on-resistance	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C		550		mΩ
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C(1)		660		
$R_{DS(ON)}$	Low-side FET on-resistance	V_{VM} = 12 V, I = 0.5 A, T_J = 25°C		350		mΩ
		V_{VM} = 12 V, I = 0.5 A, T_J = 85°C(1)		420		
I_{OFF}	Off-state leakage current	V_{VM} = 5 V, T_J = 25°C	–1		1	μA
t_{RISE}	Output rise time			60		ns
t_{FALL}	Output fall time			60		ns
t_{DEAD}	Output dead time	Internal dead time		200		ns
PWM CURRENT CONTROL (VREF, AISEN, BISEN)						
I_{REF}	Externally applied VREF input current	V_{VREF} = 1 to 3.3 V			1	μA
V_{TRIP}	xISEN trip voltage	For 100% current step with V_{VREF} = 3.3 V		500		mV

(1) Not tested in production; limits are based on characterization data

Electrical Characteristics (continued)

T_A = 25°C, over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{BLANK}	Current sense blanking time			1.8		μs
A_{ISENSE}	Current sense amplifier gain	Reference only		6.6		V/V
t_{OFF}	Current control constant off time			20		μs
PROTECTION CIRCUITS						
V_{UVLO}	VM undervoltage lockout	V_{VM} falling; UVLO report			2.9	V
		V_{VM} rising; UVLO recovery			3	
I_{OCP}	Overcurrent protection trip level		2			A
t_{DEG}	Overcurrent deglitch time			2.8		μs
t_{OCP}	Overcurrent protection period			1.6		ms
T_{TSD} (1)	Thermal shutdown temperature	Die temperature T_J	150	160	180	°C
T_{HYS} (1)	Thermal shutdown hysteresis	Die temperature T_J		50		°C

6.6 Timing Requirements

T_A = 25°C, over recommended operating conditions unless otherwise noted

NO.			MIN	MAX	UNIT
1	t_1	Delay time, xIN1 to xOUT1	100	600	ns
2	t_2	Delay time, xIN2 to xOUT1	100	600	ns
3	t_3	Delay time, xIN1 to xOUT2	100	600	ns
4	t_4	Delay time, xIN2 to xOUT2	100	600	ns
5	t_F	Output rise time	50	150	ns
6	t_R	Output fall time	50	150	ns

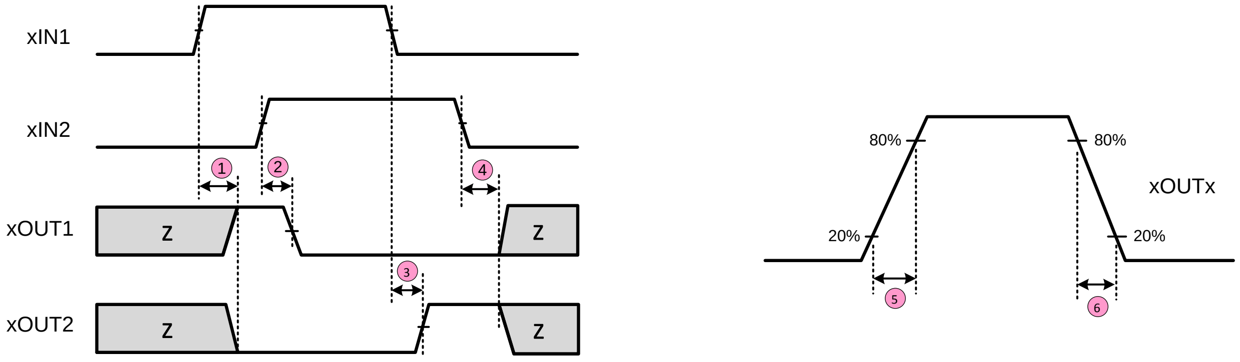


Figure 1. Timing Diagram

6.7 Typical Characteristics

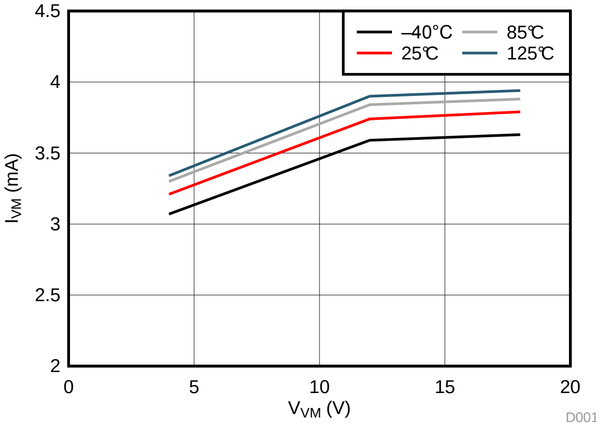


Figure 2. I_{VM} vs V_{VM}

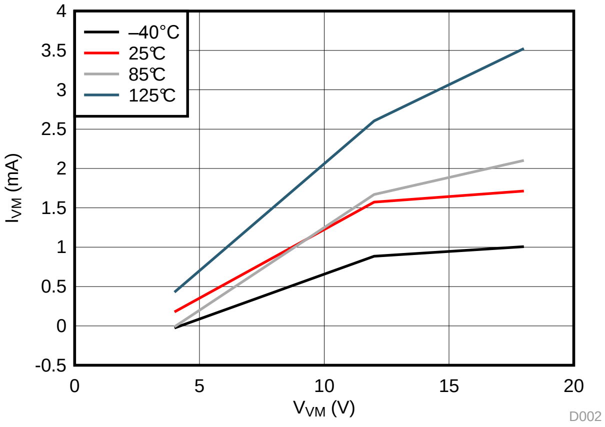


Figure 3. I_{VMQ} vs V_{VM}

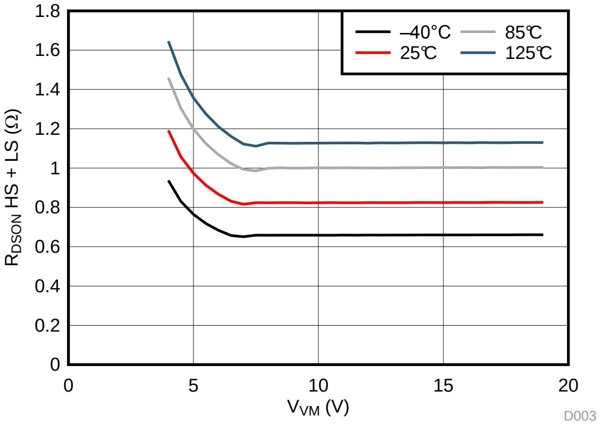


Figure 4. R_{DSON} vs V_{VM}

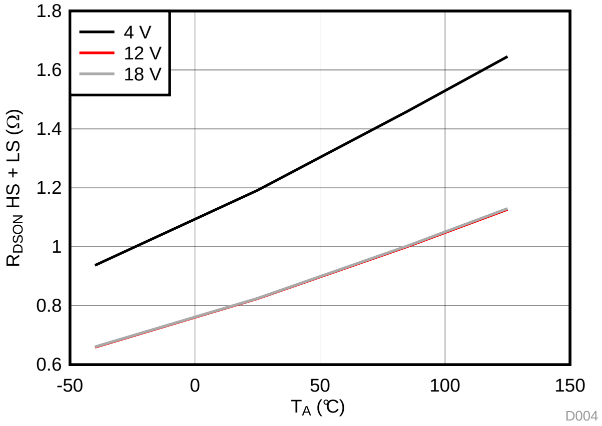


Figure 5. R_{DSON} vs Temperature

7 Detailed Description

7.1 Overview

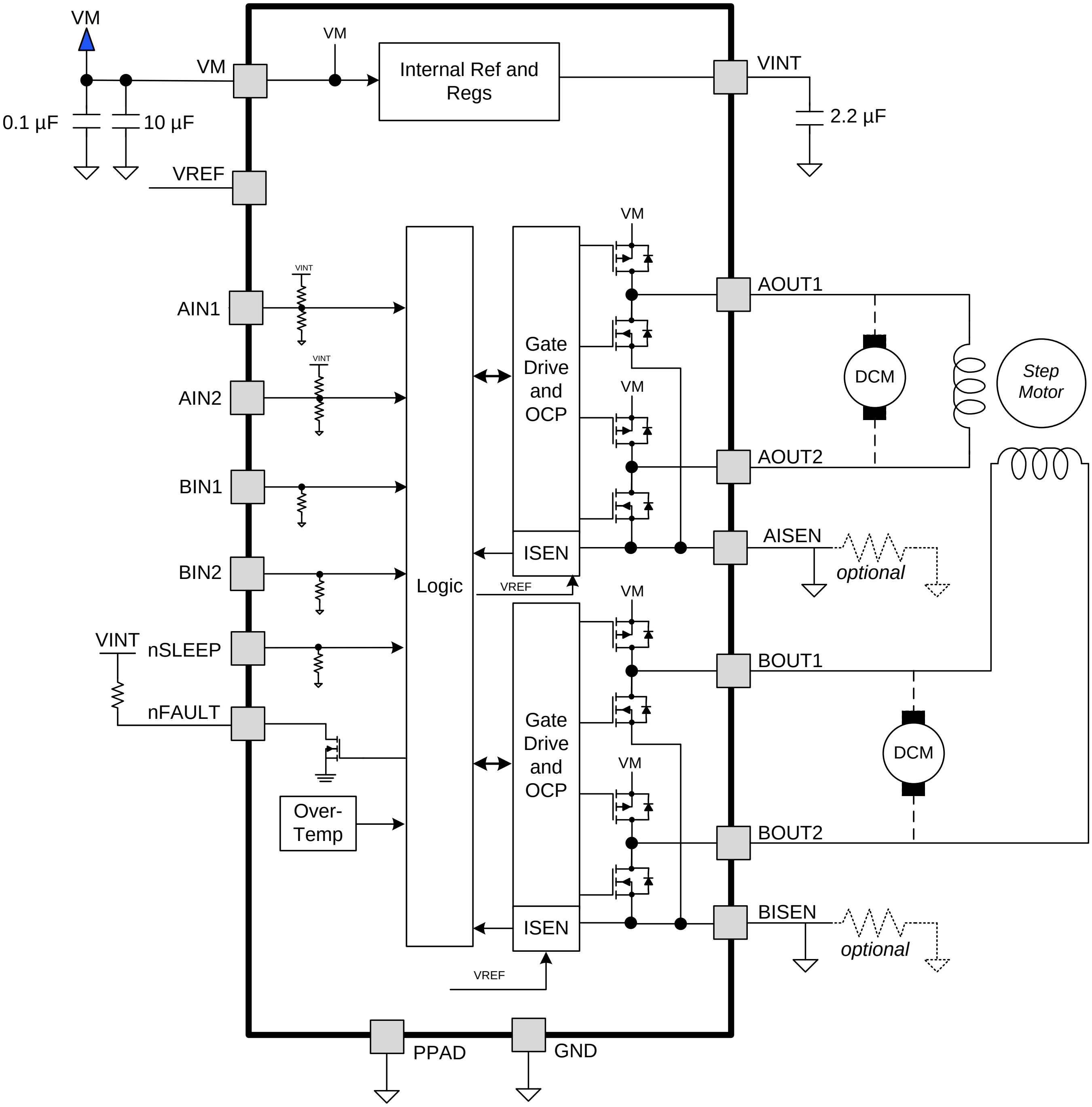
The DRV8848 is an integrated motor driver solution for two DC motors or a bipolar stepper motor. The device integrates two H-bridges that use NMOS low-side drivers and PMOS high-side drivers and current sense regulation circuitry. The DRV8848 can be powered with a supply range between 4 to 18 V and is capable of providing an output current to 1-A rms.

A simple PWM interface allows easy interfacing to the controller circuit.

The current regulation uses a fixed off-time (t_{OFF}) PWM scheme. The current regulation trip point is controlled by the value of the sense resistor and the voltage applied to VREF.

A low-power sleep mode is included, which allows the system to save power when not driving the motor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 PWM Motor Drivers

DRV8848 contains two identical H-bridge motor drivers with current-control PWM circuitry. Figure 6 shows a block diagram of the circuitry.

Feature Description (continued)

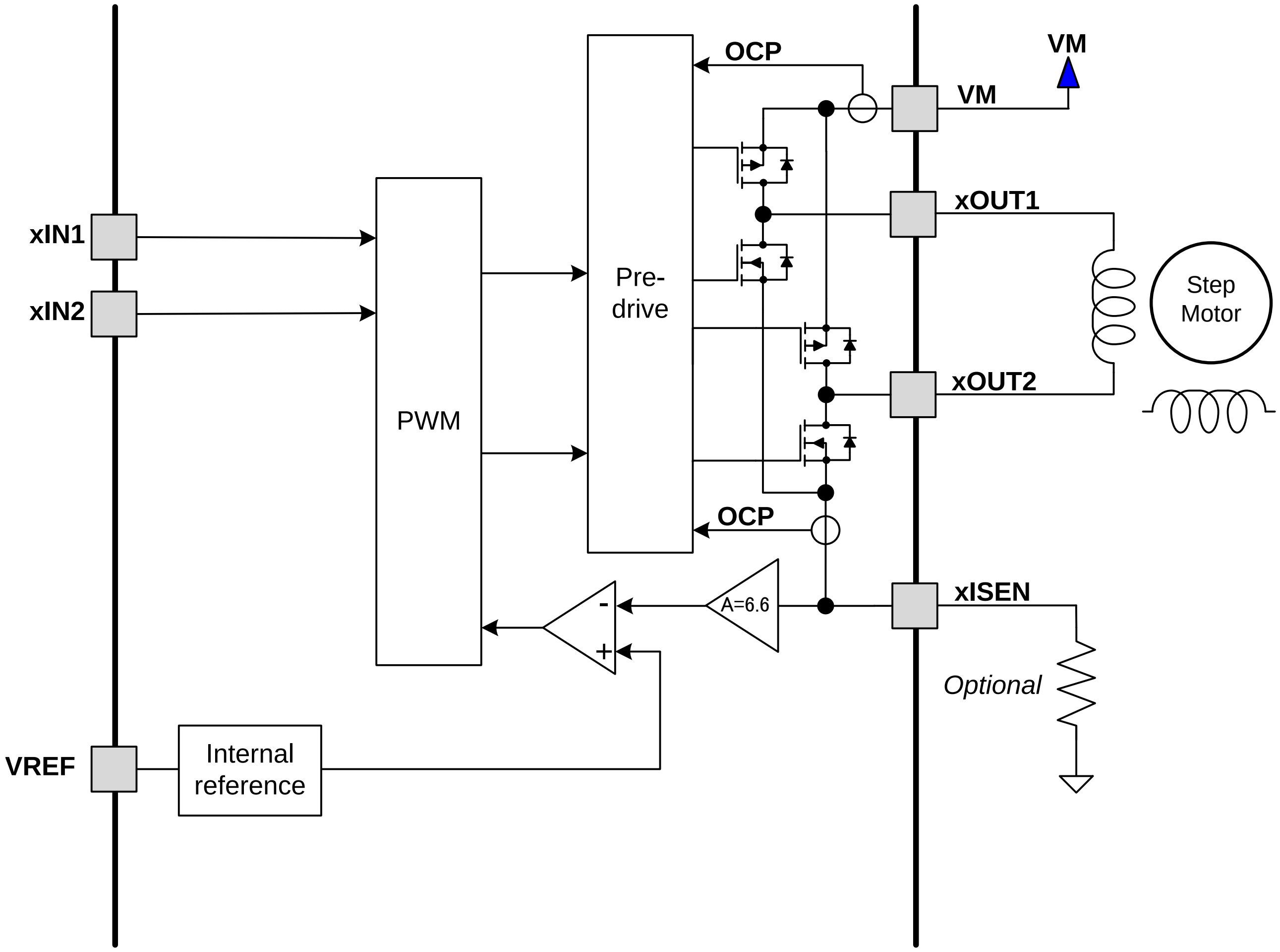


Figure 6. PWM Motor Driver Circuitry

7.3.2 Bridge Control

Table 1 shows the logic for the inputs xIN1 and xIN2.

Table 1. Bridge Control

xIN1	xIN2	xOUT1	xOUT2	Function (DC Motor)
0	0	Z	Z	Coast (fast decay)
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake (slow decay)

NOTE

Pins AIN1 and AIN2 are tri-level, so when they are left Hi-Z, they are not internally pulled to logic low. When AIN1 or AIN2 are set to Hi-Z and not in parallel mode, the output driver maintains the previous state.

7.3.3 Parallel Operation

The two drivers can be used in parallel to deliver twice the current to a single motor. To enter parallel mode, AIN1 and AIN2 must be left Hi-Z during power-up or when exiting sleep mode (nSLEEP toggling from 0 to 1). BIN1 and BIN2 are used to control the drivers. Tie AISEN and BISEN to a single sense resistor if current control is desired. To exit parallel mode, AIN1 and AIN2 must be driven high or low and the device must be powered-up or exit sleep mode. Figure 7 shows a block diagram of the device using parallel mode.

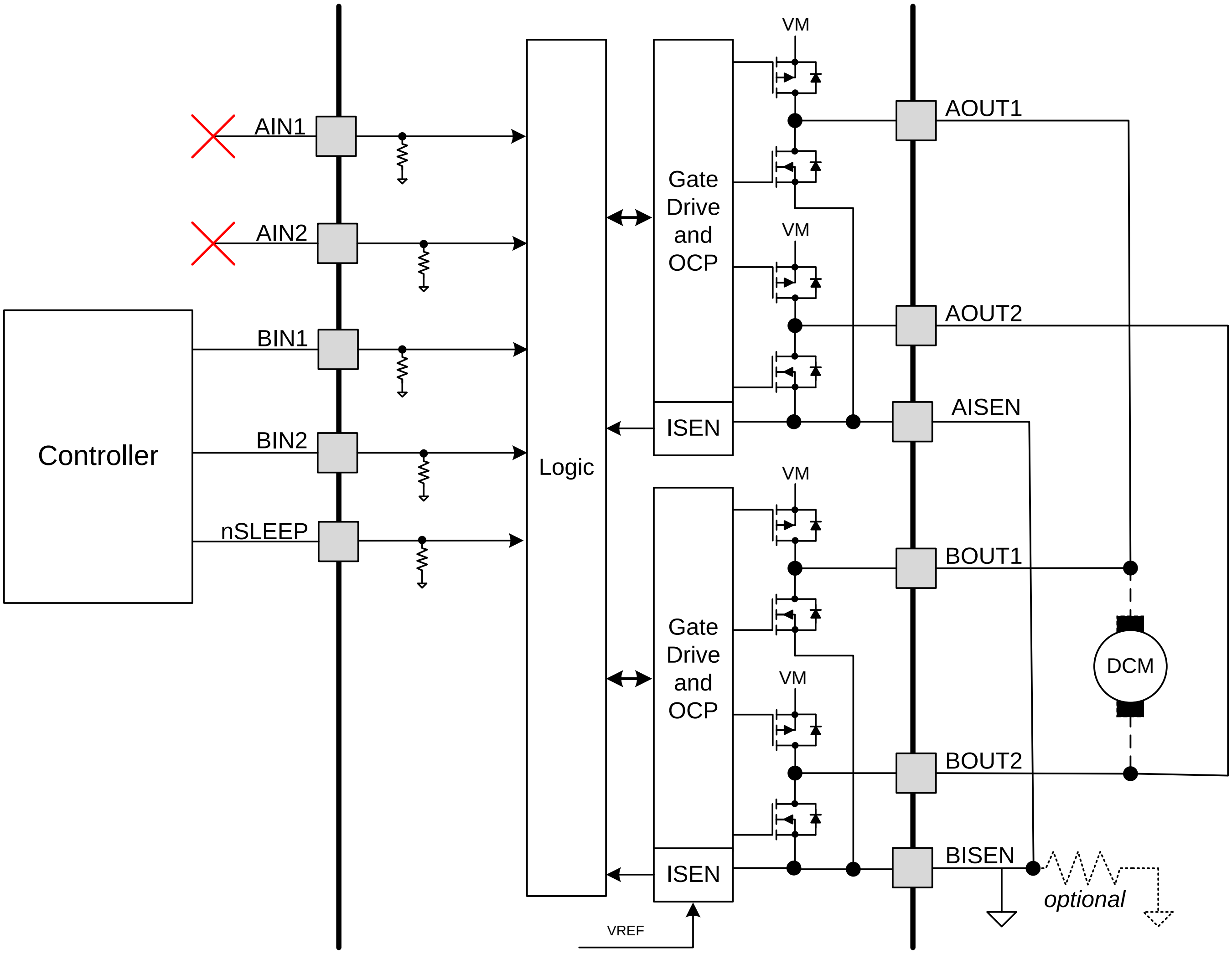


Figure 7. Parallel Mode Operation

7.3.4 Current Regulation

The current through the motor windings is regulated by a fixed-off-time PWM current regulation circuit. With DC brushed motors, current regulation can be used to limit the stall current (which is also the startup current) of the motor.

Current regulation works as follows:

When an H-bridge is enabled, current rises through the winding at a rate dependent on the supply voltage and inductance of the winding. If the current reaches the current chopping threshold, the bridge disables the current for a time t_{OFF} before starting the next PWM cycle. Note that immediately after the current is enabled, the voltage on the xISEN pin is ignored for a period of time (t_{BLANK}) before enabling the current sense circuitry. This blanking time also sets the minimum on-time of the PWM cycle.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor, connected to the xISEN pin, with a reference voltage. The reference voltage is derived from the voltage applied to the VREF pin and it is V_{VREF} / 6.6. The VREF pin can be tied, on board, to the 3.3 V – VINT pin, or it can be externally forced to a desired VREF voltage.

The full scale chopping current in a winding is calculated as follows:

$$I_{FS} = \frac{V_{VREF}}{6.6 \times R_{ISENSE}} \tag{1}$$

where

- I_{FS} is the regulated current.
- V_{VREF} is the voltage on the VREF pin.
- R_{ISENSE} is the resistance of the sense resistor.

Example: If V_{VREF} is 3.3 V and a 500-mΩ sense resistor is used, the full-scale chopping current is 3.3 V / (6.6 × 500 mΩ) = 1 A.

Note that if the current control is not needed, the xISEN pins may be connected directly to ground. In this case, VREF should be connected to VINT.

7.3.5 Current Recirculation and Decay Modes

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached (see case 1 in Figure 8).

After the chopping current threshold is reached, the drive current is interrupted, but due to the inductive nature of the motor, current must continue to flow for some period of time. This is called recirculation current. To handle this recirculation current, the DRV8848 H-bridge operates in mixed decay mode.

Mixed decay is a combination of fast and slow decay modes. In fast decay mode, the opposite drivers are turned on to allow the current to decay (see case 2 in Figure 8). If the winding current approaches zero, while in fast decay, the bridge is disabled to prevent any reverse current flow. In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge (see case 3 in Figure 8). Mixed decay starts with fast decay, then goes to slow decay. In DRV8848, the mixed decay ratio is 25% fast decay and 75% slow decay (as shown in Figure 9).

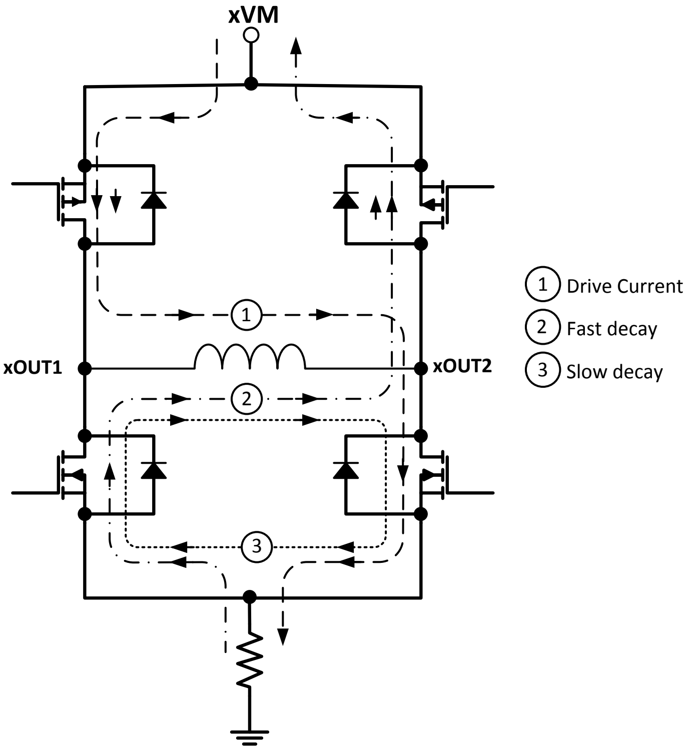


Figure 8. Decay Modes

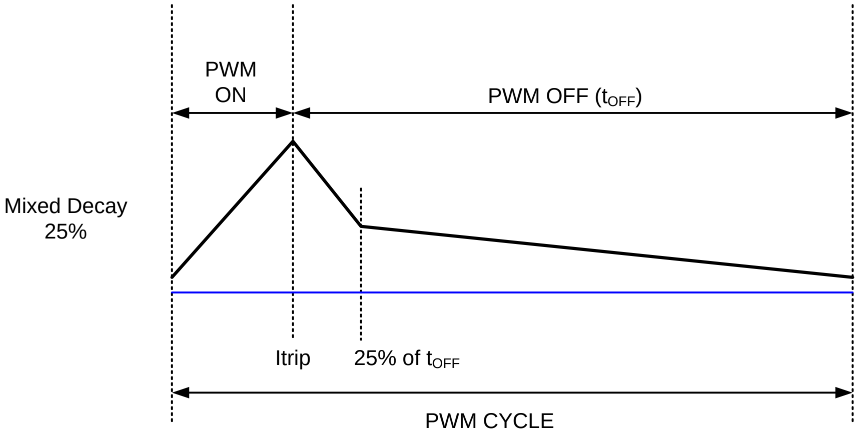


Figure 9. Mixed Decay

7.3.6 Protection Circuits

The DRV8848 is fully protected against undervoltage, overcurrent, and overtemperature events.

7.3.6.1 OCP

An analog current limit circuit on each FET limits the current through the FET by limiting the gate drive. If this analog current limit persists for longer than the OCP deglitch time t_{OCP}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. The device remains disabled until the retry time t_{RETRY} occurs. The OCP is independent for each H-bridge.

Overcurrent conditions are detected independently on both high-side and low-side devices; that is, a short to ground, supply, or across the motor winding all result in an OCP event. Note that OCP does not use the current sense circuitry used for PWM current control, so OCP functions even without presence of the xISEN resistors.

7.3.6.2 TSD

If the die temperature exceeds safe limits T_{TSD}, all FETs in the H-bridge are disabled and the nFAULT pin is driven low. After the die temperature has fallen to a safe level, operation automatically resumes. The nFAULT pin is released after operation has resumed.

7.3.6.3 UVLO

If at any time the voltage on the VM pin falls below the UVLO falling threshold voltage, V_{UVLO}, all circuitry in the device is disabled, and all internal logic is reset. Operation resumes when V_{VM} rises above the UVLO rising threshold. The nFAULT pin is driven low during an undervoltage condition and is released after operation has resumed.

Table 2. Fault Handling

FAULT	ERROR REPORT	H-BRIDGE	INTERNAL CIRCUITS	RECOVERY
VM undervoltage (UVLO)	nFAULT unlatched	Disabled	Shut down	System and fault clears on recovery
Overcurrent (OCP)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery and motor is driven after time, t_{RETRY}
Thermal shutdown (TSD)	nFAULT unlatched	Disabled	Operating	System and fault clears on recovery

7.4 Device Functional Modes

The DRV8848 is active unless the nSLEEP pin is brought logic low. In sleep mode, the VINT regulator is disabled and the H-bridge FETs are disabled Hi-Z. Note that t_{SLEEP} must elapse after a falling edge on the nSLEEP pin before the device is in sleep mode. The DRV8848 is brought out of sleep mode automatically if nSLEEP is brought logic high. Note that t_{WAKE} must elapse before the output change state after wake-up.

When V_{VM} falls below the VM UVLO threshold (V_{UVLO}), the output driver, internal logic, and VINT regulator are reset.

Table 3. Functional Modes

MODE	CONDITION	H-BRIDGE	VINT
Operating	$4\text{ V} < V_{VM} < 18\text{ V}$ nSLEEP pin = 1	Operating	Operating
Sleep	$4\text{ V} < V_{VM} < 18\text{ V}$ nSLEEP pin = 0	Disabled	Disabled
Fault	Any fault condition met	Disabled	Depends on fault

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8848 is used in stepper or brushed DC motor control.

8.2 Typical Application

The user can configure the DRV8848 with the following design procedure.

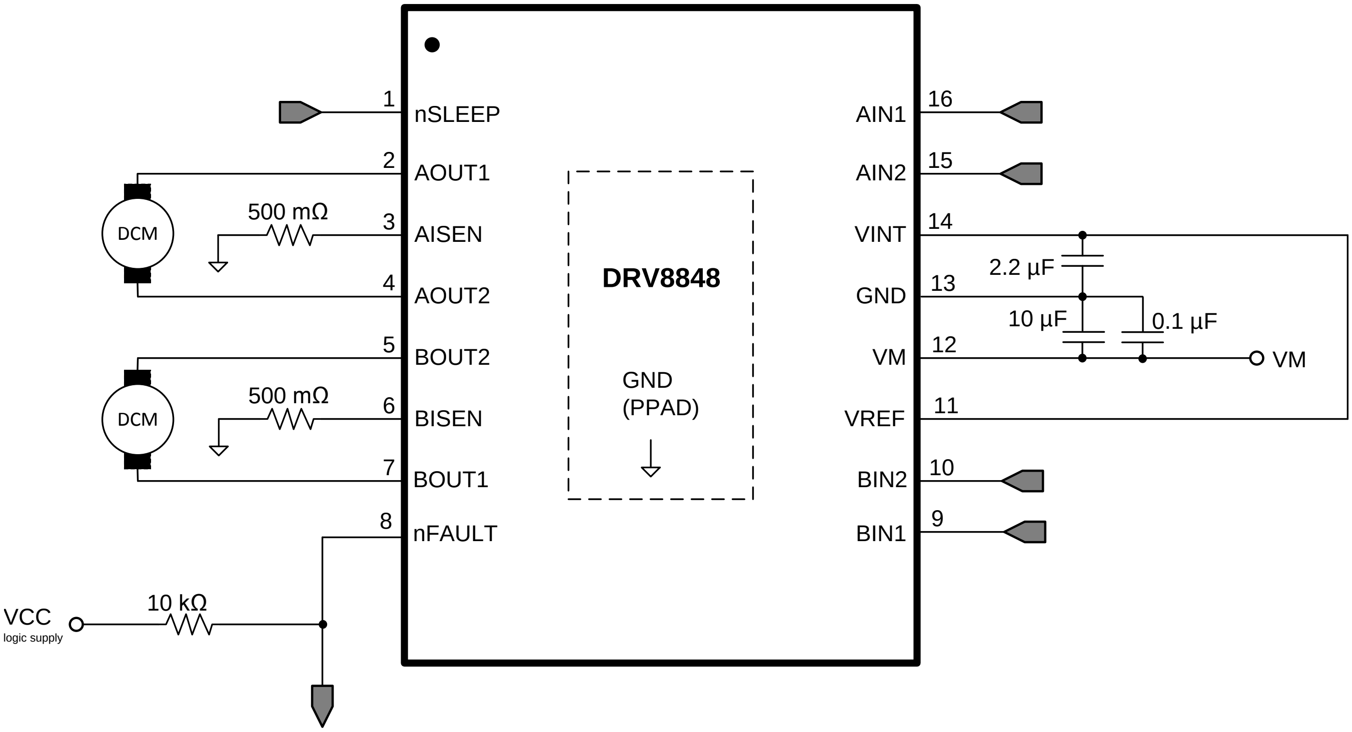


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

Table 4 gives design input parameters for system design.

Table 4. Design Parameters

DESIGN PARAMETER	REFERENCE	EXAMPLE VALUE
Nominal supply voltage	V_{VM}	12 V
Supply voltage range		4 to 18 V
Motor winding resistance	R_L	3 Ω/phase
Motor winding inductance	L_L	330 µH/phase
Target chopping current	I_{CHOP}	500 mA
Chopping current reference voltage	V_{VREF}	3.3 V

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The chopping current (I_{CHOP}) is the maximum current driven through either winding. This quantity depends on the sense resistor value (R_{XISEN}).

$$I_{CHOP} = \frac{V_{VREF}}{6.6 \times R_{XISEN}} \tag{2}$$

I_{CHOP} is set by a comparator which compares the voltage across R_{XISEN} to a reference voltage. Note that I_{CHOP} must follow Equation 3 to avoid saturating the motor.

$$I_{CHOP}\ (A) < \frac{V_{VM}\ (V)}{R_L\ (\Omega) + 2 \times R_{DS(ON)}\ (\Omega) + R_{XISEN}\ (\Omega)}$$

where

- V_{VM} is the motor supply voltage.
- R_L is the motor winding resistance. (3)

8.2.3 Application Curves

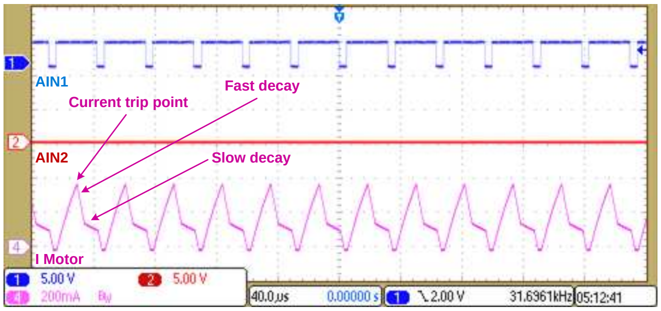


Figure 11. Current Regulation

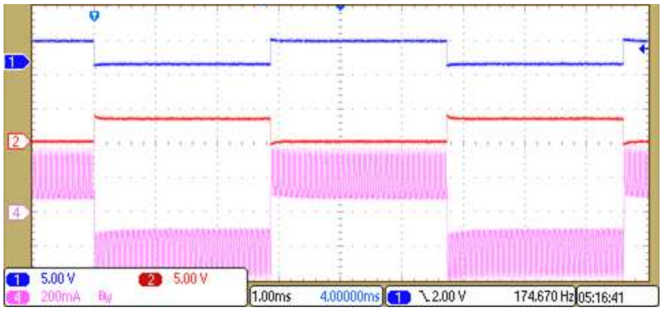


Figure 12. Stepper Mode Operation

9 Power Supply Recommendations

The DRV8848 is designed to operate from an input voltage supply (V_{VM}) range between 4 and 18 V. Place a 0.1-µF ceramic capacitor rated for VM as close to the DRV8848 as possible. In addition, the user must include a bulk capacitor of at least 10 µF on VM.

9.1 Bulk Capacitance Sizing

Bulk capacitance sizing is an important factor in motor drive system design. It depends on a variety of factors including:

- Type of power supply
- Acceptable supply voltage ripple
- Parasitic inductance in the power supply wiring
- Type of motor (brushed DC, brushless DC, stepper)
- Motor startup current
- Motor braking method

The inductance between the power supply and motor drive system limits the rate that current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. Size the bulk capacitance to meet acceptable voltage ripple levels.

The data sheet provides a recommended minimum value, but system-level testing is required to determine the appropriate-sized bulk capacitor.

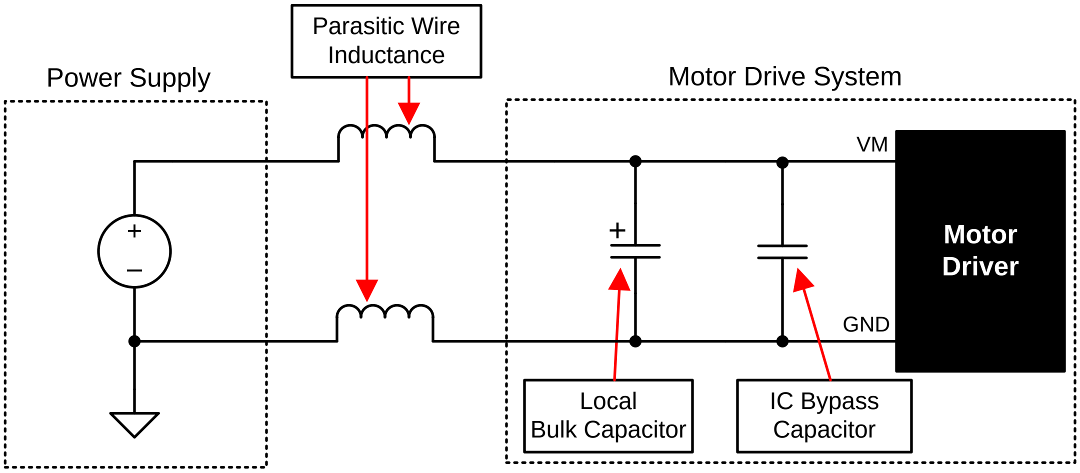


Figure 13. Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Bypass the VM terminal to GND using a low-ESR ceramic bypass capacitor with a recommended value of 10 µF rated for VM. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin.

Bypass VINT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

10.2 Layout Example

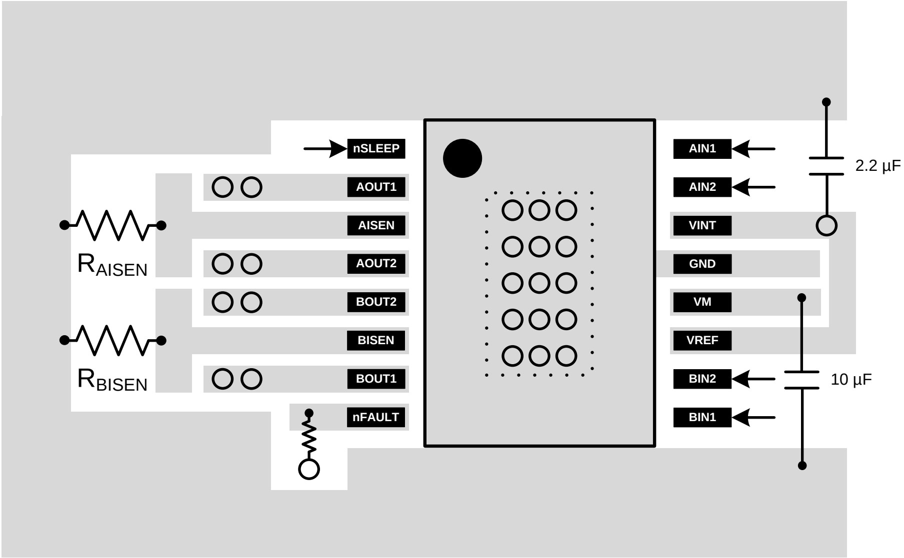


Figure 14. Layout Recommendation

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8848PWP	ACTIVE	HTSSOP	PWP	16	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848	Samples
DRV8848PWPR	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV8848	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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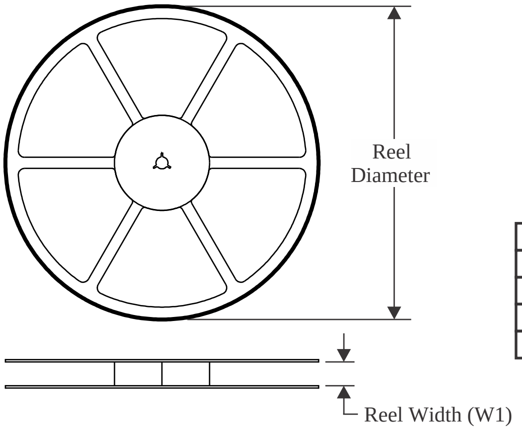
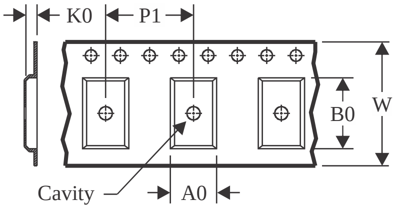
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

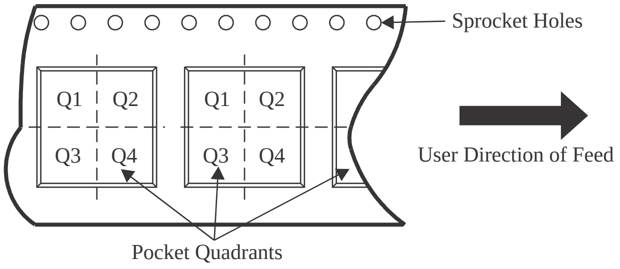


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

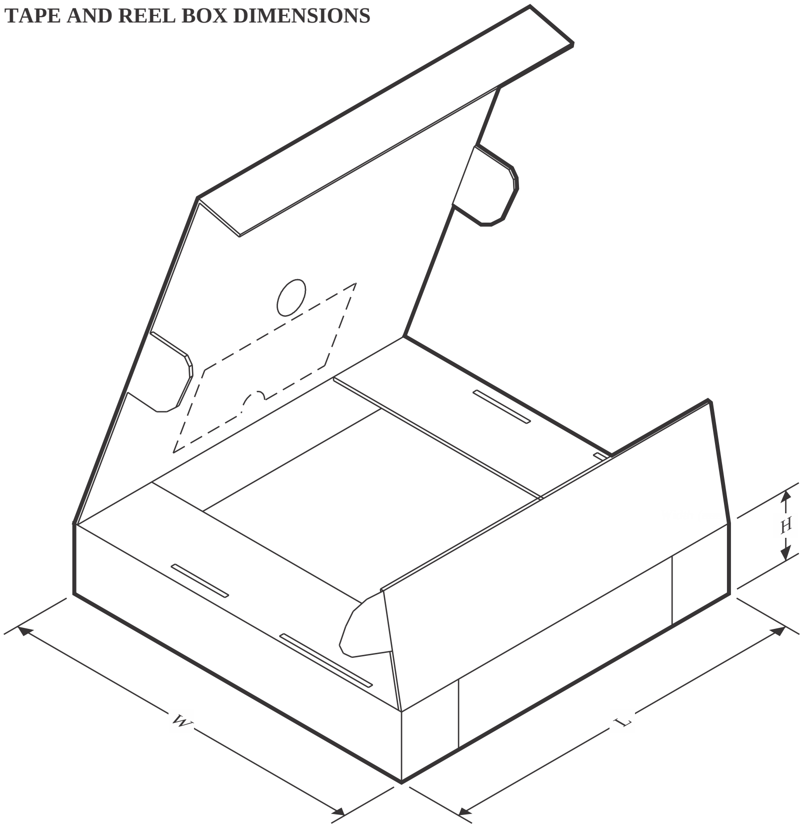
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8848PWPR	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

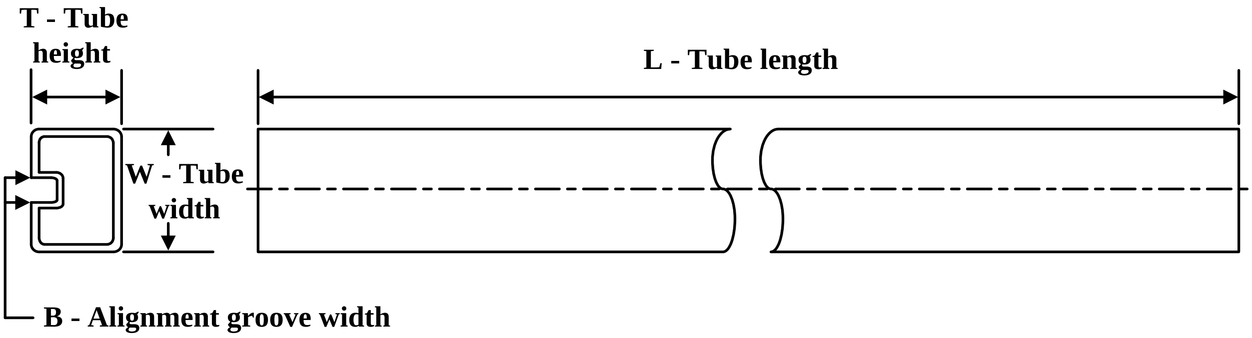
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8848PWPR	HTSSOP	PWP	16	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

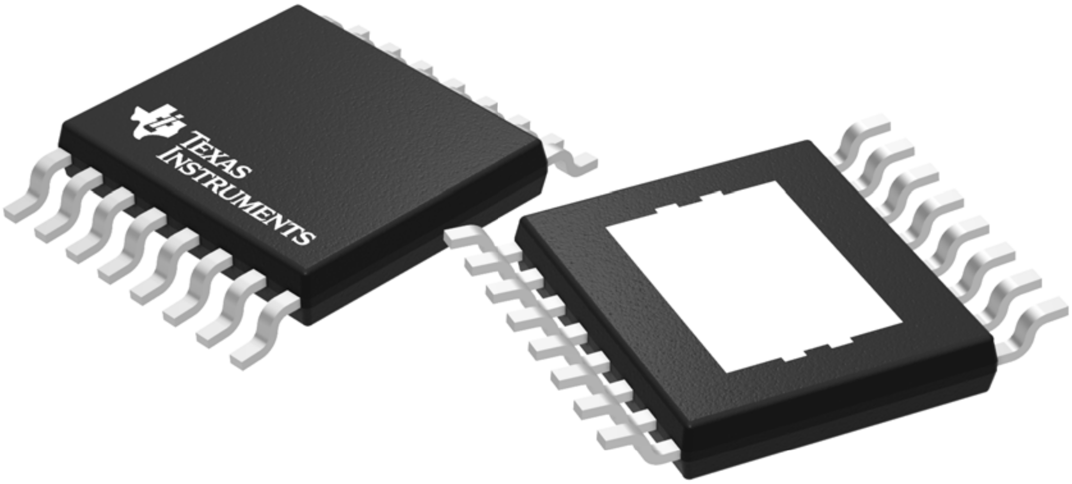
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8848PWP	PWP	HTSSOP	16	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

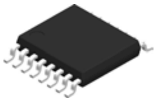
PWP 16

PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

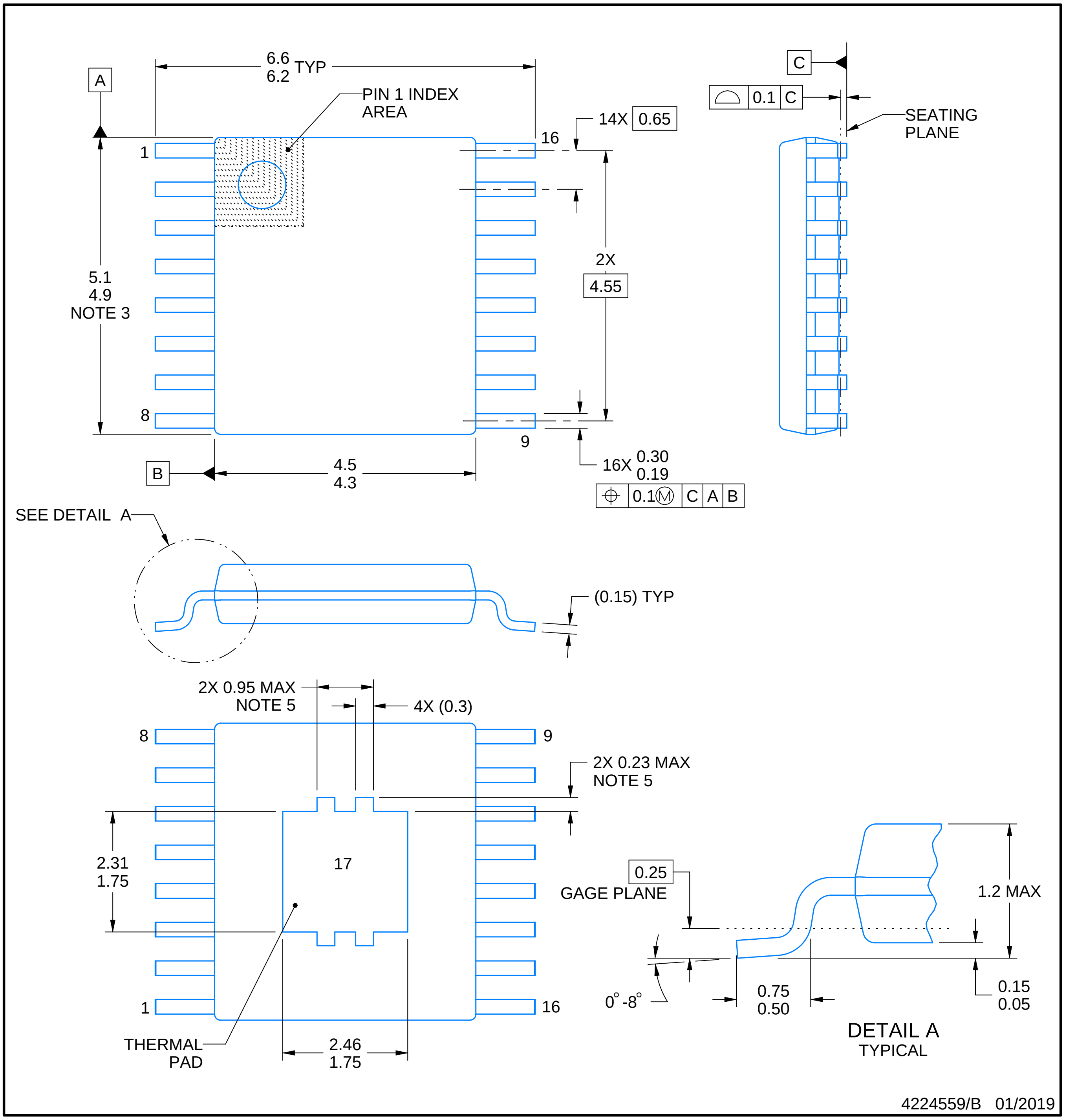


PACKAGE OUTLINE

PWP0016C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

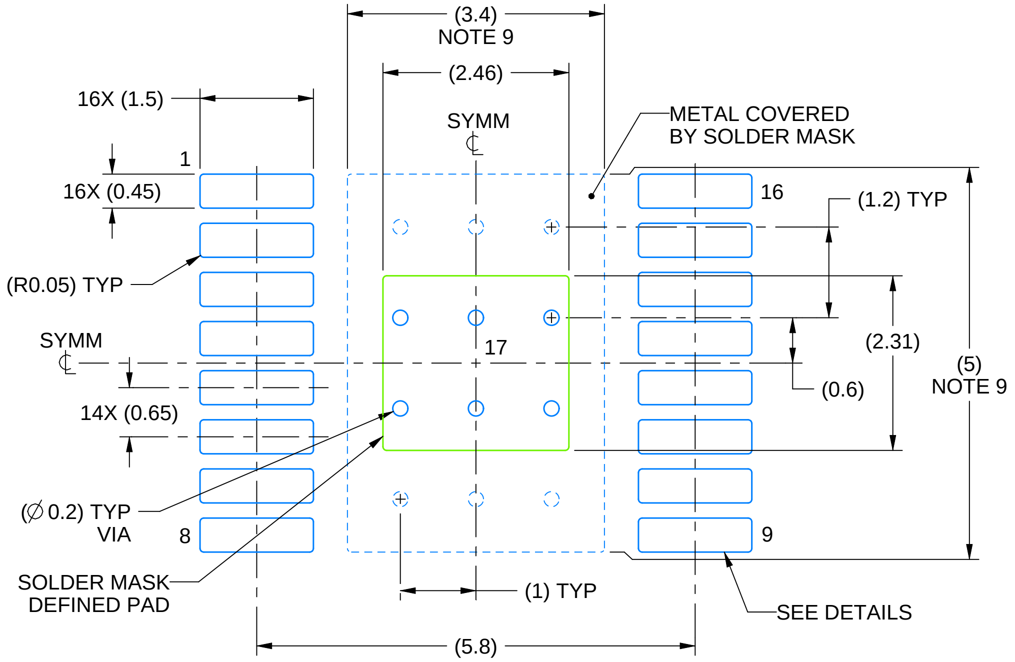


4224559/B 01/2019

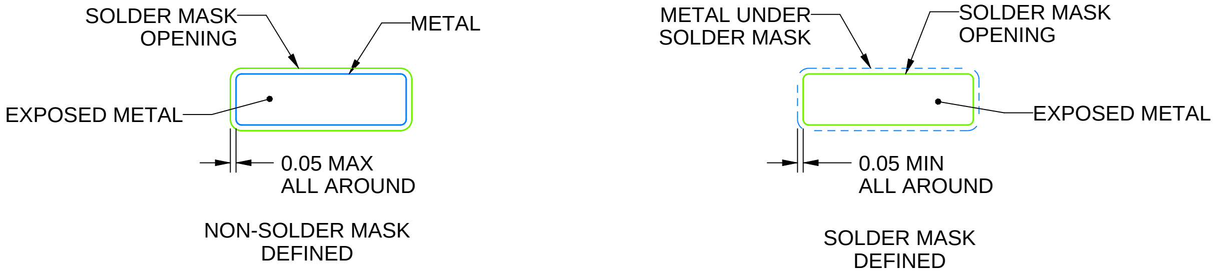
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



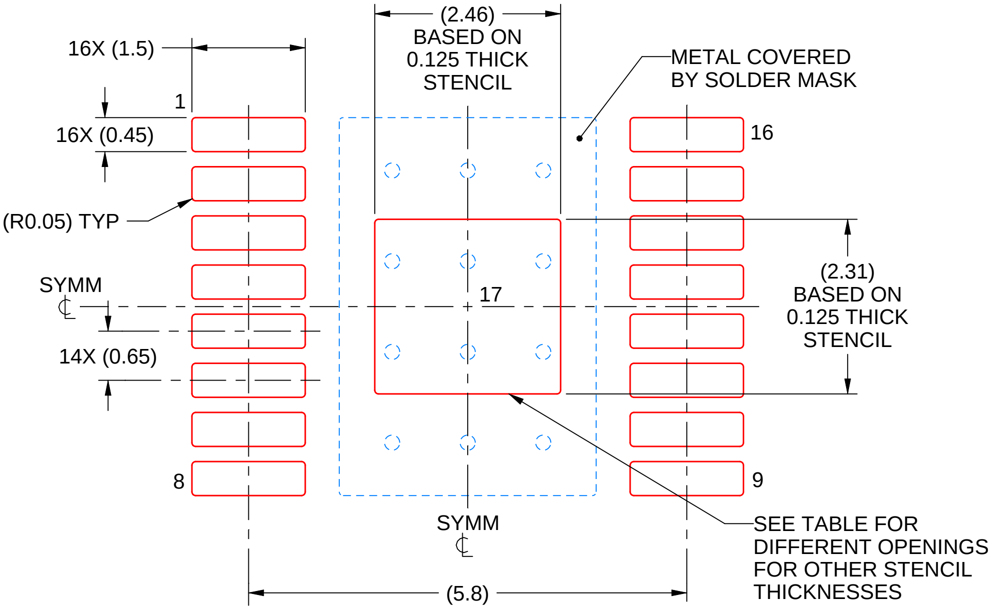
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 2.58
0.125	2.46 X 2.31 (SHOWN)
0.15	2.25 X 2.11
0.175	2.08 X 1.95

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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