MIL-PRF-38534 AND 38535 CERTIFIED FACILITY

600V ISOLATED HALF BRIDGE GATE DRIVER

4900

M.S.KENNEDY CORP.
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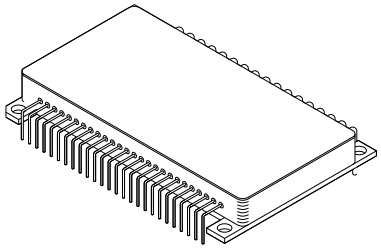


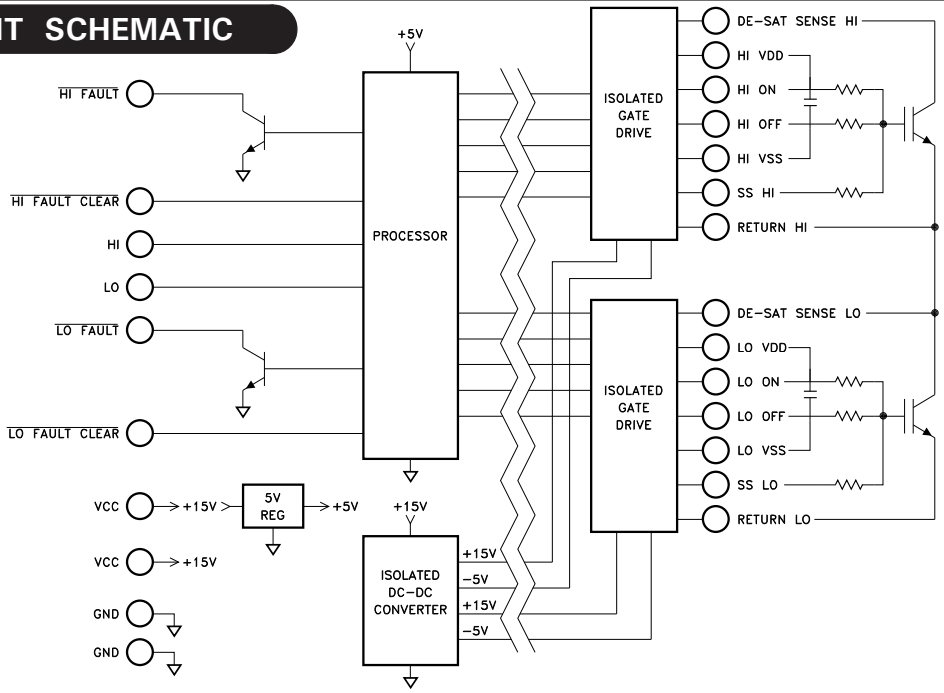
FEATURES:

- Floating Channels up to 600V
- Up to 8 Amp Peak Source and Sink Current
- De-Saturation Protection/Shutdown
- Individual ON, OFF and Soft Shutdown Pins for Each IGBT Gate
- Simultaneous Conduction Lockout
- Contact MSK for MIL-PRF-38534 Qualification Status

DESCRIPTION:

The MSK 4900 is a complete isolated half bridge gate driver hybrid capable of working to 600V channel isolation and 8 amps peak turn-on and turn-off current. Housed in an isolated, convenient bolt-down hermetic package, the MSK 4900 houses the entire isolated DC-DC converter circuitry and opto-isolators for logic signals. The input logic prevents simultaneous conduction by locking out both high side and low side drives in case both inputs are asserted ON at the same time. Each gate drive is capable of sourcing and sinking up to 8 amps peak current. The turn-on and turn-off pins are separate to allow separate gate current control. Upon detection of a de-saturation condition, a FAULT is presented and the transistor is shutdown by a separate controlled shutdown pin. There are two modes available for clearing a FAULT. They are selected at device power up. MANUAL FAULT CLEAR MODE requires the FAULT to be cleared by the system before normal operation will begin again. AUTOMATIC FAULT CLEAR MODE clears the FAULT a short period after shutdown at which time normal operation commences. The MSK 4900 has good thermal conductivity due to an isolated substrate/package design that allows direct heat sinking of the device without insulators.

EQUIVALENT SCHEMATIC



TYPICAL APPLICATIONS

- Inverter Bridge Gate Drive
- Motor Control Bridge Gate Drive

PIN-OUT INFORMATION

1 VCC1	13 TP4	25 NC	37 SOFT SHUTDOWN HI
2 VCC1	14 TP3	26 NC	38 HI OFF
3 GND1	15 LO	27 NC	39 HI VSS
4 GND1	16 NC	28 NC	40 HI ON
5 TP1	17 VCC2	29 SOFT SHUTDOWN LO	41 HI VDD
6 TP5	18 VCC2	30 LO OFF	42 RETURN HI
7 TP2	19 GND2	31 LO VSS	43 DE-SAT SENSE HI
8 $\overline{\text{LO FAULT CLEAR}}$	20 GND2	32 LO ON	
9 $\overline{\text{HI FAULT CLEAR}}$	21 GND2	33 LO VDD	
10 $\overline{\text{LO FAULT}}$	22 NC	34 RETURN LO	
11 $\overline{\text{HI FAULT}}$	23 NC	35 DE-SAT SENSE LO	
12 HI	24 NC	36 NC	

ABSOLUTE MAXIMUM RATINGS ⑥

High Voltage Isolation ⑨ 600V
Logic Input Voltage 5.5V
Vcc Supply 15.75V
Continuous Output Current 90mA
Peak Ouput Current 8A
Thermal Resistance
(output drivers - junction to case) . . . . . .17°C/W
Maximum Current Sink-open collectors 10mA

T_{ST} Storage Temperature Range ⑩ . . . -65°C to +150°C
T_{LD} Lead Temperature Range
(10 Seconds) . . . . . +300°C
T_C Case Operating Temperature
MSK4900 . . . . . -40°C to +85°C
MSK4900H . . . . . -40°C to +125°C
T_J Junction Temperature . . . . . +150°C

ELECTRICAL SPECIFICATIONS

All Ratings: Tc = +25°C Unless Otherwise Specified

Parameter	Test Conditions ⑧	Group A Subgroup	MSK 4900H			MSK 4900			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Vcc SUPPLY CHARACTERISTICS									
Vcc Voltage		-	14.25	15.00	15.75	14.25	15.00	15.75	V
Vcc Quiescent Current	No PWM	1,2,3	250	300	350	250	300	350	mA
Vcc Operating Current	$C_L = 0.22\mu F$, 20KHz 1 Channel	1,2,3	425	500	575	425	500	575	mA
Vcc Operating Current	$C_L = 0.22\mu F$, 20KHz 2 Channel	1,2,3	550	660	770	550	660	770	mA
INPUT/OUTPUT LOGIC									
Positive Trigger Input Voltage ①		-	2.0	-	-	2.0	-	-	V
Negative Trigger Input Voltage ①		-	-	-	0.8	-	-	0.8	V
Open Collector Ouput - VOL ①	$I_{OL} = 1.5mA$	-	-	0.15	0.4	-	0.15	0.4	V
Open Collector Ouput - IOL ①		-	-	-	1.5	-	-	1.5	mA
OUTPUT CHARACTERISTICS - GATE DRIVE		-							
VOH		1,2,3	15.0	16.25	17.5	15.0	16.25	17.5	V
VOL		1,2,3	-5.75	-5.0	4.4	-5.75	-5.0	4.4	V
IOH ① peak		-	8	-	-	8	-	-	A
IOL ① peak		-	8	-	-	8	-	-	A
Soft Shutdown Time	$C_L = 0.22\mu F$, 20KHz pulse	4,5,6	20	25	30	20	25	30	μS
tplh - Propagation Delay Time		4,5,6	2.5	3.1	4.0	2.5	3.1	4.0	μS
tphl - Propagation Delay Time		4,5,6	2.5	3.1	3.5	2.5	3.1	3.5	μS
tr - Rise Time		4,5,6	0.75	1.25	1.75	0.75	1.25	1.75	μS
tf - Fall Time		4,5,6	0.75	1.25	1.75	0.75	1.25	1.75	μS
td - De-Sat Delay Time		4,5,6	9.5	10.4	11.5	9.5	10.4	11.5	μS
De-Sat Trip Voltage		4,5,6	6.8	7.4	8.5	6.8	7.4	8.5	V
$R_{DS(ON)}$ Xon ① ⑦		-	-	0.44	-	-	0.44	-	Ω
$R_{DS(ON)}$ Xoff ① ⑦		-	-	0.175	-	-	0.175	-	Ω
$R_{DS(ON)}$ SSOX ① ⑦		-	-	0.175	-	-	0.175	-	Ω

NOTES:

① Guaranteed by design but not tested. Typical parameters are representative of actual device performance but are for reference only.
② Industrial grade devices shall be tested to subgroups 1 and 4 unless otherwise specified.
③ Military grade devices ("H" Suffix) shall be 100% tested to Subgroups 1, 2, 3 and 4.
④ Subgroups 5 and 6 testing available upon request.
⑤ Subgroup 1, 4 $T_A = T_C = +25°C$
2, 5 $T_A = T_C = +125°C$
3, 6 $T_A = T_C = -40°C$
⑥ Continuous operation at or above absolute maximum ratings may adversly effect the device performance and/or life cycle.
⑦ X = HI or LO
⑧ All tests performed using MSK 4900 Test Circuit unless otherwise specified.
⑨ When applying power to the device, apply the low voltage followed by the high voltage or alternatively, apply both at the same time. Do not apply high voltage without low voltage present.
⑩ Internal solder reflow temperature is 180°C, do not exceed.

APPLICATION NOTES

MSK 4900 PIN DESCRIPTIONS

VCC1,2 - are the bias supply voltages for supplying the input logic and the power supply for the isolated output. These pins should be bypassed to GND with a 22μF tantalum capacitor and a 0.1μF ceramic capacitor as close to the pins and GNDs as possible. The connected power supply must be able to provide a minimum of 1Amp to satisfy the internal DC-DC converters in rush current at power up. Latch up will occur if the supply current isn't adequate and the device will not function.

GND1,2 - are the Vcc supply returns for the input logic and the internal isolated supply. These GNDs are completely isolated from the output section. No output returns should connect to these GNDs in order to preserve isolation. All Vcc bias supply bypass connections should be made as close to these pins as possible. An input ground plane is the most preferred layout for assuring good, low impedance ground, shielding of inputs from noise, etc.

HI - is the input logic pin for commanding the high-side gate drive to turn on. This logic input is TTL compatible. This input is exclusive OR'd with LO to protect against simultaneous turn on of both the high-side and low-side gate drive. There is no dead-time programmed between HI and LO activation.

LO - is the input logic pin for commanding the low-side gate drive to turn on. This logic input is TTL compatible. This input is exclusive OR'd with HI to protect against simultaneous turn on of both the high-side and low-side gate drive. There is no dead-time programmed between HI and LO activation.

NOTE: X = HI or LO

$\overline{\text{X FAULT}}$ - is an open collector output for indicating a de-saturation condition for the gate drive. This output will be cleared upon activation of $\overline{\text{X FAULT CLEAR}}$.

$\overline{\text{X FAULT CLEAR}}$ - is a logic input pin for clearing a FAULT condition in MANUAL FAULT CLEAR MODE. The mode is determined by the logic level seen on this pin at device power up. To set MANUAL FAULT CLEAR MODE the pin must be held at logic high during power up. To set AUTOMATIC FAULT CLEAR MODE the pin must be at logic low during power up.

In MANUAL MODE a FAULT is cleared by driving the pin to logic low and back to logic high. Allow 30uSec after FAULT before activation of this pin. Once this pin is activated and released (10uSec min.), normal operation will commence.

In AUTOMATIC MODE this pin is ignored and should be connected to ground. After any FAULT occurs it is cleared 150uSec after shutdown completes allowing normal operation to continue.

X ON - is the gate drive output pin for turning the gate on. This pin will source 90mA continuous, 8A peak current. A separate gate resistor shall be selected to tailor the turn-on characteristics. This pin will turn on to +15V.

X OFF - is the gate drive output pin for turning the gate off. This pin will sink 90mA continuous, 8A peak current. A separate gate resistor shall be selected to tailor the turn-off characteristics. This pin will turn off to -5V.

DE-SAT SENSE X - is the input connection for sensing de-saturation. The de-sat voltage is with respect to RETURN X. It is necessary to include a reverse-biased zener diode and a reverse-biased schottky diode between DE-SAT SENSE X and RETURN X, along with 100Ω series resistor and an ultra fast recovery diode (600V) to protect against high voltage at the DE-SAT SENSE X pins. This circuitry will protect against positive voltage spikes greater then the de-saturation voltage, and negative voltage spikes with respect to RETURN X. In many circumstances, PWM switching of other transistors in the power stage can cause switching spikes to inadvertently trip the de-saturation circuitry, causing false FAULTS. This pin (through the protection diode circuit) shall be connected directly to the collector of the IGBT being sensed by a separator wire connection. This pin is blanked during switching so that it will not false trip, and will be blanked internally for 5uSec after gate drive turn-on.

X VDD - is the pin for the floating gate supply voltage. 47μF of bulk capacitance and 0.1μF high frequency capacitance shall be connected between this pin and X VSS as close to the pin as possible. Nominally, this voltage will be +15V with respect to the RETURN X pin and the emitter of the IGBT.

X VSS - is the return pin for the floating gate supply voltage. 47μF of bulk capacitance and 0.1μF high frequency capacitance shall be connected between this pin and X VDD as close to the pins as possible. Nominally, this voltage will be -5V with respect to the RETURN X pin and the emitter.

SSD X - is the soft shutdown pin for slowly turning the gate off after a de-saturation condition. This pin is a separate gate turn-off path and requires a separate gate resistor for this special turn-off approach. The resistor should be sized to keep di/dt from being too high after the de-sat condition. Once de-sat is detected, 25μS of soft shutdown turn-off will occur. After that, soft shutdown will de-activate and X OFF will turn on until $\overline{\text{X FAULT CLEAR}}$ is activated and released.

RETURN X - is the pin for the emitter reference to the IGBT being driven. This pin will be at zero volts to +15V to -5V for the gate drive voltage. This pin shall include the de-sat diode circuitry and shall be connected directly to the emitter of the IGBT by a separate wire connection.

NOTE:

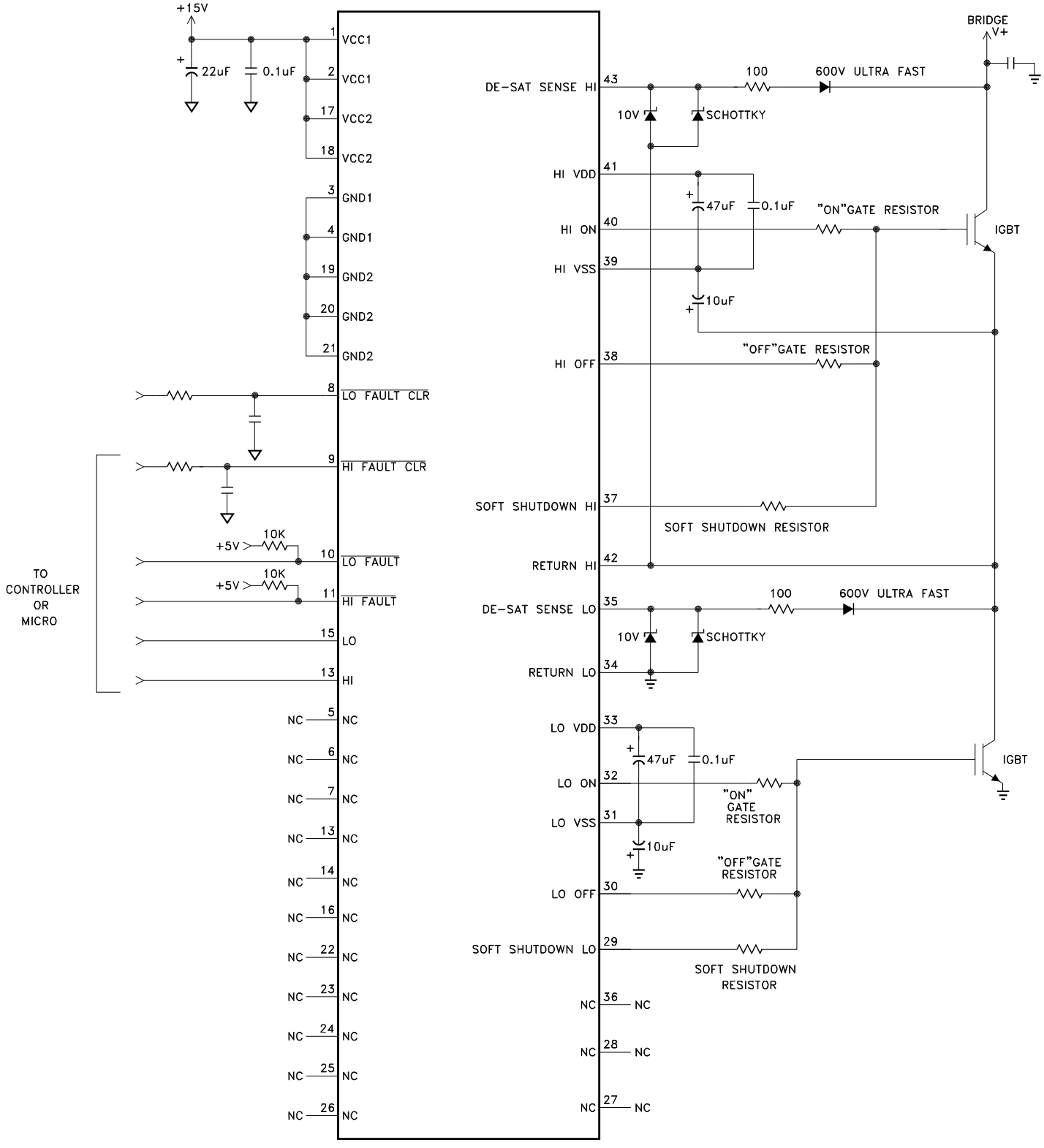
TP PINS 5,6,7,13,14 - are for factory use only. They are used during manufacturing for programming and test purposes only. Leave these pins unconnected.

OPERATION

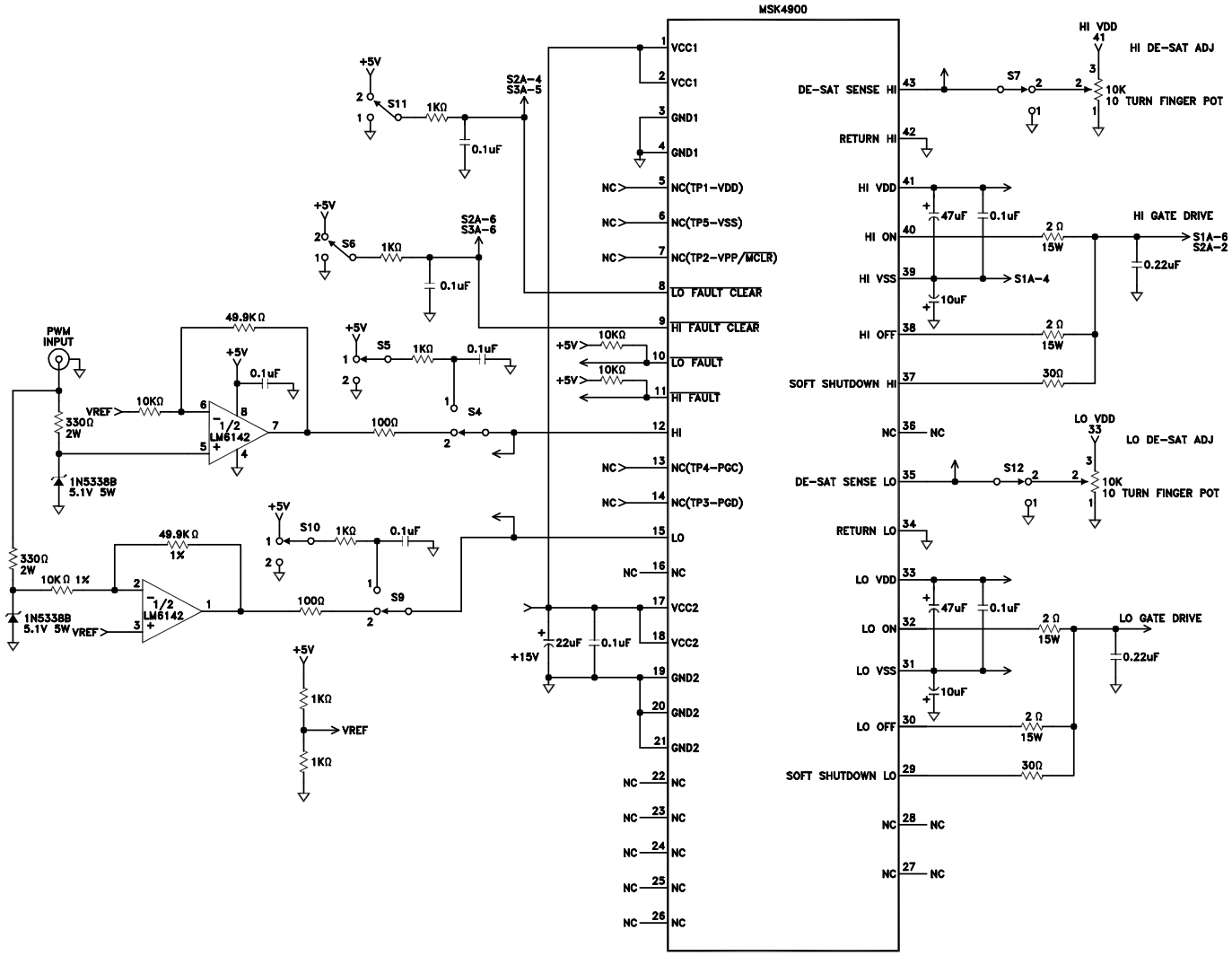
+15V must be applied at least 65mSec before the system high voltage is applied. The internal processor will be initialized 64mSec after +15V. During the 64mSec, HI, LO must be pulled logic low and $\overline{\text{X FAULT CLEAR}}$ must be held logic high to select MANUAL FAULT CLEAR MODE or held logic low to select AUTOMATIC FAULT CLEAR MODE. Once HI/LO is pulled logic high, Hi or LO (respectively) gate drive will turn on, providing +15V gate drive to the IGBT. De-saturation sensing will be blanked for 5μSec to allow switching transients to settle. After 5μSec, DE-SAT SENSE X will be active. If de-saturation occurs, an additional delay of 5uSec due to a digital noise filter function occurs then the X HI or X LO gate drive will turn off and soft shutdown - SSD X will turn-on, slowly turning the offending IGBT off to avoid excessive dv/dt and di/dt during this time. $\overline{\text{X FAULT}}$ output will also be triggered, telling the system that a de-sat shutdown occured. Soft shutdown will continue for 25μSec, after which SSD X pin will turn off and the normal X OFF pin turn on, holding the IGBT gate off until $\overline{\text{X FAULT CLEAR}}$ gets cycled low then high by the system if MANUAL FAULT CLEAR MODE has been selected or for a period of 150uSec if AUTOMATIC FAULT CLEAR MODE has been selected. Once cleared, normal operation will begin again. HI and LO will turn on and off their approprate IGBT's, but will not turn them on simultaneously. The processor exclusive OR's the inputs to prevent this condition. One input is not master of the other. If both are ON, the processor will shut both off until the condition is removed. There is no built in dead-time between HI and LO. It is up to the system to provide adequate dead-time to prevent IGBT shoot-through.

The minimum HI and LO pulse width is 1.5μSec. This is for both duty cycles approaching 0% and approaching 100% due to program propagation time. This means that any pulse input to HI and LO pins will be interpreted as a 1.5μSec pulse until the actual input pulse width extends past 1.5μSec or 0% duty cycle is reached. For duty cycles approaching 100%, any pulse high going low with a width of less than 1.5μSec will be interpreted as 1.5μSec going low pulse until the pulse width going low becomes greater than 1.5μSec, or 100% duty cycle is reached.

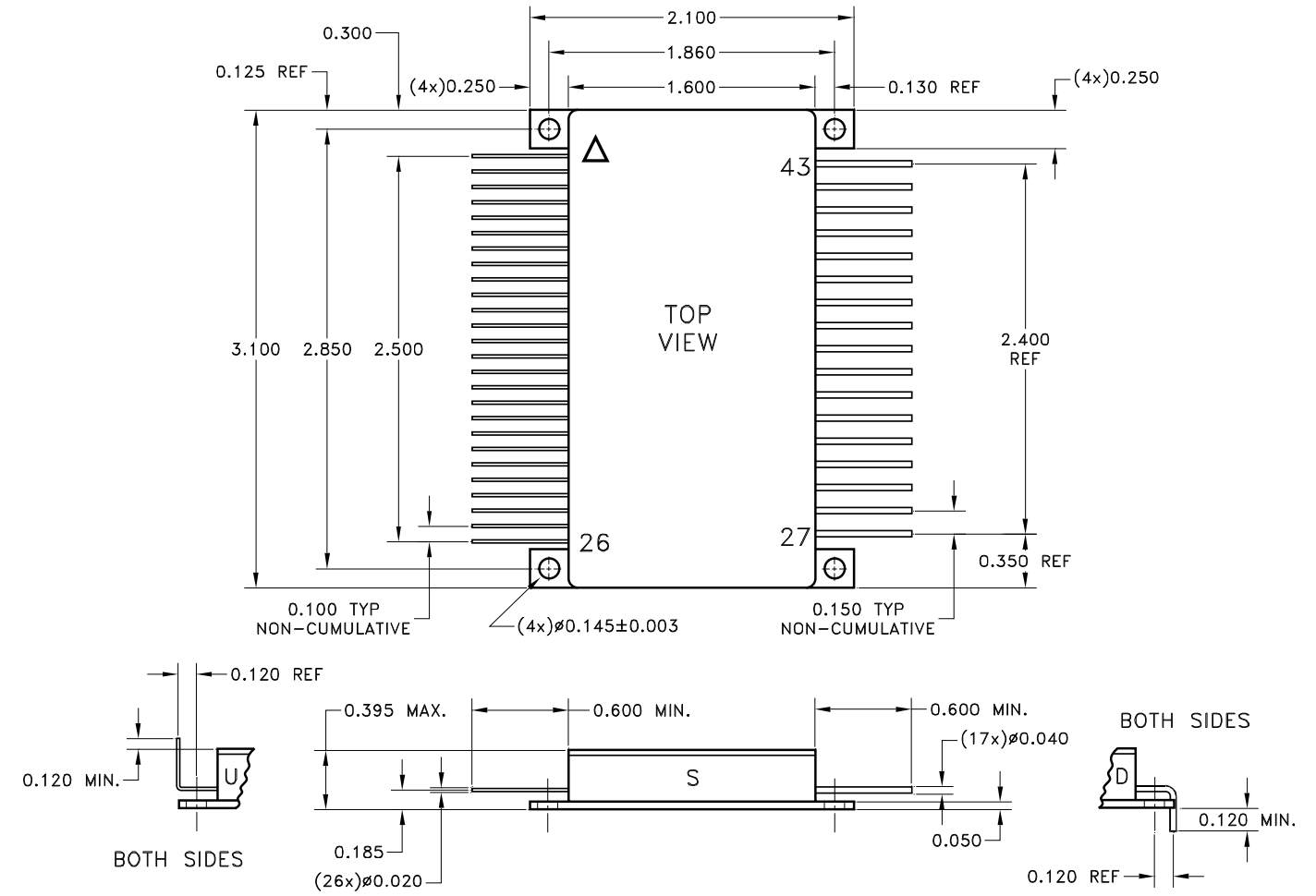
TYPICAL APPLICATION



MSK4900 TEST CIRCUIT



MECHANICAL SPECIFICATIONS



NOTE: ALL DIMENSIONS ARE ±0.010 INCHES UNLESS OTHERWISE LABELED.
ESD Triangle indicates Pin 1.

ORDERING INFORMATION

MSK4900 H U

LEAD CONFIGURATION
S = STRAIGHT, U = BENT UP, D = BENT DOWN

SCREENING
BLANK = INDUSTRIAL; H = MIL-PRF-38534 CLASS H

GENERAL PART NUMBER

THE ABOVE EXAMPLE IS A MILITARY GRADE HYBRID WITH LEADS BENT UP.

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