SI9FL064/032A MirrorBit® ROM

(Serial Peripheral Interface)
64 Megabit and 32 Megabit CMOS 3.0 Volt MirrorBit® ROM with 50 Mhz SPI Bus Interface

Data Sheet

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S19FL064/32A MirrorBit® ROM
(Serial Peripheral Interface)
64 Megabit and 32 Megabit CMOS 3.0 Volt MirrorBit® ROM with 50 Mhz SPI Bus Interface

Data Sheet

General Description

The S19FL-A device is a 3.0 Volt (2.7V to 3.6V) single power supply Serial Peripheral Interface (SPI) read-only memory device. The device is manufactured using 200 nm MirrorBit Technology.

Distinctive Characteristics

Architectural Advantages

- **Single power supply operation**
  - Full voltage range: 2.7 to 3.6V
- **SPI Bus Compatible Serial Interface**
- **Process Technology**
  - Manufactured on 200 nm MirrorBit process technology
- **Package Option**
  - 16-pin SO package (300 mils)

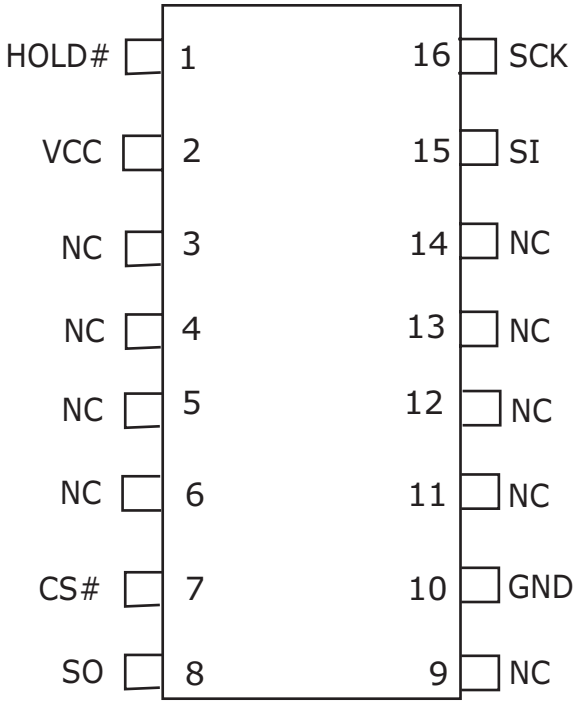
Performance Characteristics

- **Speed**
  - 50 MHz clock rate (maximum)
- **Power Saving Standby Mode**
  - Standby Mode 50 µA (max)
  - Deep Power Down Mode 1.3 µA (typical)

Table of Contents

Connection Diagrams

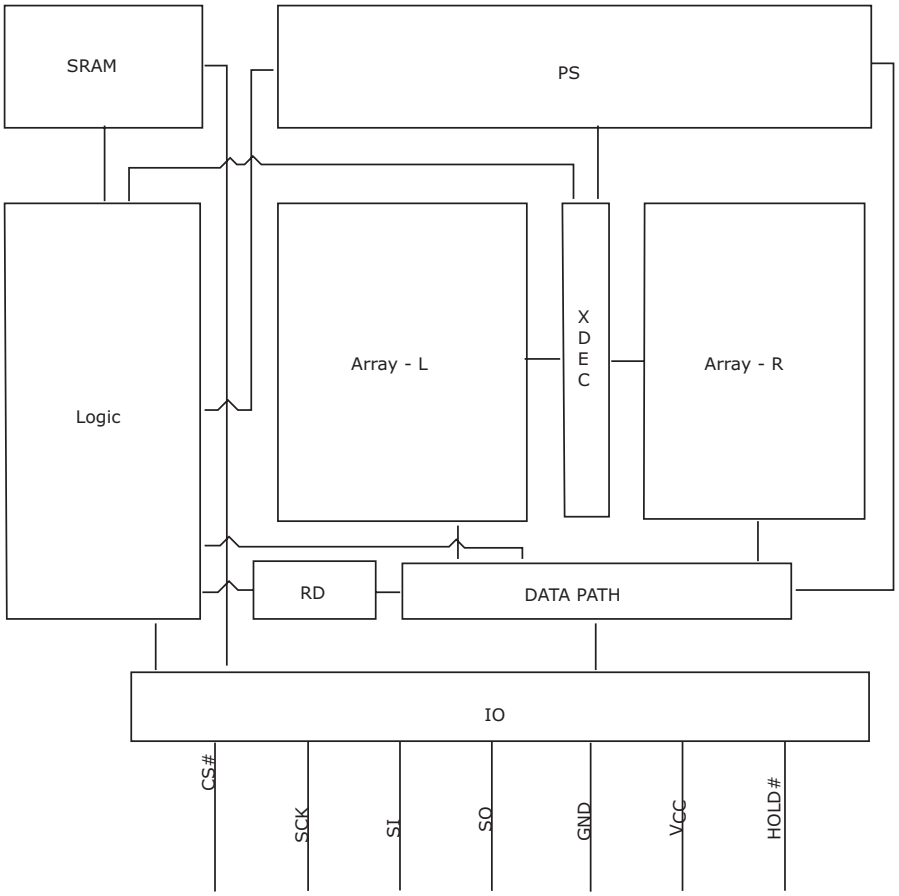
16-pin Plastic Small Outline Package (SO)



Input/Output Descriptions

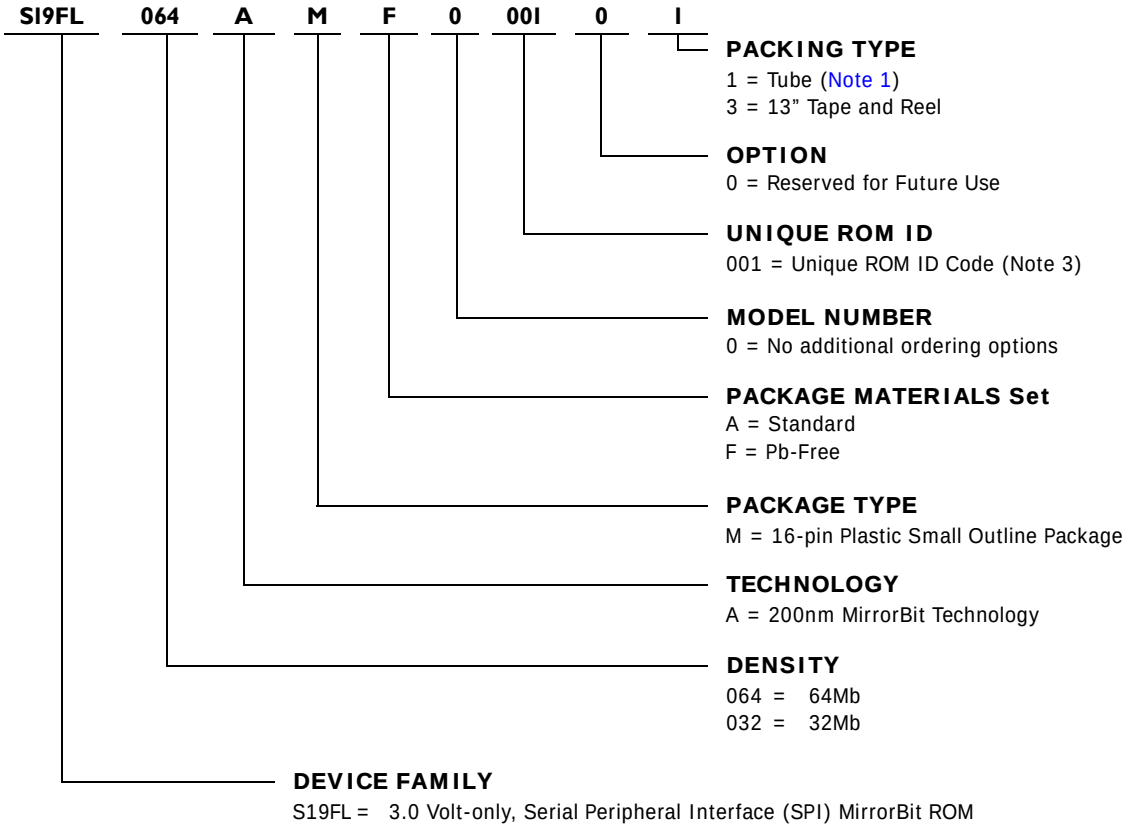
Symbol	Type	Description
SCK	Clock	Serial Clock Input: This input signal provides the timing of the serial interface. Instructions and addresses present at the Serial Data input (SI) are latched on the rising edge of Serial Clock (SCK). Data on Serial Data Output (SO) changes after the falling edge of Serial Clock (SCK).
SI	Input	Serial Data Input: This input signal is used to transfer instructions and address serially into the device. Values are latched on the rising edge of Serial Clock (SCK).
SO	Output	Serial Data Output: This input signal is used to transfer data serially out of the device. Data is shifted out on the falling edge of Serial Clock (SCK)
CS#	Input	Chip Select Input: When this input signal is High, the device is deselected, Serial Data Output (SO) is at high impedance and the device is in Standby mode. Driving Chip Select (CS#) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select (CS#) is required prior to the start of any instruction.
HOLD#	Input	Hold Input: This signal is used to pause any serial communications with the device without deselecting the device. During the Hold instruction, the Serial Data Output (SO) is high impedance and Serial Data Input (SI) and Serial Clock (SCK) are Don't Care. To start the Hold condition, the device must be selected, with Chip Select (CS#) driven Low.
VCC	Supply	Supply Voltage Input
GND	Ground	Ground Input

Block Diagram



Ordering Information

Standard products are available in several package. The ordering part number is formed by a valid combination of the following:



Note: *All S19FL-A devices are offered over the industrial temperature (-40°C to 85°C) range and 50Mhz maximum clock rate.*

S19FL-A Valid Combinations					
Base Ordering Part Number	**Package & Material**	**Model Number**	**Unique ROM ID**	**Option**	**Packing Type**
S19FL032A	MA, MF (Note 2)	0	XXX (Note 3)	0	1, 3 (Note 1)
S19FL064A	MA, MF (Note 2)	0	XXX (Note 3)	0	1, 3 (Note 1)

Notes:

1. *Type 1 is standard. Specify other options as required.*
2. *Contact your local sales office for availability.*
3. *Unique ROM ID is assigned by the factory.*

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device.

SPI Modes

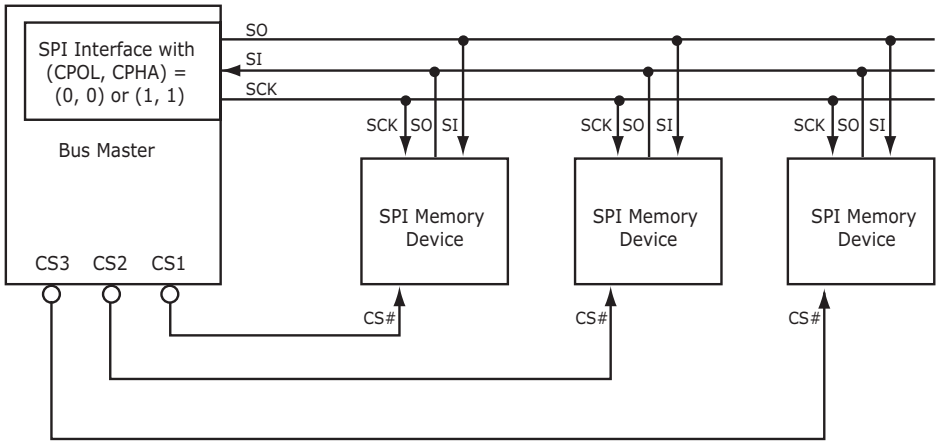
These devices can be driven by a microcontroller with its SPI peripheral running in either of the two following modes:

- CPOL = 0, CPHA = 0
- CPOL = 1, CPHA = 1

For these two modes, input data is latched in on the rising edge of Serial Clock (SCK), and output data is available from the falling edge of Serial Clock (SCK).

The difference between the two modes, as shown in Figure 2, is the clock polarity when the bus master is in Standby and not transferring data:

- SCK remains at 0 for (CPOL = 0, CPHA = 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1)



Note: The Hold (HOLD#) signal should be driven High or Low as appropriate.

Figure 1. Bus Master and Memory Devices on the SPI Bus

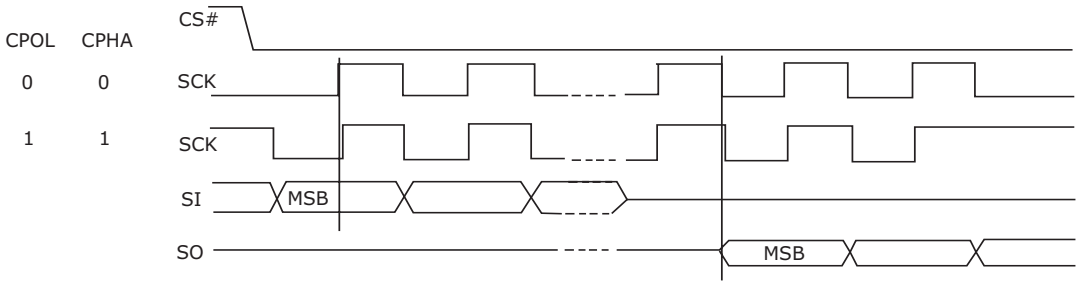


Figure 2. SPI Modes Supported

Operation Features

Hold Condition Modes

The Hold (HOLD#) signal is used to pause any serial communications with the device without resetting the clocking sequence. The HOLD# signal gates the clock input to the device.

To enter the Hold condition, the device must be selected, with Chip Select (CS#) low. The Hold condition starts on the falling edge of the HOLD# signal, provided that this coincides with Serial Clock (SCK) being low (as shown in Figure 3).

The Hold condition ends on the rising edge of the HOLD# signal, provided that this coincides with Serial Clock being low.

If the falling edge does not coincide withe Serial Clock being low, the Hold condition starts after Serial Clock next goes low. Similarly, if the rising edge does not coincide with Serial Clock being low, the Hold condition ends after Serial Clock next goes low. During the Hold condition, the Serial Data Output (SO) is high impedance and Serial Data Input (SI) and Serial Clock are Don't Care.

Normally, the device remains selected, with Chip Select driven low, for the entire duration of the Hold condition.

If Chip Select goes High while the device is in the Hold condition, this has the effect of resetting the internal logic of the device. To restart communication with the device, it is necessary to drive HOLD# high and then drive Chip Select low. This prevents the device from going back to the Hold condition.

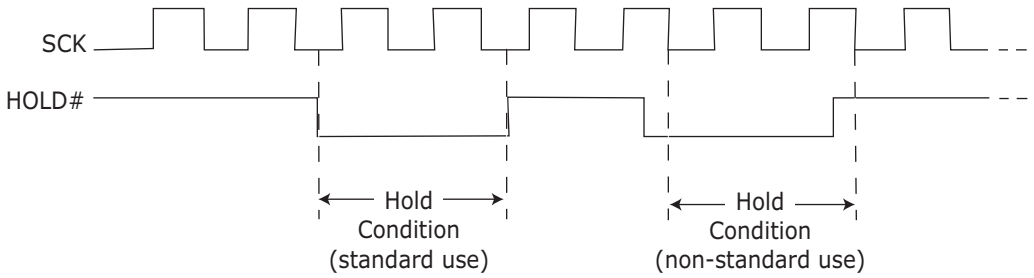


Figure 3. Hold Condition Activation

Instructions

All instructions, addresses, and data are shifted in and out of the device, starting with the most significant bit. Serial Data Input (SI) is sampled on the first rising edge of Serial Clock (SCK) after Chip Select (CS#) is driven Low. Then, the one-byte instruction code must be shifted in to the device, most significant bit first, on Serial Data Input (SI), each bit being latched on the rising edges of Serial Clock (SCK). The instruction set is listed in Table 1, on page 8.

Every instruction sequence starts with a one-byte instruction code. Chip Select (CS#) must be driven High after the last bit of the instruction sequence is shifted in.

For Read Data Bytes (READ), and Read Data Bytes at higher speed (FAST_READ) instructions, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven High after any bit of the data-out sequence is being shifted out to terminate the transaction.

Table I. Instruction Set

Instruction	Description	One-Byte Instruction Code	Address Bytes	Dummy Byte	Data Bytes
Read Operations					
READ	Read Data Bytes	03H (0000 0011)	3	0	1 to Infinity
FAST_READ	Read Data Bytes at Higher Speed	0BH (0000 1011)	3	1	1 to Infinity
RDID	Read Identification	9FH (1001 1111)	0	0	1 to 3
Deep Power Down Savings Mode Operations					
DP	Deep Power Down	B9H (1011 1001)	0	0	0
RES	Release from Deep Power Down	ABH (1010 1011)	0	0	0
	Release from Deep Power Down and Read Electronic Signature	ABH (1010 1011)	0	3	1 to Infinity

Read Data Bytes (READ)

The READ instruction reads the memory at the specified SCK frequency (f_{SCK}) with a maximum speed of 33Mhz for the S19FL032A, and 25MHz for the S19FL064A.

The device is first selected by driving Chip Select (CS#) Low. The instruction code for the Read Data Bytes (READ) instruction is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a frequency f_{SCK}, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 4. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The Read Data Bytes (READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output.

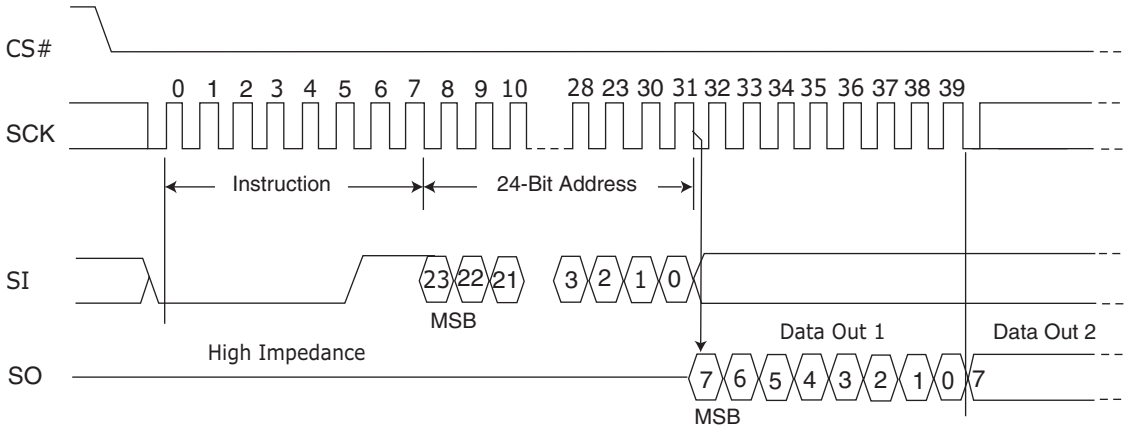


Figure 4. Read Data Bytes (READ) Instruction Sequence

Read Data Bytes at Higher Speed (FAST_READ)

The FAST_READ instruction reads the memory at the specified SCK frequency (f_{SCK}) with a maximum speed of 50 MHz. The device is first selected by driving Chip Select (CS#) Low. The instruction code for (FAST_READ) instruction is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of Serial Clock (SCK). Then the memory contents, at that address, are shifted out on Serial Data Output (SO), each bit being shifted out, at a maximum frequency F_{SCK}, during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 5. The first byte addressed can be at any location. The address automatically increments to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single (FAST_READ) instruction. When the highest address is reached, the address counter rolls over to 00000h, allowing the read sequence to be continued indefinitely.

The (FAST_READ) instruction is terminated by driving Chip Select (CS#) High. Chip Select (CS#) can be driven High at any time during data output.

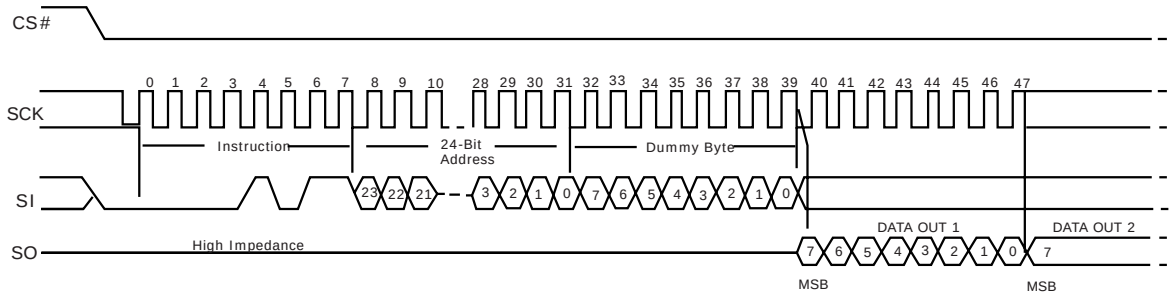


Figure 5. Read Data Bytes at Higher Speed (FAST_READ) Instruction Sequence

Read Identification (RDID)

The Read Identification (RDID) instruction allows the 8-bit manufacturer identification to be read, followed by two bytes of the device identification.

The manufacturer identification byte is assigned by JEDEC, and has a value of 01h for Spansion™ products. The device identification is assigned by the device manufacturer and indicates the memory type in the first byte and the memory capacity of the device in the second byte.

The device is first selected by driving Chip Select (CS#) low. Then, the 8-bit instruction code for the instruction is shifted in, with each bit being latched in on SI during the rising edge of SCK. This is followed by the 24-bit device identification, stored in the memory, being shifted out on Serial Data Output (SO), with each bit being shifted out during the falling edge of Serial Clock.

The instruction sequence is shown in Figure 6, on page 10.

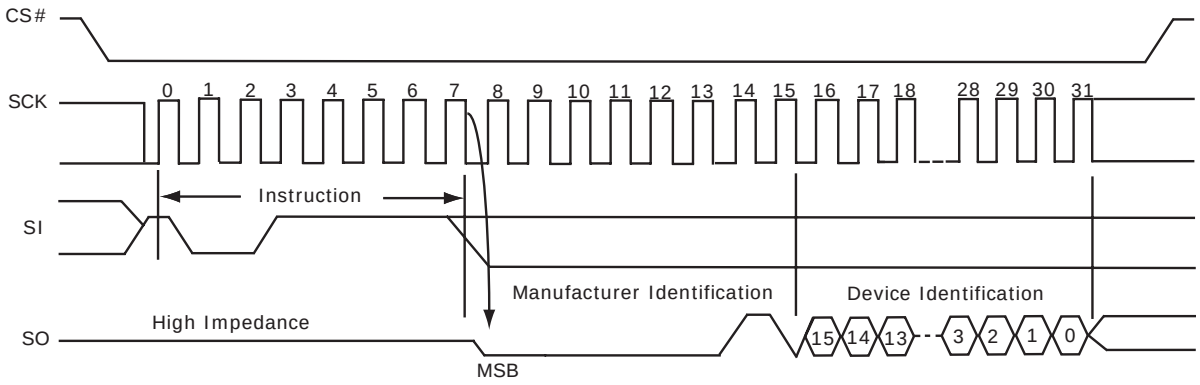


Figure 6. Read Identification (RDID) Instruction Sequence and Data-Out Sequence

Driving CS# high after the Device Identification is read at least once, terminates the READ_ID instruction. The Read Identification (RDID) instruction can also be terminated by driving CD# high at any time during data output.

When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode, and execute instructions.

Table 2. Read Identification (RDID) Data-Out Sequence

Device	Manufacturer Identification	Device Identification	
		Memory Type	Memory Capacity
S19FL032A	01h	02h	015h
S19FL064A	01h	02h	016h

Deep Power Down (DP)

The Deep Power Down (DP) instruction places the device in the lowest current mode of 1.3 µA typical.

The Deep Power Down (DP) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 7, on page 11.

Driving Chip Select (CS#) High after the eighth bit of the instruction code is latched places the device in Deep Power Down mode. The Deep Power Down mode can only be entered by executing the Deep Power Down (DP) instruction to reduce the standby current (from I_{SB} to I_{DP} as specified in Table 5, on page 16). As soon as Chip Select (CS#) is driven high, it requires a delay of t_{DP} currently in progress before Deep Power Down mode is entered.

Once the device enters the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES). This releases the device from the Deep Power Down mode.

The Deep Power Down mode automatically stops at Power-down, and the device always powers up in the Standby mode.

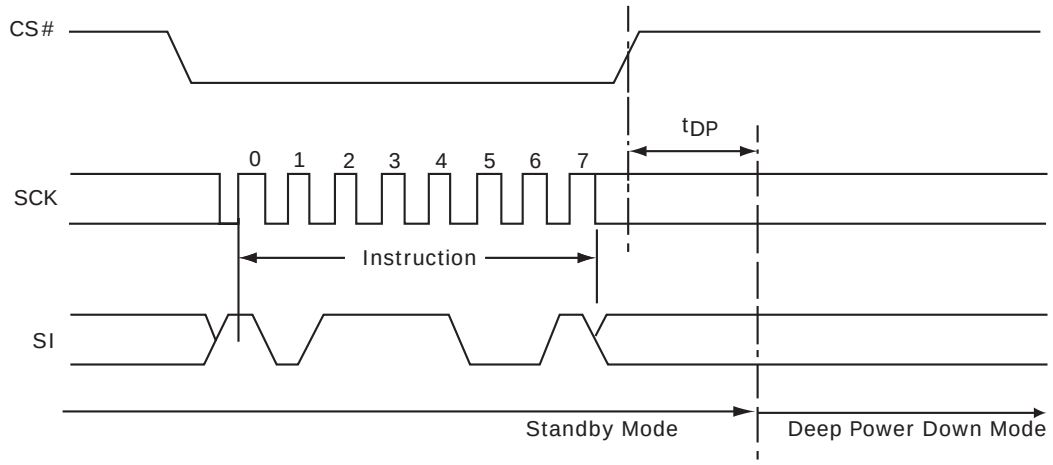


Figure 7. Deep Power Down (DP) Instruction Sequence

Release from Deep Power Down (RES)

The Release from Deep Power Down (RES) instruction provides the only way to exit the Deep Power Down mode. Once the device enters the Deep Power Down mode, all instructions are ignored except the Release from Deep Power Down (RES) instruction. Executing this instruction takes the device out of Deep Power Down mode.

The Release from Deep Power Down (RES) instruction is entered by driving Chip Select (CS#) Low, followed by the instruction code on Serial Data Input (SI). Chip Select (CS#) must be driven Low for the entire duration of the sequence.

The instruction sequence is shown in Figure 8, on page 12.

Driving Chip Select (CS#) High after the 8-bit instruction byte is received by the device, but before the whole of the 80bit Electronic Signature is transmitted for the first time, still ensures that the device is placed into Stand-by mode. If the device was previously in the Deep Power Down mode, though, the transition to the Stand-by Power mode is delayed by t_{RES}, and Chip Select (CS#) must remain High for at least $t_{RES(max)}$, as specified in Table 7, on page 18. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode and execute instructions.

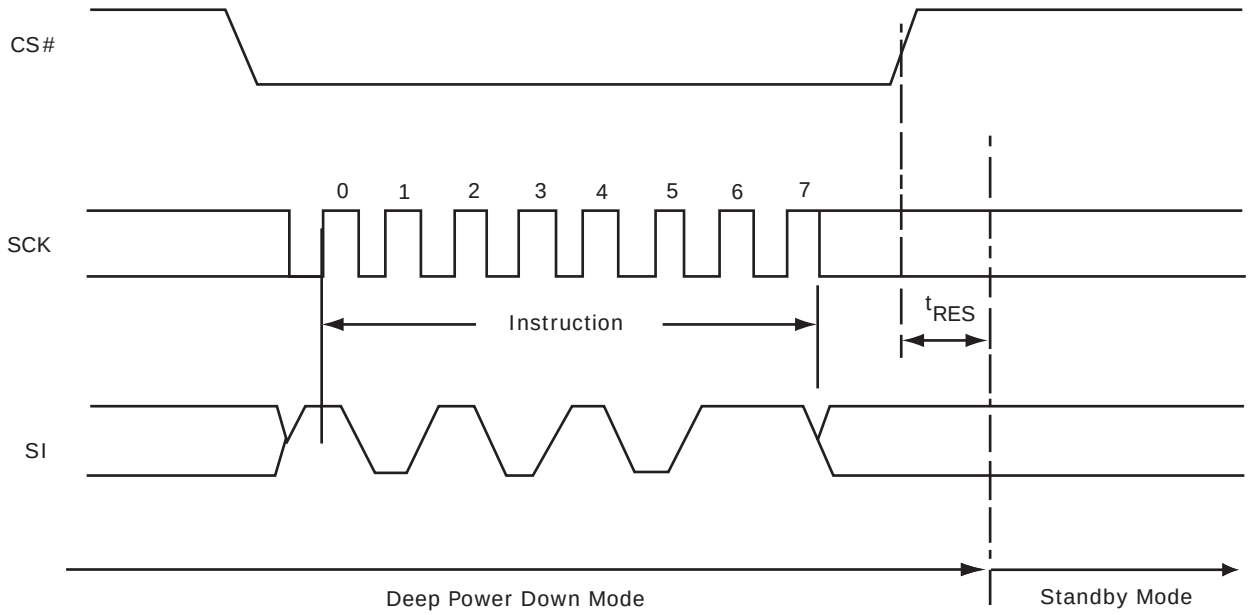


Figure 8. Release from Deep Power Down Instruction Sequence

Release from Deep Power Down and Read Electronic Signature (RES)

Once the device enters Deep Power Down mode, all instructions are ignored except the RES instruction. The RES instruction can also be used to read the old-style 8-bit Electronic Signature of the device on the SO pin. The RES instruction always provides access to the device's Electronic Signature and can be applied even if DP mode was not entered.

The device features an 8-bit Electronic Signature, whose value for the S19FL064A is 16h and the S19FL032A is 15h. This can be read using the RES instruction.

The device is first selected by driving Chip Select (CS#) low. The instruction code is followed by three dummy bytes, each bit being latched-in on Serial Data Input (SI) during the rising edge of Serial Clock (SCK). Then, the 8-bit Electronic Signature stored in memory, is shifted out of Serial Data Output (SO), each bit being shifted out during the falling edge of Serial Clock (SCK).

The instruction sequence is shown in Figure 9, on page 13.

The Release from Deep Power Down and Read Electronic Signature (RES) is terminated by driving Chip Select (CS#) high after the Electronic Signature is red at least once. Sending additional clock cycles on Serial Clock (SCK) while Chip Select (CS#) is driven low, causes the Electronic Signature to be output repeatedly.

When Chip Select (CS#) is driven high, the device is put in the Stand-by Power mode. If the device was not previously in the Deep Power Down mode, the transition to the Stand-by Power mode is immediate. If the device was previously in the Deep Poser Down mode, the transition to the Stand-by mode is delayed by t_{RSE} and Chip Select (CS#) must remain high for at least $t_{RES(max)}$, as specified in Table 7, on page 18. Once in the Stand-by Power mode, the device waits to be selected, so that it can receive, decode, and execute insturctions.

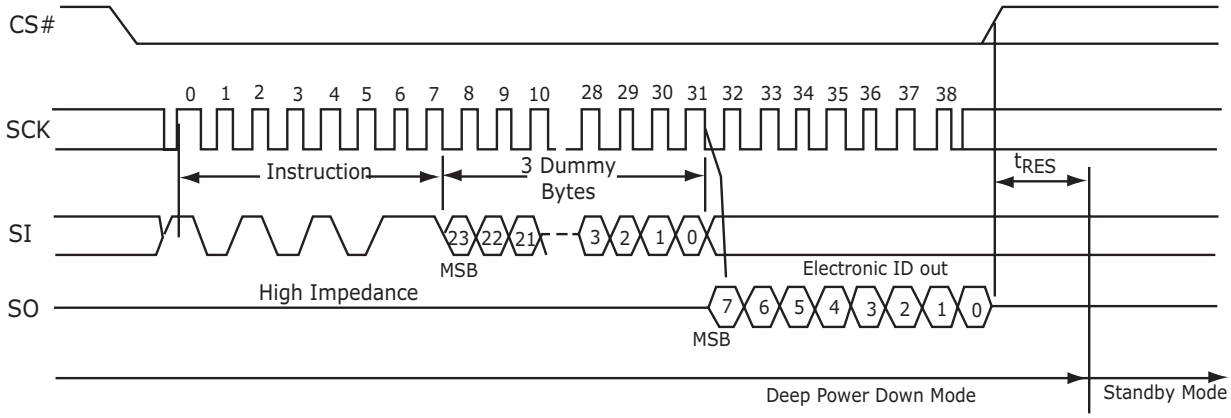


Figure 9. Release from Deep Power Down and Read Electronic Signature (RES) Instruction Sequence

Power-up and Power-down

The device must not be selected at power-up or power-down (that is, CS# must follow the voltage applied on V_{CC}) until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power-up, and then for a further delay of t_{PU} (Table 3)
- V_{SS} at power-down

A simple pull-up resistor on Chip Select (CS#) can usually be used to ensure safe and proper power-up and power-down.

The device ignores all instructions until a time delay of t_{PU} (Table 3) has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold. However, correct operation of the device is not guaranteed if by this time V_{CC} is still below V_{CC} (min).

At power-up, the device is in Standby mode (not Deep Power Down mode).

Normal precautions must be taken for supply rail decoupling to stabilize the V_{CC} feed. Each device in a system should have the V_{CC} rail decoupled by a suitable capacitor close to the package pins (this capacitor is generally of the order of 0.1 µF).

At power-down, when V_{CC} drops from the operating voltage to below the minimum V_{CC} threshold, all operations are disabled and the device does not respond to any instructions.

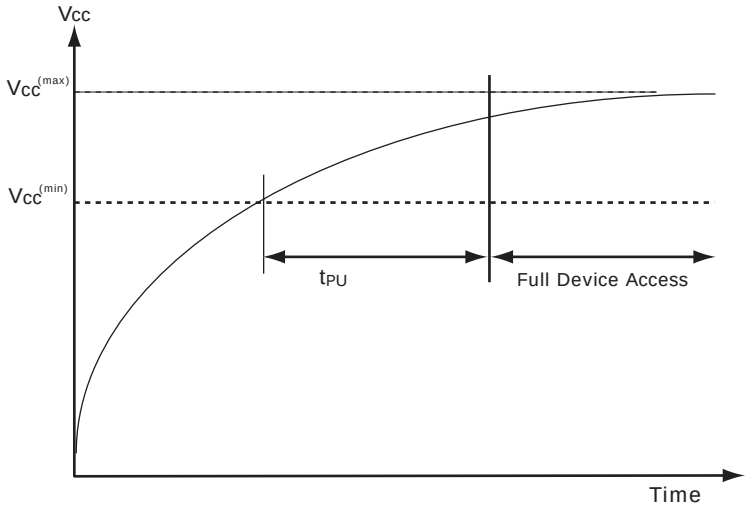


Figure 10. Power-Up Timing

Table 3. Power-Up Timing

Symbol	Parameter	Min	Max	Unit
$V_{CC(min)}$	V_{CC} (minimum)	2.7		V
t_{PU}	V_{CC} (min) to device operation	10		ms

Absolute Maximum Ratings

Stressing the device above the rating listed in the **Absolute Maximum Ratings** section below may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Ambient Storage Temperature . . . . . –65°C to +150°C

Voltage with Respect to Ground:

All Inputs and I/Os. . . . . –0.3 V to 4.5 V

Operating Ranges

Ambient Operating Temperature (T_A)

Industrial . . . . . –40°C to +85°C

Positive Power Supply

Voltage Range . . . . . 2.7 V to 3.6 V

Note: *Operating ranges define those limits between which functionality of the device is guaranteed.*

DC Characteristics

This section summarizes the DC and AC Characteristics of the device. Designers should check that the operating conditions in their circuit match the measurement conditions specified in the Test Specifications in Table 6, when relying on the quoted parameters.

Table 4. SI9FL032A DC Characteristics—CMOS Compatible

Parameter	Description	Test Conditions (See Note)		Min	Typ.	Max	Unit
V_{CC}	Supply Voltage			2.7	3	3.6	V
I_{CC1}	Active Read Current	SCK = 0.1 V_{CC}/0.9V_{CC}	33 MHz			12	mA
		SCK = 0.1 V_{CC}/0.9V_{CC}	V_{CC} = 3.0V 50 MHz			19	mA
I_{SB}	Standby Current	V_{CC} = 3.0 V CS# = V_{CC}			20	50	µA
I_{DP}	Deep Power Down Current	V_{CC} = 3.0 V CS# = V_{CC}			1.5	5	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}				1	µA
V_{IL}	Input Low Voltage			–0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = $V_{CC\ min}$				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA		V_{CC} – 0.2			V

Note: *Typical values are at TA = 25°C and 3.0 V.*

Table 5. SI9FL064A DC Characteristics—CMOS Compatible

Parameter	Description	Test Conditions (See Note)		Min	Typ.	Max	Unit
V_{CC}	Supply Voltage			2.7	3	3.6	V
I_{CC1}	Active Read Current	SCK = 0.1 V_{CC}/0.9V_{CC}	25 MHz		8	10	mA
		SCK = 0.1 V_{CC}/0.9V_{CC}	V_{CC} = 3.0V 50 MHz		14	19	mA
I_{SB}	Standby Current	V_{CC} = 3.0 V CS# = V_{CC}				50	µA
I_{DP}	Deep Power Down Current	V_{CC} = 3.0 V CS# = V_{CC}			1.3	5	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}				1	µA
I_{LO}	Output Leakage Current	V_{IN} = GND to V_{CC}				1	µA
V_{IL}	Input Low Voltage			–0.3		0.3 V_{CC}	V
V_{IH}	Input High Voltage			0.7 V_{CC}		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA, V_{CC} = $V_{CC\ min}$				0.4	V
V_{OH}	Output High Voltage	I_{OH} = –0.1 mA		V_{CC} – 0.2			V

Note: *Typical values are at T_A = 25°C and 3.0 V.*

Test Conditions

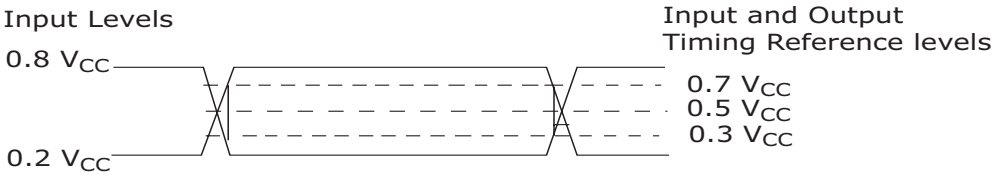


Figure II. AC Measurements I/O Waveform

Table 6. Test Specifications

Symbol	Parameter	Min	Max	Unit
C_L	Load Capacitance	30		pF
	Input Rise and Fall Times		5	ns
	Input Pulse Voltage	0.2 V_{CC} to 0.8 V_{CC}		V
	Input Timing Reference Voltage	0.3 V_{CC} to 0.7 V_{CC}		V
	Output Timing Reference Voltage	0.5 V_{CC}		V

AC Characteristics

Table 7. AC Characteristics

Symbol (Note 1)	Parameter	Min	Typ (Note 1)	Max (Note 1)	Unit
F_{SCK}	SCK Clock Frequency READ instruction	D.C.		33 (S19FL064A), 25 (S19FL064A)	MHz
F_{SCK}	SCK Clock Frequency for: FAST_READ, DP, RES,	D.C.		50	MHz
t_{CRT}	Clock Rise Time (Slew Rate)	0.1			V/ns
t_{CFT}	Clock Fall Time (Slew Rate)	0.1			V/ns
t_{WH}	SCK High Time	9			ns
t_{WL}	SCK Low Time	9			
t_{CS}	CS# High Time	100			
t_{CSS} (1)	CS# Setup Time	5			
t_{CSH} (1)	CS# HOLD Time	5			
t_{HD} (1)	HOLD# Setup Time (relative to SCK)	5			
t_{CD} (1)	HOLD# Hold Time (relative to SCK)	5			
t_{HC}	HOLD# Setup Time (relative to SCK)	5			
t_{CH}	HOLD# Hold Time (relative to SCK)	5			
t_{V}	Output Valid	0		10	
t_{HO}	Output Hold Time	0			
$t_{HD:DAT}$	Data in Hold Time	5			
$t_{SU:DAT}$	Data in Setup Time	5			
t_{R}	Input Rise Time			5	
t_{F}	Input Fall Time			5	
t_{LZ} (1)	HOLD# to Output Low Z			10	
t_{HZ} (1)	HOLD# to Output High Z			10	
t_{DIS} (1)	Output Disable Time			10	
t_{DP}	CS# High to Deep Power Down Mode			3	µs
t_{RES}	Release DP Mode			30	µs

Notes:

1. Not 100% tested.

AC Characteristics

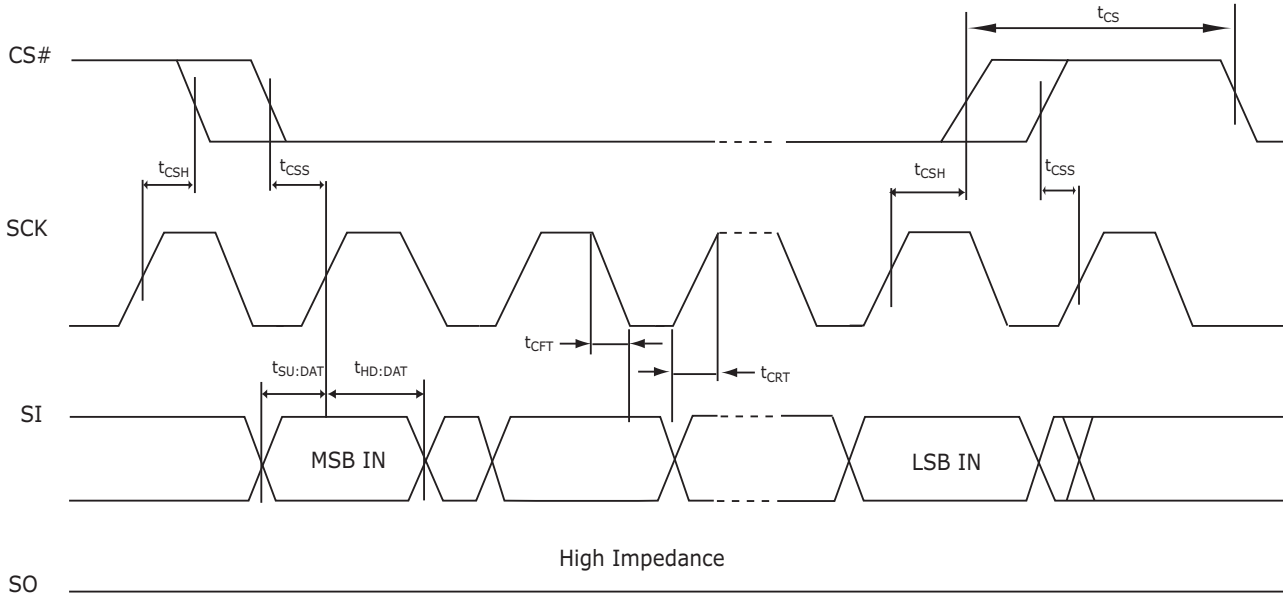


Figure 12. SPI Mode 0 (0,0) Input Timing

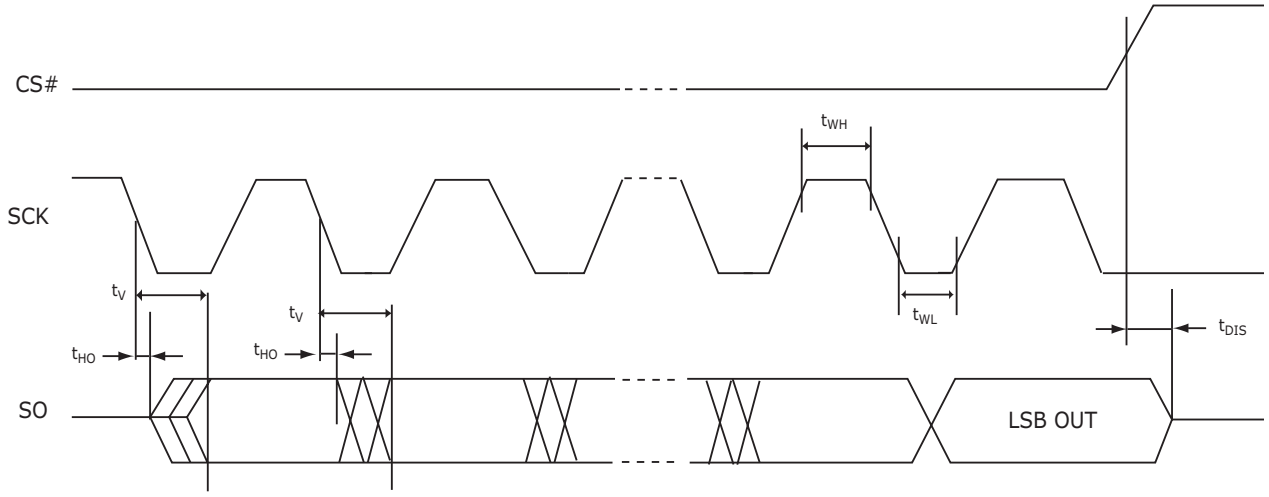


Figure 13. SPI Mode 0 (0,0) Output Timing

AC Characteristics

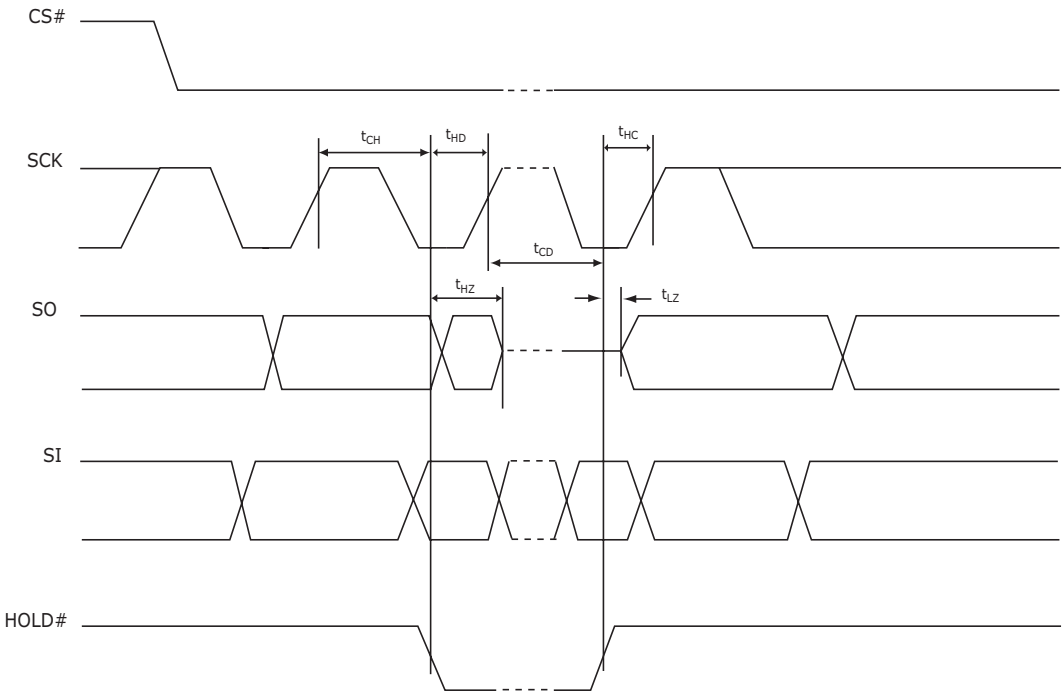
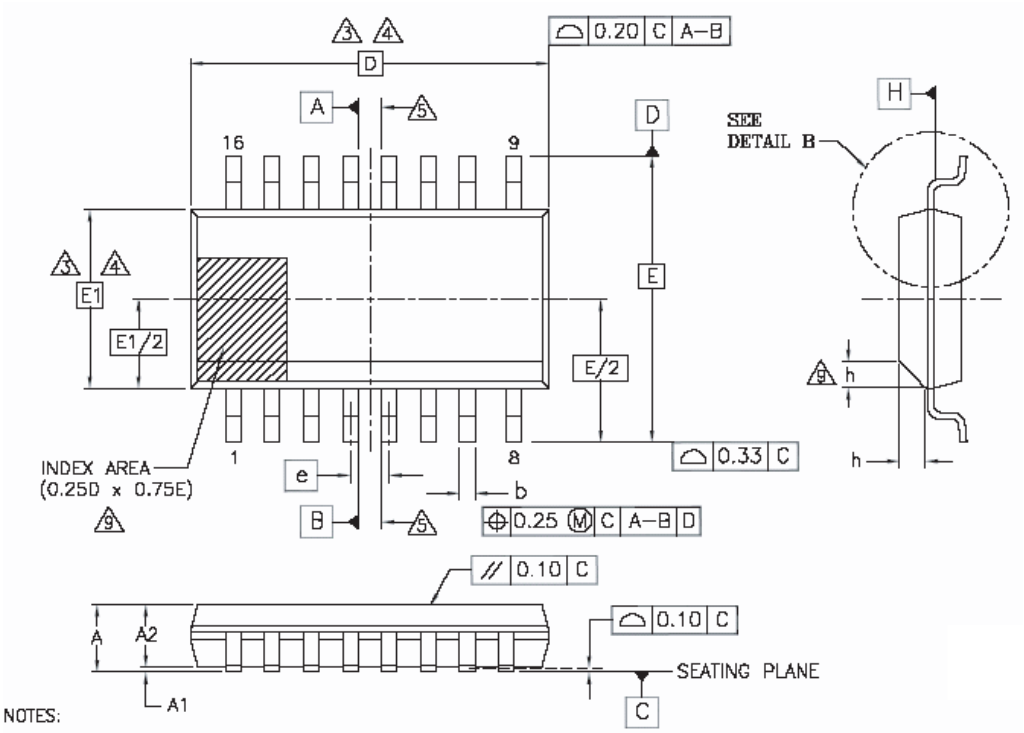


Figure 14. HOLD# Timing

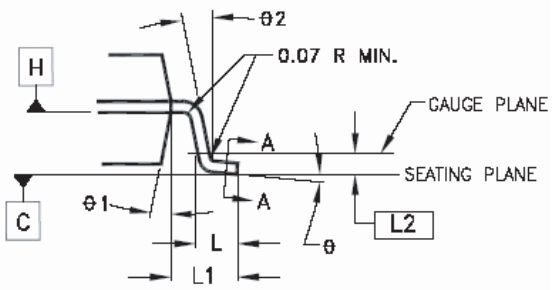
Physical Dimensions

S016 Wide—16-pin Plastic Small Outline 300 mils Body Width Package



NOTES:

PACKAGE	xSO3 016(INCHES)		xSO3 016(MM)	
JEDEC	MS-013<D>AA		MS-013<D>AA	
SYMBOL	MIN	MAX	MIN	MAX
A	.093	.104	2.35	2.65
A1	.004	.012	0.10	0.30
A2	.081	.104	2.05	2.55
b	.012	.020	0.31	0.51
b1	.011	.019	0.27	0.48
c	.008	.013	0.20	0.33
c1	.008	.012	0.20	0.30
D	.406 BSC		10.30 BSC	
E	.406 BSC		10.30 BSC	
E1	.295 BSC		7.50 BSC	
e	.050 BSC		1.27 BSC	
L	.016	.050	0.40	1.27
L1	.055 REF		1.40 REF	
L2	.010 BSC		0.25 BSC	
N	16		16	
h	0.10	0.30	0.25	0.75
θ	0°	8°	0°	8°
θ1	5°	15°	5°	15°
θ2	0°		0°	



Revision Summary

Revision A0 (March 8, 2005)

Initial Release.

Revision AI (March 9, 2005)

Deleted 8-pin WSON package.

Changed fSCK from 33 to 25 MHz.

Revision A2 (June I5, 2005)

Added HOLD# signal information in the following sections:

Connection Diagram.

Input/Output Descriptions.

Block Diagram.

SPI Mode

Updated Bus Master and Memory Devices on the SPI Bus diagram.

Added note.

Operation Features

Added Hold Condition Modes.

Added Read Identification (RDID) information.

Added Release from Deep Power Down and Read Electronic Signature (RES) information.

Power-Up and Power-Down

Updated text.

Updated Power-Up Timing table.

DC Characteristics

Updated DC Characteristics CMOS Compatible table.

AC Characteristics

Updated AC Characteristic table with HOLD# signal timing values.

Updated SPI Mode 0 (0,0) Input Timing diagram.

Added HOLD# Timing diagram.

Ordering Information

Updated Ordering Information matrix.

Updated Valid Combination table.

Revision B0 (November 2, 2005)

Incorporated 32-Mb density.

Revision BI (June 23 2008)

Changed document status from *Advanced Information* to *Full Production*.

Updated trademarks and trademark section.

Revision B2 (June 25 2008)

Corrected document headers.

Colophon

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