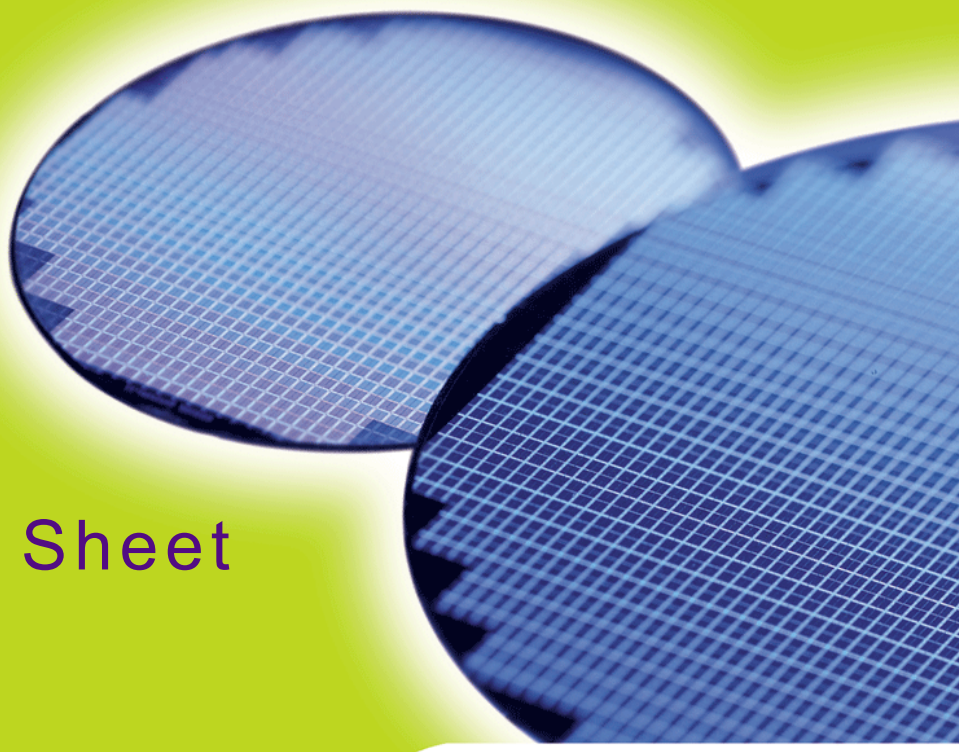
April 2008

IDSH1G–02A1F1C
IDSH1G–03A1F1C
IDSH1G–04A1F1C

1-Gbit Double-Data-Rate-Three SDRAM

DDR3 SDRAM
RoHS Compliant Products



Advance

Internet Data Sheet

Rev. 0.62

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Page 31	Updated output slew rates
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Page 9	Added “termination data strobe “ in table 3
Page 7	Corrected figure, Ballout for 1Gb × 8 Components
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	Inital document

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1 Overview

This chapter gives an overview of the Double-Data-Rate-Three (DDR3) SDRAM component product family and describes its main characteristics.

1.1 Features

The DDR3 SDRAM offers the following key features:

- 1.5 V ± 0.075 V supply voltage for V_{DD} and V_{DDQ}
- SDRAM configurations with ×4, ×8 and ×16 data in/outputs
- Eight internal banks for concurrent operation
- 8-Bit prefetch architecture
- Page Size:1 kByte page size for ×4 and ×8; 2 kByte page size for ×16 components
- Asynchronous $\overline{\text{RESET}}$
- Auto-Precharge operation for read and write commands
- Refresh, Self-Refresh and power saving Power-down modes; Auto Self-refresh (ASR) and Partial array self refresh (PASR)
- Average Refresh Period 7.8 µs at a T_{OPER} up to 85 °C, 3.9 µs up to 95 °C
- Operating temperature range 0 - 85 °C and 85 - 95 °C
- Data mask function for write operation
- Commands can be entered on each positive clock edge
- Data and data mask are referenced to both edges of a differential data strobe pair (double data rate)
- CAS latency (CL): 5, 6, 7, 8, 9, 10 and 11
- Posted CAS with programmable additive latency (AL = 0, CL–1 and CL–2) for improved command, address and data bus efficiency
- Read Latency RL = AL + CL
- Programmable CAS Write Latency (CWL) per operating frequency
- Write Latency WL = AL + CWL
- Burst length 8 (BL8) and burst chop 4(BC4) modes: fixed via mode register (MRS) or selectable On-The-Fly (OTF)
- Programmable read burst ordering: interleaved or nibble sequential
- Multi-purpose register (MPR) for readout of non-memory related information
- System level timing calibration support via write leveling and MPR read pattern
- Differential clock inputs (CK/$\overline{\text{CK}}$)
- Bi-directional, differential data strobe pair (DQS/$\overline{\text{DQS}}$) is transmitted / received with data. Edge aligned with read data and center-aligned with write data
- DLL aligns transmitted read data and strobe pair transition with clock
- Push-pull output driver with nominal R_{ON} of 34 Ω at V_{OUT} = V_{DDQ}/2
- Programmable on-die termination (ODT) for data, data mask and differential strobe pairs
- Dynamic ODT mode for improved signal integrity and pre-selectable termination impedances during writes
- Terminate DQS (TDQS) Feature for Mix of ×4 and ×8 based Memory Modules within a Memory Channel
- ZQ Calibration for output driver and on-die termination using external reference resistor to ground
- Two reference voltage inputs V_{REFDQ}, V_{REFCA}
- Lead and halogen free packages: 78 ball (PG-TFBGA-78) for ×4 and ×8 components
- Lead and halogen free packages: 96 ball (PG-TFBGA-96) for ×16 components, 0.8 × 0.8 mm ball pitch

1.2 Product List

The product list shows all possible products within the 1-Gbit DDR3 SDRAM first component generation. Availability depends on application needs. For Qimonda part number nomenclature see **Chapter 6**.

TABLE 1
Ordering Information

QAG Part Number	Max. Clock frequency	CAS-RCD-RP latencies	Supported CAS latencies	Speed Sort Name	Package
DDR3 SDRAM Components in ×4 Organization (256M × 4)					
IDSH1G-02A1F1C-08D	400	5-5-5		DDR3-800D	PG-TFBGA-78
IDSH1G-02A1F1C-08E	400	6-6-6		DDR3-800E	PG-TFBGA-78
IDSH1G-02A1F1C-10E	533	6-6-6		DDR3-1066E	PG-TFBGA-78
IDSH1G-02A1F1C-10F	533	7-7-7		DDR3-1066F	PG-TFBGA-78
IDSH1G-02A1F1C-10G	533	8-8-8		DDR3-1066G	PG-TFBGA-78
IDSH1G-02A1F1C-13G	667	8-8-8		DDR3-1333G	PG-TFBGA-78
IDSH1G-02A1F1C-13H	667	9-9-9		DDR3-1333H	PG-TFBGA-78
IDSH1G-02A1F1C-13J	667	10-10-10		DDR3-1333J	PG-TFBGA-78
DDR3 SDRAM Components in ×8 Organization (128M × 8)					
IDSH1G-03A1F1C-08D	400	5-5-5		DDR3-800D	PG-TFBGA-78
IDSH1G-03A1F1C-08E	400	6-6-6		DDR3-800E	PG-TFBGA-78
IDSH1G-03A1F1C-10E	533	6-6-6		DDR3-1066E	PG-TFBGA-78
IDSH1G-03A1F1C-10F	533	7-7-7		DDR3-1066F	PG-TFBGA-78
IDSH1G-03A1F1C-10G	533	8-8-8		DDR3-1066G	PG-TFBGA-78
IDSH1G-03A1F1C-13G	667	8-8-8		DDR3-1333G	PG-TFBGA-78
IDSH1G-03A1F1C-13H	667	9-9-9		DDR3-1333H	PG-TFBGA-78
IDSH1G-03A1F1C-13J	667	10-10-10		DDR3-1333J	PG-TFBGA-78
IDSH1G-03A1F1C-16G	800	8-8-8		DDR3-1600G	PG-TFBGA-78
IDSH1G-03A1F1C-16H	800	9-9-9		DDR3-1600H	PG-TFBGA-78
IDSH1G-03A1F1C-16J	800	10-10-10		DDR3-1600J	PG-TFBGA-78
IDSH1G-03A1F1C-16K	800	11-11-11		DDR3-1600K	PG-TFBGA-78
DDR3 SDRAM Components in ×16 Organization (64M × 16)					
IDSH1G-04A1F1C-08D	400	5-5-5		DDR3-800D	PG-TFBGA-96
IDSH1G-04A1F1C-08E	400	6-6-6		DDR3-800E	PG-TFBGA-96
IDSH1G-04A1F1C-10E	533	6-6-6		DDR3-1066E	PG-TFBGA-96
IDSH1G-04A1F1C-10F	533	7-7-7		DDR3-1066F	PG-TFBGA-96
IDSH1G-04A1F1C-10G	533	8-8-8		DDR3-1066G	PG-TFBGA-96
IDSH1G-04A1F1C-13G	667	8-8-8		DDR3-1333G	PG-TFBGA-96
IDSH1G-04A1F1C-13H	667	9-9-9		DDR3-1333H	PG-TFBGA-96
IDSH1G-04A1F1C-13J	667	10-10-10		DDR3-1333J	PG-TFBGA-96

1.3 DDR3 SDRAM Addressing

TABLE 2
1-Gbit DDR3 SDRAM Addressing

Configuration	256Mbit × 4	128Mbit × 8	64Mbit × 16	Note
Internal Organization	8 banks × 32 Mbits × 4	8 banks × 16 Mbits × 8	8 banks × 8 Mbits × 16	
Number of Banks	8	8	8	
Bank Address	BA[2:0]	BA[2:0]	BA[2:0]	
Row Address	A[13:0]	A[13:0]	A[12:0]	
Number of addressable Rows	8K	8K	4K	
Column Address	A[9:0], A11	A[9:0]	A[9:0]	
Number of addressable Columns (page length)	2048	1024	1024	1)
Page Size	1 KB	1 KB	2 KB	2)
Auto-Precharge	A10 / AP	A10 / AP	A10 / AP	
Burst length on-the-fly bit	A12/$\overline{BC}$	A12/$\overline{BC}$	A12/$\overline{BC}$	

1) Page length is the number of addressable columns and is defined as $2^{COLBITS}$, where COLBITS is the number of column address bits, excluding A10/AP and A12/$\overline{BC}$

2) Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per memory bank and calculated as follows: Page Size = $2^{COLBITS}$ × ORG/8, where COLBITS is the number of column address bits and ORG is the number of DQ bits for a given SDRAM configuration (×4, ×8 or ×16).

1.4 Package Ballout

Figure 1, **Figure 2** and **Figure 3** show the ballouts for DDR3 SDRAM components. See **Chapter 6** for package outlines.

FIGURE 1
Ballout for 1Gb ×4 Components (PG-TFBGA-78)

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NC	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	NC	$\overline{\text{DQS}}$				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	NC				NC	NC	VDDQ	E
F	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	F
G	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	G
H	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				NC	VREFCA	VSS	J
K	VDD	A3	A0				A12 / $\overline{\text{BC}}$	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	$\overline{\text{RESET}}$	A13				NC	A8	VSS	N

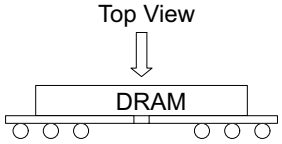

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FIGURE 2
Ballout for 1Gb × 8 Components (PG-TFBGA-78)

	1	2	3	4	5	6	7	8	9	
A	VSS	VDD	NC				NU/$\overline{\text{TDQS}}$	VSS	VDD	A
B	VSS	VSSQ	DQ0				DM/TDQS	VSSQ	VDDQ	B
C	VDDQ	DQ2	DQS				DQ1	DQ3	VSSQ	C
D	VSSQ	DQ6	$\overline{\text{DQS}}$				VDD	VSS	VSSQ	D
E	VREFDQ	VDDQ	DQ4				DQ7	DQ5	VDDQ	E
F	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	F
G	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	G
H	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	H
J	VSS	BA0	BA2				NC	VREFCA	VSS	J
K	VDD	A3	A0				A12 / $\overline{\text{BC}}$	BA1	VDD	K
L	VSS	A5	A2				A1	A4	VSS	L
M	VDD	A7	A9				A11	A6	VDD	M
N	VSS	$\overline{\text{RESET}}$	A13				NC	A8	VSS	N

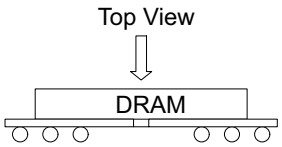

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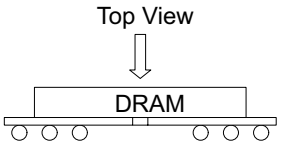
FIGURE 3
Ballout for 1Gb × 16 Components (PG-TFBGA-96)

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				$\overline{\text{DQSU}}$	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	$\overline{\text{DQSL}}$				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	$\overline{\text{RAS}}$				CK	VSS	NC	J
K	ODT	VDD	$\overline{\text{CAS}}$				$\overline{\text{CK}}$	VDD	CKE	K
L	NC	$\overline{\text{CS}}$	$\overline{\text{WE}}$				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12 / $\overline{\text{BC}}$	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	$\overline{\text{RESET}}$	NC				NC	A8	VSS	T



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1.5 Input / Output Signal Functional Description

TABLE 3
Input / Output Signal Functional Description

Symbol	EDA Signal Name[1)]	Type	Function
CK, $\overline{CK}$	ck_t, ck_c	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	cke	Input	**Clock Enable:** CKE High activates, and CKE Low deactivates internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (active row in any bank). CKE is asynchronous for Self-Refresh exit. After V_{REFCA} and V_{REFDQ} have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained High throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$, ODT, CKE and $\overline{RESET}$ are disabled during Power-down. Input buffers, excluding CKE and $\overline{RESET}$ are disabled during self refresh.
$\overline{CS}$	cs_n	Input	**Chip Select:** All command are masked when $\overline{CS}$ is registered High. $\overline{CS}$ provides for external Rank selection on systems with multiple ranks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	ras_n, cas_n, we_n	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
ODT	odt	Input	**On-Die Termination:** ODT (registered High) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM signal for ×4/×8 configurations. For ×16 configuration ODT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, DMU and DML signal. The ODT signal will be ignored if the Mode Register MR1 is programmed to disable ODT and during Self Refresh.
DM (×4, ×8); DMU, DML (×16)	dm (×4); dm_tdqs_t (×8); dmu, dml (×16)	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a Write access. DM is sampled on both edges of DQS. DMU and DML are the input mask signals for ×16 components and control the lower or upper bytes.
TDQS/$\overline{TDQS}$	dm_tdqs_t, nu_tdqs_c	Termination	**Termination Data Strobe:** TDQS/$\overline{TDQS}$ is applicable for ×8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{TDQS}$ is not used. ×4/×16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
BA0 - BA2	ba0 - ba2	Input	**Bank Address Inputs:** Define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a mode register set cycle.

Symbol	EDA Signal Name[1)]	Type	Function
A0 - A13(×4, ×8); A0-A12(×16)	a0 - a13(×4, ×8); a0-a12(×16)	Input	**Address Inputs:** Provides the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/$\overline{BC}$ have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands. For numbers of addresses used on this assembly see **Table 2**.
A10 / AP	a10	Input	**Auto-Precharge:** A10/AP is sampled during Read/Write commands to determine whether Auto-Precharge should be performed to the accessed bank after the Read/Write operation. (High: Auto-Precharge, Low: no Auto-Precharge). A10/AP is sampled during Precharge command to determine whether the Precharge applies to one bank (A10 Low) or all banks (A10 High). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	a12	Input	**Burst Chop:** A12/$\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (High: no burst chop, Low: burst chopped). See **"Command Truth Table" on Page 11** for details.
DQ (×4, ×8); DQL/DQU (×16)	dq (×4, ×8) dql/dqu (×16)	Input/ Output	**Data Input/Output:** Bi-directional data bus.
DQS / $\overline{DQS}$ (×4, ×8); DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$(×16)	dqs_t / dqs_c (×4, ×8); dqsl_t, dqsl_c, dqsu_t, dqsu_c (×16)	Input/ Output	**Data Strobe:** output with read data, input with write data. Edge-aligned with read data, centered in write data. For the ×16, DQSL corresponds to the data on DQL0 - DQL7; DQSU corresponds to the data on DQU0-DQU7.The data strobes DQS, DQSL and DQSU are paired with differential signals $\overline{DQS}$, $\overline{DQSL}$ and $\overline{DQSU}$, respectively, to provide differential pair signaling to the system during both reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
$\overline{RESET}$	reset_n	CMOS Input	**Active Low Asynchronous Reset:** Reset is active when $\overline{RESET}$ is Low, and inactive when $\overline{RESET}$ is High. $\overline{RESET}$ must be High during normal operation. $\overline{RESET}$ is a CMOS rail to rail signal with DC High and Low are 80% and 20% of V_{DD}, $\overline{RESET}$ active is destructive to data contents.
NC	—	—	**No Connect:** no internal electrical connection is present
V_{DDQ}	vddq	Supply	**DQ Power Supply:** 1.5 V ± 0.075 V
V_{SSQ}	vssq	Supply	**DQ Ground**
V_{DD}	vdd	Supply	**Power Supply:** 1.5 V ± 0.075 V
V_{SS}	vss	Supply	**Ground**
V_{REFDQ}	vrefdq	Supply	**Reference Voltage for DQ**
V_{REFCA}	vrefca	Supply	**Reference Voltage for Command and Address inputs**
ZQ	zq	Supply	Reference ball for ZQ calibration

1) The EDA Signal Name is used in Qimonda's Simulation Models such as IBIS, Verilog, etc.

Note: Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, and $\overline{RESET}$) do not supply termination.

2 Functional Description

The DDR3 SDRAM is a high-speed dynamic random-access memory internally configured as an eight-bank SDRAM.

2.1 Truth Tables

The truth tables list the input signal values at a given clock edge which represent a command or state transition expected to be executed by the DDR3 SDRAM . **Table 4** lists all valid commands to the DDR3 SDRAM. For a detailed description of the various power mode entries and exits please refer to **Table 5**. In addition, the DM functionality is described in **Table 6**.

TABLE 4
Command Truth Table

Function	Abbr.	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA2 - BA0	A15 - A13	A12/$\overline{BC}$	A10/AP	A11, A9-A0	Note
		Prev. Cycle	Curr. Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				1)2)3)4)5)
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	1)2)3)4)5)
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	1)2)3)4)5)6)7)8)
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	1)2)3)4)5)6)7)8)9)
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	1)2)3)4)5)
Precharge all Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	1)2)3)4)5)
Active	ACT	H	H	L	L	H	H	BA	RA (Row Address)				1)2)3)4)5)
Write (BL8MRS or BC4MRS)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	1)2)3)4)5)10)
Write (BC4OTF)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	1)2)3)4)5)10)
Write (BL8OTF)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	1)2)3)4)5)10)
Write w/AP (BL8MRS or BC4MRS)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	1)2)3)4)5)10)
Write w/AP (BC4OTF)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	1)2)3)4)5)10)
Write w/AP (BL8OTF)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	1)2)3)4)5)10)
Read (BL8MRS or BC4MRS)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	1)2)3)4)5)10)
Read (BC4OTF)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	1)2)3)4)5)10)
Read (BL8OTF)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	1)2)3)4)5)10)
Read w/AP (BL8MRS or BC4MRS)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	1)2)3)4)5)10)
Read w/AP (BC4OTF)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	1)2)3)4)5)10)
Read w/AP (BL8OTF)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	1)2)3)4)5)10)
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	1)2)3)4)5)11)

Function	Abbr.	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA2 - BA0	A15 - A13	A12/ $\overline{BC}$	A10/ AP	A11, A9-A0	Note
		Prev. Cycle	Curr. Cycle										
Device Deselect	DES	H	H	H	X	X	X	X	X	X	X	X	1)2)3)4)5)12)
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	1)2)3)4)5)8)13)
				H	V	V	V						
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	1)2)3)4)5)8)13)
				H	V	V	V						
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	1)2)3)4)5)
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	1)2)3)4)5)

1) BA = Bank Address, RA = Row Address, CA = Column Address, $\overline{BC}$ = Burst Chop, AP = Auto Precharge, X = Don't care, V = valid
2) All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The higher order address bits of BA, RA and CA are device density and IO configuration (×4, ×8, ×16) dependent.
3) $\overline{RESET}$ is a low active signal which will be used only for asynchronous reset. It must be maintained High during any function.
4) Bank addresses (BA) determine which bank is to be operated upon. For MRS, BA selects a Mode Register.
5) V means H or L (but a defined logic level) and X means either "defined or undefined (like floating) logic level".
6) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh
7) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation.
8) Refer to **"Clock Enable (CKE) Truth Table for Synchronous Transitions" on Page 13** for more detail with CKE transition.
9) Self refresh exit is asynchronous.
10) Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
11) The No Operation (NOP) command should be used in cases when the DDR3 SDRAM is in an idle or a wait state. The purpose of the NOP command is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A NOP command will not terminate a previous operation that is still executing, such as a read or write burst.
12) The Deselect command (DES) performs the same function as a No Operation command.
13) The Power Down Mode does not perform any refresh operation.

TABLE 5
Clock Enable (CKE) Truth Table for Synchronous Transitions

Current State [1]	CKE(N-1)[2]	CKE(N)[2]	Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Note
	Previous Cycle	Current Cycle			
Power Down	L	L	X	Maintain Power Down	4)5)6)7)8)9)
	L	H	DES or NOP	Power Down Exit	4)5)6)7)8)10)
Self Refresh	L	L	X	Maintain Self Refresh	4)5)6)7)9)11)
	L	H	DES or NOP	Self Refresh Exit	4)5)6)7)11)12)13)
Bank(s) Active	H	L	DES or NOP	Active Power Down Entry	4)5)6)7)8)10)14)
Reading	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Writing	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Precharging	H	L	DES or NOP	Power Down Entry	4)5)6)7)8)10)14)15)
Refreshing	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)
All Banks Idle	H	L	DES or NOP	Precharge Power Down Entry	4)5)6)7)10)8)14)16)
	H	L	REF	Self Refresh Entry	4)5)6)7)14)16)17)
Any other state	Refer to **"Command Truth Table" on Page 11** for more detail with all command signals				4)5)6)7)18)

1) Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
2) CKE(N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
3) COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.
4) All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5) The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
6) CKE must be registered with the same value on $t_{CKE.MIN}$ consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the $t_{CKE.MIN}$ clocks of registeration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + $t_{CKE.MIN}$ + t_{IH}.
7) DES and NOP are defined in **"Command Truth Table" on Page 11**.
8) The Power Down does not perform any refresh operations
9) X means Don't care (including floating around V_{REFCA}) in Self Refresh and Power Down. It also applies to address pins.
10) Valid commands for Power Down Entry and Exit are NOP and DES only
11) V_{REF} (both V_{REFCA} and V_{REFDQ}) must be maintained during Self Refresh operation.
12) On Self Refresh Exit DES or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read, or ODT commands may be issued only after t_{XSDLL} is satisfied.
13) Valid commands for Self Refresh Exit are NOP and DES only.
14) Self Refresh can not be entered while Read or Write operations are in progress.
15) If all banks are closed at the conclusion of a read, write or precharge command then Precharge Power-down is entered, otherwise Active Power-down is entered.
16) 'Idle state' is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is High, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, $t_{ZQ.INIT}$, $t_{ZQ.OPER}$, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).
17) Self Refresh mode can only be entered from the All Banks Idle state.
18) Must be a legal command as defined in **"Command Truth Table" on Page 11**.

TABLE 6
Data Mask (DM) Truth Table

Name (Function)	DM	DQs
Write Enable	L	Valid
Write Inhibit	H	X

2.2 Mode Register 0 (MR0)

The mode register MR0 stores the data for controlling various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLL reset, WR (write recovery time for auto-precharge) and DLL control for precharge Power-Down, which includes various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1, and BA2, while controlling the states of address pins according to **Table 7**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0[1)]	PPD	WR			DLL res	TM	CL			RBT	CL	BL	

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TABLE 7
MR0 Mode register Definition (BA[2:0]=000_B)

Field	Bits[1)]	Description
BL	A[1:0]	**Burst Length (BL) and Control Method** Number of sequential bits per DQ related to one Read/Write command. 00_B **BL8MRS** mode with fixed burst length of 8. A12/$\overline{BC}$ at Read or Write command time is Don't care at read or write command time. 01_B **BLOTF** on-the-fly (OTF) enabled using A12/$\overline{BC}$ at Read or Write command time. When A12/$\overline{BC}$ is High during Read or Write command time a burst length of 8 is selected (BL8OTF mode). When A12/$\overline{BC}$ is Low, a burst chop of 4 is selected (BC4OTF mode). Auto-Precharge can be enabled or disabled. 10_B **BC4MRS** mode with fixed burst chop of 4 with $t_{CCD} = 4 \times n_{CK}$. A12/$\overline{BC}$ is Don't care at Read or Write command time. 11_B **TBD** Reserved
RBT	A3	**Read Burst Type** 0_B Nibble Sequential 1_B Interleaved

Field	Bits[1)]	Description
CL	A[6:4,2]	**CAS Latency (CL)** CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. *Note: All other bit combinations are reserved.* 0000_B RESERVED 0010_B 5 0100_B 6 0110_B 7 1000_B 8 1010_B 9 1100_B 10 1110_B 11
TM	A7	**Test Mode** The normal operating mode is selected by MR0(bit A7 = 0) and all other bits set to the desired values shown in this table. Programming bit A7 to a 1 places the DDR3 SDRAM into a test mode that is only used by the SDRAM manufacturer and should NOT be used. No operations or functionality is guaranteed if A7 = 1. 0_B Normal Mode 1_B Vendor specific test mode
DLLres	A8	**DLL Reset** The internal DLL Reset bit is self-clearing, meaning it returns back to the value of 0 after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, t_{DLLK} must be met before any functions that require the DLL can be used (i.e. Read commands or synchronous ODT operations). 0_B No DLL Reset 1_B DLL Reset triggered
WR	A[11:9]	**Write Recovery for Auto-Precharge** Number of clock cycles for write recovery during Auto-Precharge. WR_{MIN} in clock cycles is calculated by dividing $t_{WR.MIN}$ (in ns) by the actual $t_{CK.AVG}$ (in ns) and rounding up to the next integer: WR.MIN [n_{CK}] = Roundup($t_{WR.MIN}$[ns] / $t_{CK.AVG}$[ns]). The WR value in the mode register must be programmed to be equal or larger than WR.MIN. The resulting WR value is also used with t_{RP} to determine t_{DAL}. Since WR of 9 and 11 is not implemented in DDR3 and the above formula results in these values, higher values have to be programmed. 000_B Reserved 001_B 5 010_B 6 011_B 7 100_B 8 101_B 10 110_B 12 111_B Reserved
PPD	A12	**Precharge Power-Down DLL Control** Active Power-Down will always be with DLL-on. Bit A12 will have no effect in this case. For Precharge Power-Down, bit A12 in MR0 is used to select the DLL usage as shown below. 0_B **Slow Exit.** DLL is frozen during precharge Power-down.Read and synchronous ODT commands are only allowed after t_{XPDLL}. 1_B **Fast Exit.** DLL remains on during precharge Power-down.Any command can be applied after t_{XP}, provided that other timing parameters are satisfied.

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to 0_B.

2.3 Mode Register 1 (MR1)

The Mode Register MR1 stores the data for enabling or disabling the DLL, output driver strength, R_{TT_NOM} impedance, additive latency (AL), Write leveling enable and Qoff (output disable). The Mode Register MR1 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA0 and Low on BA1and BA2, while controlling the states of address pins according to **Table 8**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0[1)]	Qoff	TDQS	0	RTT_ nom	0	Level	RTT_ nom	DIC	AL		RTT_ nom	DIC	DLL dis

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TABLE 8
MR1 Mode Register Definition (BA[2:0]=001_B)

Field	Bits[1)]	Description
DLLdis	A0	**DLL Disable** The DLL must be enabled for normal operation. DLL enable is required during power up initialization, after reset and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1(A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled and reset upon exit of Self-Refresh operation. Any time the DLL is enabled, a DLL reset must be issued afterwards. Any time the DLL is reset, t_{DLLK} clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{DQSCK}, t_{AON}, t_{AOF} or t_{ADC} parameters. During t_{DLLK}, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation. . 0_B DLL is enabled 1_B DLL is disabled
DIC	A[5, 1]	**Output Driver Impedance Control** *Note: All other bit combinations are reserved.* 00_B Nominal Drive Strength RON40 = RZQ/6 (nominal 40.0 Ω, with nominal RZQ = 240 Ω) 01_B Nominal Drive Strength RON34 = RZQ/7 (nominal 34.3 Ω, with nominal RZQ = 240 Ω)
R_{TT_NOM}	A[9, 6, 2]	**Nominal Termination Resistance of ODT** **Notes** 1. *If R_{TT_NOM} is used during Writes, only the values $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* 2. *In Write leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all R_{TT}_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 0, only R_{TT_NOM} settings of $R_{ZQ}/2$, $R_{ZQ}/4$ and $R_{ZQ}/6$ are allowed.* 3. *All other bit combinations are reserved.* 000_B ODT disabled, R_{TT_NOM} = off, Dynamic ODT mode disabled 001_B RTT60 = RZQ / 4 (nominal 60 Ω with nominal RZQ = 240 Ω) 010_B RTT120 = RZQ / 2 (nominal 120 Ω with nominal RZQ = 240 Ω 011_B RTT40 = RZQ / 6 (nominal 40 Ω with nominal RZQ = 240 Ω) 100_B RTT20 = RZQ / 12 (nominal 20 Ω with nominal RZQ = 240 Ω) 101_B RTT30 = RZQ / 8 (nominal 30 Ω with nominal RZQ = 240 Ω)

Field	Bits[1)]	Description
AL	A[4, 3]	**Additive Latency (AL)** Any read or write command is held for the time of Additive Latency (AL) before it is issued as internal read or write command. **Notes** *1. AL has a value of CL - 1 or CL - 2 as per the CL value programmed in the MR0 register.* 00_B AL = 0 (AL disabled) 01_B AL = CL - 1 10_B AL = CL - 2 11_B Reserved
Level	A7	**Write Leveling Mode** 0_B **Write Leveling Mode** Disabled, Normal operation mode 1_B **Write Leveling Mode** Enabled
TDQS	A11	**TDQS enable** 0_B Disable 1_B Enable
Qoff	A12	**Output Disable** Under normal operation, the SDRAM outputs are enabled during read operation and write leveling for driving data (Qoff bit in the MR1 is set to 0_B). When the Qoff bit is set to 1_B, the SDRAM outputs (DQ, DQS, $\overline{DQS}$, also on upper byte lane in case of ×16) will be disabled - also during write leveling. Disabling the SDRAM outputs allows users to run write leveling on multiple ranks and to measure I_{DD} currents during Read operations, without including the output. 0_B Output buffer enabled 1_B Output buffer disabled

1) A13, A14, A15 - even if not available on a specific device - must be programmed to 0_B.

2.4 Mode Register 2 (MR2)

The Mode Register MR2 stores the data for controlling refresh related features, R_{TT_WR} impedance, and CAS write latency. The Mode Register MR2 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA1 and Low on BA0 and BA2, while controlling the states of address signals according to **Table 9**.

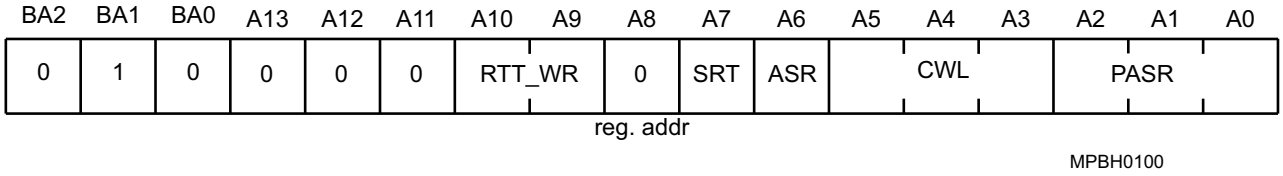

TABLE 9
MR2 Mode Register Definition (BA[2:0]=010_B)

Field	Bits[1)]	Description
PASR	A[2:0]	**Partial Array Self Refresh (PASR)** If PASR (Partial Array Self Refresh) is enabled, data located in areas of the array beyond the specified self refresh location may get lost if self refresh is entered. During non-self-refresh operation, data integrity will be maintained if t_{REFI} conditions are met. 000_B Full array (Banks 000_B - 111_B) 001_B Half Array(Banks 000_B - 011_B) 010_B Quarter Array(Banks 000_B - 001_B) 011_B 1/8th array (Banks 000_B) 100_B 3/4 array(Banks 010_B - 111_B) 101_B Half array(Banks 100_B - 111_B) 110_B Quarter array(Banks 110_B - 111_B) 111_B 1/8th array(Banks 111_B)
CWL	A[5:3]	**CAS Write Latency (CWL)** Number of clock cycles from internal write command to first write data in. 000_B 5 (3.3 ns ≥ $t_{CK.AVG}$ ≥ 2.5 ns) 001_B 6 (2.5 ns > $t_{CK.AVG}$ ≥ 1.875 ns) 010_B 7 (1.875 ns > $t_{CK.AVG}$ ≥ 1.5 ns) 011_B 8 (1.5 ns > $t_{CK.AVG}$ ≥ 1.25 ns) *Note: Besides CWL limitations on $t_{CK.AVG}$, there are also $t_{AA.MIN/MAX}$ restrictions that need to be observed. For details, please refer to* ***"Speed Bins" on Page 35****.*
ASR	A6	**Auto Self Refresh (ASR)** When enabled, DDR3 SDRAM will automatically provide appropriate self refresh entry all supported operating temperature values. If not enabled, the SRT bit must be programmed to indicate T_{OPER} during subsequent self refresh operation. 0_B Disabled, manual Self-Refresh Reference (SRT) 1_B Auto Self Refresh enabled

Field	Bits[1)]	Description
SRT	A7	**Self-Refresh Temperature Range (SRT)** If ASR = 0, the SRT bit must be programmed to indicate T_{OPER} during subsequent self refresh operation. If ASR = 1, SRT bit must be set to 0_b. 0_B Normal operating temperature range 1_B Extended operating temperature range
R_{TT_WR}	A[10:9]	**Dynamic ODT mode and R_{TT_WR} Pre-selection** **Notes** *1. The R_{TT_WR} value can be applied during writes even when R_{TT_NOM} is disabled. During write leveling, Dynamic ODT is not available.* 00_B Dynamic ODT mode disabled 01_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/4 = 60 Ω 10_B Dynamic ODT mode enabled with R_{TT_WR} = RZQ/2 = 120Ω

1) A13, A14, A15 - even if not available on a specific device - must be programmed to 0_B.

2.5 Mode Register 3 (MR3)

The Mode Register MR3 controls Multi purpose registers and optional On-die thermal sensor (ODTS) feature. The Mode Register MR3 is written by asserting Low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, High on BA1 and BA0, and Low on BA2 while controlling the states of address signals according to **Table 10**.

BA2	BA1	BA0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	1	0	0	0	0	0	0	0	0	0	0	0	MPR	MPR loc	

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TABLE 10
MR3 Mode Register Definition (BA[2:0]=011_B)

Field	Bits[1)]	Description
MPR loc	A[1:0]	**Multi Purpose Register Location** 00_B Pre-defined data pattern for read synchronization 01_B RFU 10_B RFU 11_B RFU
MPR	A2	**Multi Purpose Register Enable** 0_B MPR disabled, normal memory operation 1_B Dataflow from the Multi Purpose register MPR

1) A13, A14 and A15 - even if not available on a specific device - must be programmed to 0_B.

2.6 Read / Write Operations and Access Modes

After a bank has been activated, a read or write access can be executed. This is accomplished by setting $\overline{RAS}$ High, $\overline{CS}$ and $\overline{CAS}$ Low at the clock's rising edge. $\overline{WE}$ must also be defined at this time to determine whether the access cycle is a read operation ($\overline{WE}$ High) or a write operation ($\overline{WE}$ Low). The DDR3 SDRAM provides a burst column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock edges.

2.6.1 Burst Order

Accesses within a given burst may be interleaved or nibble sequential depending on the programmed bit A3 in the mode register MR0.

Regarding read commands, the lower 3 column address bits CA[2:0] at read command time determine the start address for the read burst.

Regarding write commands, the burst order is always fixed. For writes with a burst length of 8, the inputs on the lower 3 column address bits CA[2:0] are ignored during the write command. For writes with a burst being chopped to 4, the input on column address 2 (CA[2]) determines if the lower or upper four burst bits are selected. In this case, the inputs on the lower 2 column address bits CA[1:0] are ignored during the write command.The following table shows burst order versus burst start address for reads and writes of bursts of 8 as well as of bursts of 4 operation (burst chop).

TABLE 11
Bit Order during Burst

Burst Length	Command	Column Address 2:0			Interleaved Burst Sequence								Nibble Sequential Burst Sequence								Note
					Bit Order within Burst								Bit Order within Burst								
		CA2	CA1	CA0	1.	2.	3.	4.	5.	6.	7.	8.	1.	2.	3.	4.	5.	6.	7.	8.	
8	READ	0	0	0	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)
		0	0	1	**1**	0	3	2	**5**	4	7	6	**1**	2	3	0	**5**	6	7	4	1)
		0	1	0	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	1)
		0	1	1	**3**	2	1	0	**7**	6	5	4	**3**	0	1	2	**7**	4	5	6	1)
		1	0	0	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	1)
		1	0	1	**5**	4	7	6	**1**	0	3	2	**5**	6	7	4	**1**	2	3	0	1)
		1	1	0	**6**	7	4	5	**2**	3	0	1	**6**	7	4	5	**2**	3	0	1	1)
		1	1	1	**7**	6	5	4	**3**	2	1	0	**7**	4	5	6	**3**	0	1	2	1)
	WRITE	V	V	V	**0**	1	2	3	**4**	5	6	7	**0**	1	2	3	**4**	5	6	7	1)2)
4 (Burst Chop Mode)	READ	0	0	0	**0**	1	2	3	**T**	T	T	T	**0**	1	2	3	**T**	T	T	T	1)3)4)
		0	0	1	**1**	0	3	2	**T**	T	T	T	**1**	2	3	0	**T**	T	T	T	1)3)4)
		0	1	0	**2**	3	0	1	**T**	T	T	T	**2**	3	0	1	**T**	T	T	T	1)3)4)
		0	1	1	**3**	2	1	0	**T**	T	T	T	**3**	0	1	2	**T**	T	T	T	1)3)4)
		1	0	0	**4**	5	6	7	**T**	T	T	T	**4**	5	6	7	**T**	T	T	T	1)3)4)
		1	0	1	**5**	4	7	6	**T**	T	T	T	**5**	6	7	4	**T**	T	T	T	1)3)4)
		1	1	0	**6**	7	4	5	**T**	T	T	T	**6**	7	4	5	**T**	T	T	T	1)3)4)
		1	1	1	**7**	6	5	4	**T**	T	T	T	**7**	4	5	6	**T**	T	T	T	1)3)4)
	WRITE	0	V	V	**0**	1	2	3	**X**	X	X	X	**0**	1	2	3	**X**	X	X	X	1)2)4)5)
		1	V	V	**4**	5	6	7	**X**	X	X	X	**4**	5	6	7	**X**	X	X	X	1)2)4)5)

1) 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
2) V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
3) T: output drivers for data and strobe are in high impedance.
4) In case of BC4MRS (burst length being fixed to 4 by MR0 setting), the internal write operation starts two clock cycles earlier than for the BL8 modes. This means that the starting point for t_{WR} and t_{WTR} will be pulled in by two clocks. In case of BC4OTF mode (burst length being selected on-the-fly via A12/$\overline{BC}$), the internal write operation starts at the same point in time as a burst of 8 write operation. This means that during on-the-fly control, the starting point for t_{WR} and t_{WTR} will not be pulled in by two clocks.
5) X: Don't Care

3 Operating Conditions and Interface Specification

3.1 Absolute Maximum Ratings

TABLE 12
Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Voltage on V_{DD} ball relative to V_{SS}	V_{DD}	–0.4	+1.975	V	1)2)
Voltage on V_{DDQ} ball relative to V_{SS}	V_{DDQ}	–0.4	+1.975	V	1)2)
Voltage on any ball relative to V_{SS}	V_{IN}, V_{OUT}	–0.4	+1.975	V	1)
Storage Temperature	T_{STG}	–55	+100	°C	1)3)

1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2) V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{REFDQ} and V_{REFCA} must not be greater than 0.6 × V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV, V_{REFDQ} and V_{REFCA} may be equal or less than 300 mV.

3) Storage Temperature is the case surface temperature on the center/top side of the SDRAM. For the measurement conditions, please refer to JESD51-2 standard.

3.2 Operating Conditions

TABLE 13
SDRAM Component Operating Temperature Range

Parameter	Symbol	Rating		Unit	Note
		Min.	Max.		
Normal Operating Temperature Range	T_{OPER}	0	85	°C	1)2)3)
Extended Temperature Range		85	95	°C	1)3)4)

1) Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the SDRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2) The Normal Temperature Range specifies the temperatures where all SDRAM specification will be supported.
3) During operation, the SDRAM operating temperature must be maintained above 0 °C under all operating conditions. Either the device operating temperature rating may be used to set an appropriate refresh rate and/or to monitor the maximum operating temperature.
4) Some application require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C operating temperature. Full specifications are provided in this range, but the following additional conditions apply:
a) Refresh commands have to be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9 µs.
b) If Self-Refresh operation is required in the Extended Temperature Range, than it is mandatory to eitheruse the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0_B and MR2 A7 = 1_B) or enable the Auto Self-Refresh mode (ASR) (MR2 A6 = 1_B and MR2 A7= 0_B). For SDRAM operations on DIMM module refer to DIMM module data sheets and SPD bytes for Extended Temperature and Auto Self-Refresh option availability.

TABLE 14
DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply Voltage	V_{DD}	1.425	1.5	1.575	V	1)2)
Supply Voltage for Output	V_{DDQ}	1.425	1.5	1.575	V	1)2)
Reference Voltage for DQ, DM inputs	$V_{REFDQ.DC}$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3)4)
Reference Voltage for ADD, CMD inputs	$V_{REFCA.DC}$	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3)4)
External Calibration Resistor connected from ZQ ball to ground	R_{ZQ}	237.6	240.0	242.4	Ω	5)

1) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together
2) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
3) The AC peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF.DC}$ by more than ±1% V_{DD} (for reference: approx. ± 15 mV).
4) For reference: approx. V_{DD}/2 ± 15 mV.
5) The external calibration resistor R_{ZQ} can be time-shared among DRAMs in multi-rank DIMMs.

TABLE 15
Input and Output Leakage Currents

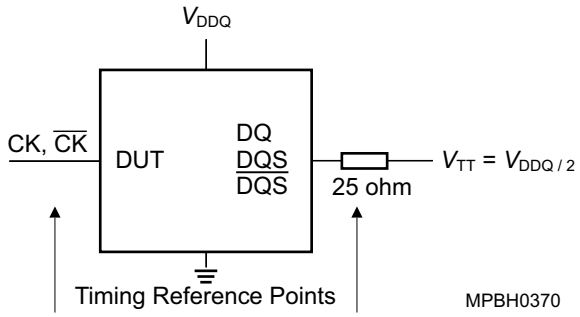
Parameter	Symbol	Condition	Rating		Unit	Note
			Min.	Max.		
Input Leakage Current	I_{IL}	Any input 0 V < V_{IN} < V_{DD}	–2	+2	µA	1)2)
Output Leakage Current	I_{OL}	0V < V_{OUT} < V_{DDQ}	–5	+5	µA	2)3)

1) All other balls not under test = 0 V.
2) Values are shown per ball.
3) DQ's, DQS, $\overline{DQS}$ and ODT are disabled.

3.3 Interface Test Conditions

Figure 4 represents the effective reference load of 25 Ω used in defining the relevant timing parameters of the device as well as for output slew rate measurements. It is not intended as either a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Qimonda correlates to its production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

FIGURE 4
Reference Load for AC Timings and Output Slew Rates



The Timing Reference Points are the idealized input and output nodes / terminals on the outside of the packaged SDRAM device as they would appear in a schematic or an IBIS model. The output timing reference voltage level for single ended signals is the cross point with $V_{TT.}$ The output timing reference voltage level for differential signals is the cross point of the true (e.g. DQS) and the complement (e.g. $\overline{DQS}$) signal.

3.4 Voltage Levels

3.4.1 DC and AC Logic Input Levels

Table 16 shows the input levels for single-ended input signals for Address and Control Signals.
Table 17 shows the input levels for single-ended input signals for DQ and DM Signals.

TABLE 16
DC and AC Input Levels for Single-Ended Command, Address and Control Signals

Parameter	Symbol	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Unit	Note
		Min.	Max.	Min.	Max.		
DC input logic high	$V_{IH.CA.DC}$	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.CA.DC}$	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.CA.AC}$	V_{REF} + 0.175	See 2)	V_{REF} + 0.175	See 2)	V	1)
AC input logic low	$V_{IL.CA.AC}$	See 2)	V_{REF} - 0.175	See 2)	V_{REF} - 0.175	V	1)
Reduced AC input logic high	$V_{IH.CA.AC150}$	—	—	V_{REF} + 0.150	See 2)	V	1)
Reduced AC input logic low	$V_{IL.CA.AC150}$	—	—	See 2)	V_{REF} - 0.150	V	1)

1) For input only pins except RESET: $V_{REF} = V_{REF.CA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.

TABLE 17
DC and AC Input Levels for Single-Ended DQ and DM Signals

Parameter	Symbol	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Unit	Note
		Min.	Max.	Min.	Max.		
DC input logic high	$V_{IH.DQ.DC}$	V_{REF} + 0.100	V_{DD}	V_{REF} + 0.100	V_{DD}	V	1)
DC input logic low	$V_{IL.DQ.DC}$	V_{SS}	V_{REF} - 0.100	V_{SS}	V_{REF} - 0.100	V	1)
AC input logic high	$V_{IH.DQ.AC}$	V_{REF} + 0.175	See 2)	V_{REF} + 0.150	See 2)	V	1) 3)
AC input logic low	$V_{IL.DQ.AC}$	See 2)	V_{REF} - 0.175	See 2)	V_{REF} - 0.150	V	1) 3)

1) For DQ and DM: $V_{REF} = V_{REFDQ}$, for input only signals except $\overline{\text{RESET}}$: $V_{REF} = V_{REFCA}$
2) See **Chapter 3.9**, **Overshoot and Undershoot Specification**.
3) Single ended swing requirement for DQS, $\overline{\text{DQS}}$ is 350 mV (peak to peak). Differential swing requirement for DQS, $\overline{\text{DQS}}$ is 700 mV (peak to peak).

Differential Swing Requirement for Differential Signals

Table 18 shows the input levels for differential input signals.

TABLE 18
Differential Swing Requirement for Clock (CK - $\overline{CK}$) and Strobe (DQS - $\overline{DQS}$)

Parameter	Symbol	DDR3–800, DDR3–1066, DDR3–1333, DDR3–1600		Unit	Note
		Min.	Max.		
Differential input high	$V_{IH.DIFF}$	+0.200	See [1]	V	[2]
Differential input low	$V_{IL.DIFF}$	See[1]	–0.200	V	[2]
Differential input high AC	$V_{IH.DIFF.AC}$	2 × ($V_{IH.AC}$ - V_{REF}) [3]	See [1]	V	[4]
Differential input low AC	$V_{IL.DIFF.AC}$	See [1]	2 × (V_{REF} - $V_{IL.AC}$) [5]	V	[4]

1) These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits ($V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to **Chapter 3.9**.
2) Used to define a differential signal slew-rate.
3) Clock: use $V_{IH.CA.AC}$ for $V_{IH.AC}$. Strobe: use $V_{IH.DQ.AC}$ for $V_{IH.AC}$.
4) For CK - $\overline{CK}$ use $V_{IH}/V_{IL.CA.AC}$ of ADD/CMD and V_{REFCA} ; for DQS - $\overline{DQS}$ (×4, ×8); or DQSL - $\overline{DQSL}$, DQSU - $\overline{DQSU}$ (×16) use $V_{IH}/V_{IL.DQ.AC}$ of DQs and V_{REFDQ}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
5) Clock: use $V_{IL.CA.AC}$ for $V_{IL.AC}$. Strobe: use $V_{IL.DQ.AC}$ for $V_{IL.AC}$.

TABLE 19
Allowed Time Before Ringback (t_{DVAC}) for CLK - $\overline{CLK}$ and DQS - $\overline{DQS}$

Slew Rate [V/ns]	t_{DVAC} [ps] @ |$V_{IH/IL.DIFF.AC}$| = 350mV		t_{DVAC} [ps] @ |$V_{IH/IL.DIFF.AC}$| = 300mV	
	Min.	Max.	Min.	Max.
> 4.0	75	—	175	—
4.0	57	—	170	—
3.0	50	—	167	—
2.0	38	—	163	—
1.8	34	—	162	—
1.6	29	—	161	—
1.4	22	—	159	—
1.2	13	—	155	—
1.0	0	—	150	—
<1.0	0	—	150	—

Single-Ended Requirements for Differential Signals

Each individual component of a differential signal (for ×4, ×8: CK, DQS, $\overline{CK}$, $\overline{DQS}$, for ×16: CK, DQSL, DQSU, $\overline{CK}$, $\overline{DQSL}$, $\overline{DQSU}$) has also to comply with certain requirements for single-ended signals. CK and $\overline{CK}$ have to approximately reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately equal to the AC-levels ($V_{IH.CA.AC}$ / $V_{IL.CA.AC}$) for ADD/CMD signals) in every half-cycle. DQS, $\overline{DQS}$ (×4, ×8) and DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ (×16), respectively, have to reach $V_{SEH.MIN}$ / $V_{SEL.MAX}$ (approximately the AC-levels ($V_{IH.DQ.AC}$ / $V_{IL.DQ.AC}$) for DQ signals) in every half-cycle preceeding and following a valid transition. Note that the applicable AC-levels for ADD/CMD and DQs might be different per speed-bin etc. E.g. if $V_{IH.CA.AC150}$ / $V_{IL.CA.AC150}$ is used for ADD/CMD signals, then

these AC-levels apply also for the single-ended signals CK and $\overline{CK}$.

Note that while ADD/CMD and DQ signal requirements are with respect to V_{REF}, the single-ended components of differential signals have a requirement with respect to $V_{DD}/2$; this is nominally the same. The transition of single-ended signals through the AC-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL.MAX}$, $V_{SEH.MIN}$ has no bearing on timing, but adds a restriction on the common mode charateristics of these signals.

TABLE 20
Each Single-Ended Levels for CK, DQS, DQSL, DQSU, $\overline{CK}$, $\overline{DQS}$, $\overline{DQSL}$ or $\overline{DQSU}$

Parameter	Symbol	DDR3–800, DDR3–1066, DDR3–1333, DDR3–1600		Unit	Note
		Min.	Max.		
Single-ended high-level for strobes	V_{SEH}	$(V_{DD}/2)$ + 0.175	See [1]	V	2)3)
Single-ended high-level for CK, $\overline{CK}$	V_{SEH}	$(V_{DD}/2)$ + 0.175	See [1]	V	
Single-ended low-level for strobes	V_{SEL}	See [1]	$(V_{DD}/2)$ - 0.175	V	
Single-ended low-level for CK, $\overline{CK}$	V_{SEL}	See [1]	$(V_{DD}/2)$ - 0.175	V	

1) These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$ need to be within the respective limits ($V_{IH.DC.MAX}$, $V_{IL.DC.MIN}$) for single-ended signals as well as the limitations for overshoot and undershoot.

2) For CK, $\overline{CK}$ use $V_{IH.CA.AC}/V_{IL.CA.AC}$ of ADD/CMD; for strobes (DQS, $\overline{DQS}$, DQSL, $\overline{DQSL}$, DQSU, $\overline{DQSU}$) use $V_{IH.DQ.AC}/V_{IL.DQ.AC}$ of DQs.

3) $V_{IH.DQ.AC}/V_{IL.DQ.AC}$ for DQs is based on V_{REFDQ}; $V_{IH.CA.AC}/V_{IL.CA.AC}$ for ADD/CMD is based on V_{REFCA}; if a reduced AC-high or ac-low level is used for a signal group, then the reduced level applies also here.

TABLE 21
Cross Point Voltage for Differential Input Signals (CK, DQS)

Symbol	Parameter	DDR3–800, DDR3–1066, DDR3–1333, DDR3–1600		Unit	Note
		Min.	Max.		
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK - $\overline{CK}$	–150	150	mV	
		–175	175	mV	1)
V_{IX}	Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS -$\overline{DQS}$	–150	150	mV	

1) Extended range for V_{IX} is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing V_{SEL}/V_{SEH} (see **Single-Ended Requirements for Differential Signals**) of at least $V_{DD}/2$ +/-250 mV and if the differential slew rate of CK - $\overline{CK}$ is larger than 3 V/ns.

3.4.2 DC and AC Output Measurements Levels

TABLE 22
DC and AC Output Levels for Single-Ended Signals

Parameter	Symbol	Value	Unit	Note
DC output high measurement level (for output impedance measurement)	$V_{OH.DC}$	$0.8 \times V_{DDQ}$	V	
DC output mid measurement level (for output impedance measurement)	$V_{OM.DC}$	$0.5 \times V_{DDQ}$	V	
DC output low measurement level (for output impedance measurement)	$V_{OL.DC}$	$0.2 \times V_{DDQ}$	V	
AC output high measurement level (for output slew rate)	$V_{OH.AC}$	$V_{TT} + 0.1 \times V_{DDQ}$	V	1)
AC output low measurement level (for output slew rate)	$V_{OL.AC}$	$V_{TT} - 0.1 \times V_{DDQ}$	V	1)

1) Background: the swing of ± $0.1 \times V_{DDQ}$ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ} / 2$.

TABLE 23
AC Output Levels for Differential Signals

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
AC differential output high measurement level (for output slew rate)	$V_{OH.DIFF.AC}$	$+0.2 \times V_{DDQ}$		V	1)
AC differential output low measurement level (for output slew rate)	$V_{OL.DIFF.AC}$	$–0.2 \times V_{DDQ}$		V	1)
Deviation of the output cross pointvoltage from the termination voltage	V_{OX}	-100	100	mV	2)

1) Background: the swing of ± $0.2 \times V_{DDQ}$ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to $V_{TT} = V_{DDQ} / 2$ at each of the differential outputs.

2) With an effective test load of 25 Ω to $V_{TT} = V_{DDQ}/2$ at each of the differential outputs (see chapter **Chapter 3.3**, **Interface Test Conditions**).

3.5 ODT DC Impedance and Mid-Level Characteristics

Table 24 provides the ODT DC impedance and mid-level characteristics.

TABLE 24
ODT DC Impedance and Mid-Level Characteristics

Symbol	Description	V_{OUT} Condition	Min.	Nom.	Max.	Unit	Note
R_{TT120}	R_{TT} effective = 120 Ω	$V_{IL.AC}$ and $V_{IH.AC}$	0.9	1.0	1.6	$R_{ZQ}/2$	1)2)3)4)
R_{TT60}	R_{TT} effective = 60 Ω		0.9	1.0	1.6	$R_{ZQ}/4$	1)2)3)4)
R_{TT40}	R_{TT} effective = 40 Ω		0.9	1.0	1.6	$R_{ZQ}/6$	1)2)3)4)
R_{TT30}	R_{TT} effective = 30 Ω		0.9	1.0	1.6	$R_{ZQ}/8$	1)2)3)4)
R_{TT20}	R_{TT} effective = 20 Ω		0.9	1.0	1.6	$R_{ZQ}/12$	1)2)3)4)
ΔV_M	Deviation of V_M with respect to V_{DDQ} / 2	floating	–5	—	+5	%	1)2)3)4)5)

1) With R_{ZQ} = 240 Ω.
2) Measurement definition for R_{TT} : Apply $V_{IH.AC}$ and $V_{IL.AC}$ to test ball separately, then measure current $I(V_{IH.AC})$ and $I(V_{IL.AC})$ respectively. $R_{TT} = [V_{IH.AC} - V_{IL.AC}] / [I(V_{IH.AC}) - I(V_{IL.AC})]$
3) The tolerance limits are specified after calibration with stable voltage and temperature. For the behaviour of the tolerance limits if temperature or voltage changes after calibration, see the **ODT DC Impedance Sensitivity on Temperature and Voltage Drifts**.
4) The tolerance limits are specified under the condition that $V_{DDQ} = V_{DD}$ and that $V_{SSQ} = V_{SS}$.
5) Measurement Definition for ΔV_M: Measure voltage (V_M) at test ball (midpoint) with no load: $\Delta V_M = (2 \times V_M / V_{DDQ} - 1) \times 100\%$

3.6 ODT DC Impedance Sensitivity on Temperature and Voltage Drifts

If temperature and/or voltage change after calibration, the tolerance limits widen for R_{TT} according to the following tables. The following definitions are used:

$\Delta T = T - T$ (at calibration)

$\Delta V = V_{DDQ} - V_{DDQ}$ (at calibration)

$V_{DD} = V_{DDQ}$

TABLE 25
ODT DC Impedance after proper IO Calibration and Voltage/Temperature Drift

Symbol	Value		Unit	Note
	Min.	Max.		
R_{TT}	0.9 - dR_{TT}dT × |ΔT| - dR_{TT}dV × |ΔV|	1.6 + dR_{TT}dT × |ΔT| + dR_{TT}dV × |ΔV|	$R_{ZQ} / TISF_{RTT}$	1)

1) $TISF_{RTT}$: Termination Impedance Scaling Factor for R_{TT}:
$TISF_{RTT}$ = 12 for R_{TT020}
$TISF_{RTT}$ = 8 for R_{TT030}
$TISF_{RTT}$ = 6 for R_{TT040}
$TISF_{RTT}$ = 4 for R_{TT060}
$TISF_{RTT}$ = 2 for R_{TT120}

TABLE 26
OTD DC Impedance Sensitivity Parameters

Symbol	Value		Unit	Note
	Min.	Max.		
$dR_{TT}dT$	0	1.5	%/°C	1)
$dR_{TT}dV$	0	0.15	%/mV	

1) These parameters may not be subject to production test. They are verified by design and characterization.

3.7 Output Slew Rate Definition and Requirements

The slew rate definition depends if the signal is single-ended or differential. For the relevant AC output reference levels see **Chapter 3.4.2**.

3.7.1 Output Slew Rates

TABLE 27
Output Slew Rates

Parameter	Symbol	DDR3–800, DDR3–1066, DDR3–1333, DDR3–1600		Unit	Note
		Min.	Max.		
Single-ended Output Slew Rate	SRQse	2.5	5 1)	V / ns	2)3)
Differential Output Slew Rate	SRQdiff	5	12	V / ns	

1) In two cases, a maximum slew rate of 6 V/ns applies for a single DQ signal within a byte lane.
- **Case 1** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e they stay at either high or low).
- **Case 2** is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 5 V/ns applies.

2) For $R_{ON} = R_{ZQ}/7$ settings only.

3) Background for Symbol Nomenclature: SR: Slew Rate; Q: Query Output; se: single-ended; diff: differential

3.8 Interface Capacitance

Definition and values for interface capacitances are provided in the following table.

TABLE 28
Interface Capacitance Values

Parameter	Signals	Symbol	DDR3–800		DDR3–1066		DDR3–1333		DDR3–1600		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Input/Output Capacitance	DQ, DM, DQS, $\overline{\text{DQS}}$	C_{IO}	1.5	3.0	1.5	3.0	1.5	2.5	1.5	2.3	pF	1)2)3)
Input Capacitance	CK, $\overline{\text{CK}}$	C_{CK}	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF	2)3)
Delta of Input Capacitance	CK, $\overline{\text{CK}}$	C_{DCK}	0	0.15	0	0.15	0	0.15	0	0.15	pF	2)3)4)
Delta of Input/Output Capacitance of DQS balls	DQS, $\overline{\text{DQS}}$	C_{DDQS}	0	0.2	0	0.2	0	0.15	0	0.15	pF	2)3)5)
Input Capacitance	All other input-only pins	C_{I}	0.75	1.5	0.75	1.5	0.75	1.3	0.75	1.3	pF	2)3)6)
Delta of Input Capacitance	All CTRL input-only pins	$C_{DI.CTRL}$	–0.5	0.3	–0.5	0.3	–0.4	0.2	–0.4	0.2	pF	2)3)7)8)
Delta of Input Capacitance	All ADD and CMD input-only pins	$C_{DI.ADD\_CMD}$	–0.5	0.5	–0.5	0.5	–0.4	0.4	–0.4	0.4	pF	2)3)9) 10)
Delta of Input/Output Capacitance	DQ, DM, DQS, $\overline{\text{DQS}}$	C_{DIO}	–0.5	0.3	–0.5	0.3	–0.5	0.3	–0.5	0.3	pF	2)3)11)
ZQ Capacitance	ZQ	C_{ZQ}	–	3	–	3	–	3	–	3	pF	12)

1) Although the DM signal has different function, the loading matches DQ and DQS
2) This parameter is not subject to production test. It is verified by design and characterization. Capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD}, V_{DDQ}, V_{SS}, V_{SSQ} applied and all other balls floating (except the ball under test, CKE, $\overline{\text{RESET}}$ and ODT as necessary). V_{DD} = V_{DDQ} = 1.5 V, V_{BIAS} = V_{DD}/2 and on-die termination off
3) This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4) Absolute value of C_{CK} - $C_{CK\#}$
5) Absolute value of $C_{IO.DQS}$ - $C_{IO.DQS\#}$
6) C_{I} applies to ODT, $\overline{\text{CS}}$, CKE, A[13:0] (×4, ×8) or A[12:0] (×16), BA[2:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$
7) C_{DI_CTRL} applies to ODT, $\overline{\text{CS}}$ and CKE
8) C_{DI_CTRL} = $C_{I.CTRL}$ - 0.5 × (C_{CK} + $C_{CK\#}$)
9) $C_{DI\_ADD\_CMD}$ applies to A[A13:0] (×4, ×8) or A[A12:0] (×16), BA[2:0], BA[2:0], $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$
10) $C_{DI\_ADD\_CMD}$ = $C_{I.ADD,CMD}$ - 0.5 × ($C_{I.CK}$ + $C_{I.CK\#}$)
11) C_{DIO} = $C_{IO.DQ,DM}$ - 0.5 × ($C_{IO.DQS}$ + $C_{IO.DQS\#}$)
12) Maximum external load capacitance on ZQ signal: 5 pF

3.9 Overshoot and Undershoot Specification

TABLE 29
AC Overshoot / Undershoot Specification for Address and Control Signals

Parameter	DDR3–800	DDR3–1066	DDR3–1333	DDR3–1600	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DD}	0.67	0.5	0.4	0.33	V × ns	1)
Maximum undershoot area below V_{SS}	0.67	0.5	0.4	0.33	V × ns	1)

1) Applies for the following signals: A[15:0], BA[3:0], $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE and ODT

FIGURE 5
AC Overshoot / Undershoot Definitions for Address and Control Signals

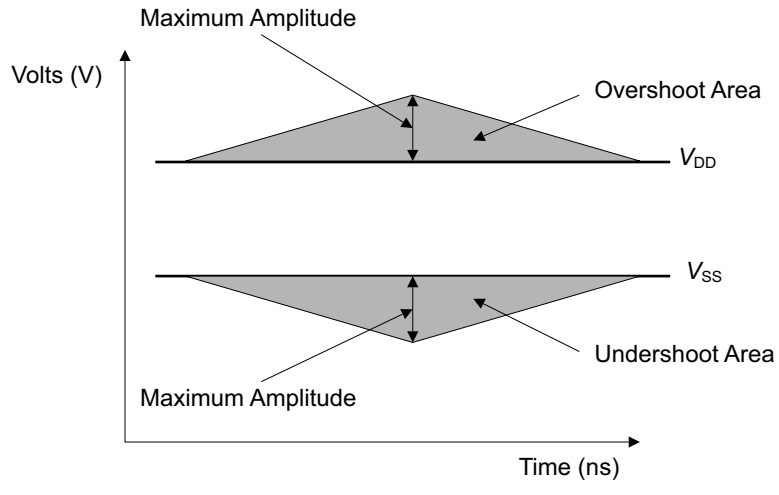
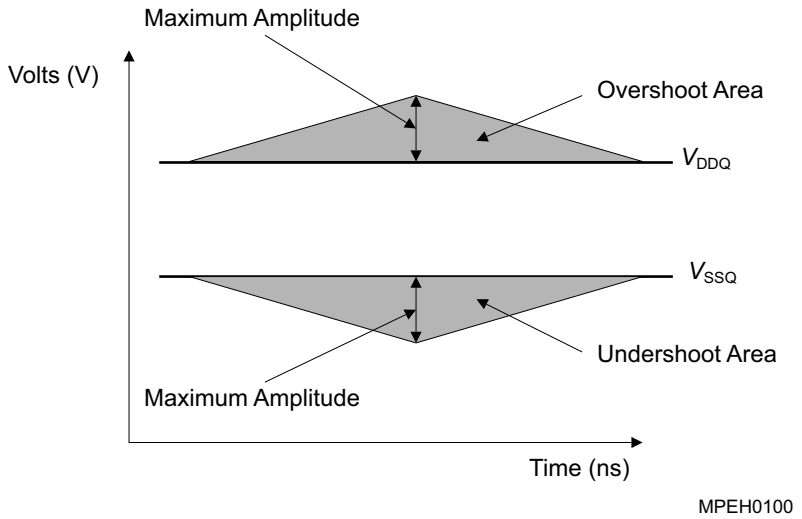


TABLE 30
AC Overshoot / Undershoot Specification for Clock, Data, Strobe and Mask Signals

Parameter	DDR3–800	DDR3–1066	DDR3–1333	DDR3–1600	Unit	Note
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	V	1)
Maximum peak amplitude allowed for undershoot area	0.4	0.4	0.4	0.4	V	1)
Maximum overshoot area above V_{DDQ}	0.25	0.19	0.15	0.13	V × ns	1)
Maximum undershoot area below V_{SSQ}	0.25	0.19	0.15	0.13	V × ns	1)

1) Applies for CK, $\overline{CK}$, DQ, DQS, $\overline{DQS}$ & DM

FIGURE 6
AC Overshoot / Undershoot Definitions for Clock, Data, Strobe and Mask Signals



4 Speed Bins and Timing Parameters

AC timings are provided with CK/$\overline{CK}$ and DQS/$\overline{DQS}$ differential slew rate of 2.0 V/ns. Timings are further provided for calibrated OCD drive strength. The CK/$\overline{CK}$ input reference level (for timing referenced to CK / $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross. The DQS/$\overline{DQS}$ reference level (for timing referenced to DQS/$\overline{DQS}$) is the point at which DQS and $\overline{DQS}$ cross. Inputs are not recognized as valid until V_{REF} stabilizes. During the period before $V_{REF.CA}$ and V_{REFDQ} stabilizes, CKE = 0.2 x V_{DDQ} is recognized as low. The output timing reference voltage level is V_{TT}. For details of all relevant AC timing parameters see the QIMONDA DDR3 component datasheet.

4.1 Speed Bins

The following tables show DDR3 speed bins and relevant timing parameters. Other timing parameters are provided in the following chapter.

The absolute specification for all speed bins is T_{OPER} and V_{DD} = V_{DDQ} = 1.5 V +/-0.075 V. In addition the following general notes apply.

General Notes for Speed Bins:

- The CL setting and CWL setting result in $t_{CK.AVG.MIN}$ and $t_{CK.AVG.MAX}$ requirements. When making a selection of $t_{CK.AVG}$, both need to be fulfiled: Requirements from CL setting as well as requirements from CWL setting
- $t_{CK.AVG.MIN}$ limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be provided. An application should use the next smaller standard $t_{CK.AVG}$ value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK.AVG}$ [ns], rounding up to the next 'Supported CL'
- $t_{CK.AVG.MAX}$ limits: Calculate $t_{CK.AVG}$ = $t_{AA.MAX}$ / CLSELECTED and round the resulting $t_{CK.AVG}$ down to the next valid speed bin limit (i.e. 3.3 ns or 2.5 ns or 1.875 ns or 1.25 ns). This result is $t_{CK.AVG.MAX}$ corresponding to CLSELECTED
- 'Reserved' settings are not allowed. User must program a different value
- Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization
- Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the tables which are not subject to Production Tests but verified by Design/Characterization

TABLE 31
DDR3-800 Speed Bins and Operating Conditions

Speed Bin		DDR3-800D		DDR3-800E		Unit	Note
CL-n_{RCD}-n_{RP}		5-5-5		6-6-6			
QAG Partnumber Extension		-08D		-08E			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	12.5	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.5	—	15.0	—	ns	1)
PRE command period	t_{RP}	12.5	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	50.0	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6		6		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5		5		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 32
DDR3-1066 Speed Bins and Operating Conditions

Speed Bin		DDR3-1066E		DDR3-1066F		DDR3-1066G		Unit	Note
CL-n_{RCD}-n_{RP}		6-6-6		7-7-7		8-8-8			
QAG Partnumber Extension		-10E		-10F		-10G			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	11.25	20.0	13.125	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	11.25	—	13.125	—	15.0	—	ns	1)
PRE command period	t_{RP}	11.25	—	13.125	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.75	—	50.625	—	52.5	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8		6, 7, 8		6, 8		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6		5, 6		5, 6		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 33
DDR3-1333 Speed Bins and Operating Conditions

Speed Bin		DDR3-1333G		DDR3-1333H		DDR3-1333J		Unit	Note
CL-n_{RCD}-n_{RP}		8-8-8		9-9-9		10-10-10			
QAG Partnumber Extension		-13G		-13H		-13J			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	12.0	20.0	13.5	20.0	15.0	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	12.0	—	13.5	—	15.0	—	ns	1)
PRE command period	t_{RP}	12.0	—	13.5	—	15.0	—	ns	1)
ACT to ACT or REF command period	t_{RC}	48.0	—	49.5	—	51.0	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10		6, 8, 9, 10		6, 8, 10		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7		5, 6, 7		5, 6, 7		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	1.5	1.875	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

TABLE 34
DDR3-1600 Speed Bins and Operating Conditions

Speed Bin		DDR3-1600H		DDR3-1600J		DDR3-1600K		Unit	Note
CL-n_{RCD}-n_{RP}		9-9-9		10-10-10		11-11-11			
QAG Partnumber Extension		-16H		-16J		-16K			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Internal read command to first data	t_{AA}	11.25	20.0	12.5	20.0	13.75	20.0	ns	1)
ACT to internal read or write delay time	t_{RCD}	11.25	—	12.5	—	13.75	—	ns	1)
PRE command period	t_{RP}	11.25	—	12.5	—	13.75	—	ns	1)
ACT to ACT or REF command period	t_{RC}	46.25	—	47.5	—	48.75	—	ns	1)
Supported CL Settings	Sup_CL	5, 6, 7, 8, 9, 10, 11		5, 6, 7, 8, 9, 10, 11		6, 8, 10, 11		n_{CK}	1)
Supported CWL Settings	Sup_CWL	5, 6, 7, 8		5, 6, 7, 8		5, 6, 7, 8		n_{CK}	1)
Average Clock Period with CL = 5; CWL = 5	$t_{CK.AVG.CL05.CWL05}$	2.5	3.3	2.5	3.3	RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 6	$t_{CK.AVG.CL05.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 7	$t_{CK.AVG.CL05.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 5; CWL = 8	$t_{CK.AVG.CL05.CWL08}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 5	$t_{CK.AVG.CL06.CWL05}$	2.5	3.3	2.5	3.3	2.5	3.3	ns	1)2)
Average Clock Period with CL = 6; CWL = 6	$t_{CK.AVG.CL06.CWL06}$	1.875	2.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 7	$t_{CK.AVG.CL06.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 6; CWL = 8	$t_{CK.AVG.CL06.CWL08}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 5	$t_{CK.AVG.CL07.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 6	$t_{CK.AVG.CL07.CWL06}$	1.875	2.5	1.875	2.5	RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 7	$t_{CK.AVG.CL07.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 7; CWL = 8	$t_{CK.AVG.CL07.CWL08}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 5	$t_{CK.AVG.CL08.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 6	$t_{CK.AVG.CL08.CWL06}$	1.875	2.5	1.875	2.5	1.875	2.5	ns	1)2)
Average Clock Period with CL = 8; CWL = 7	$t_{CK.AVG.CL08.CWL07}$	1.5	1.875	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 8; CWL = 8	$t_{CK.AVG.CL08.CWL08}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 5	$t_{CK.AVG.CL09.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 6	$t_{CK.AVG.CL09.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 7	$t_{CK.AVG.CL09.CWL07}$	1.5	1.875	1.5	1.875	RESERVED		ns	1)2)
Average Clock Period with CL = 9; CWL = 8	$t_{CK.AVG.CL09.CWL08}$	1.25	1.5	RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 5	$t_{CK.AVG.CL10.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 6	$t_{CK.AVG.CL10.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 10; CWL = 7	$t_{CK.AVG.CL10.CWL07}$	1.5	1.875	1.5	1.875	1.5	1.875	ns	1)2)
Average Clock Period with CL = 10; CWL = 8	$t_{CK.AVG.CL10.CWL08}$	1.25	1.5	1.25	1.5	RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 5	$t_{CK.AVG.CL11.CWL05}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 6	$t_{CK.AVG.CL11.CWL06}$	RESERVED		RESERVED		RESERVED		ns	1)2)

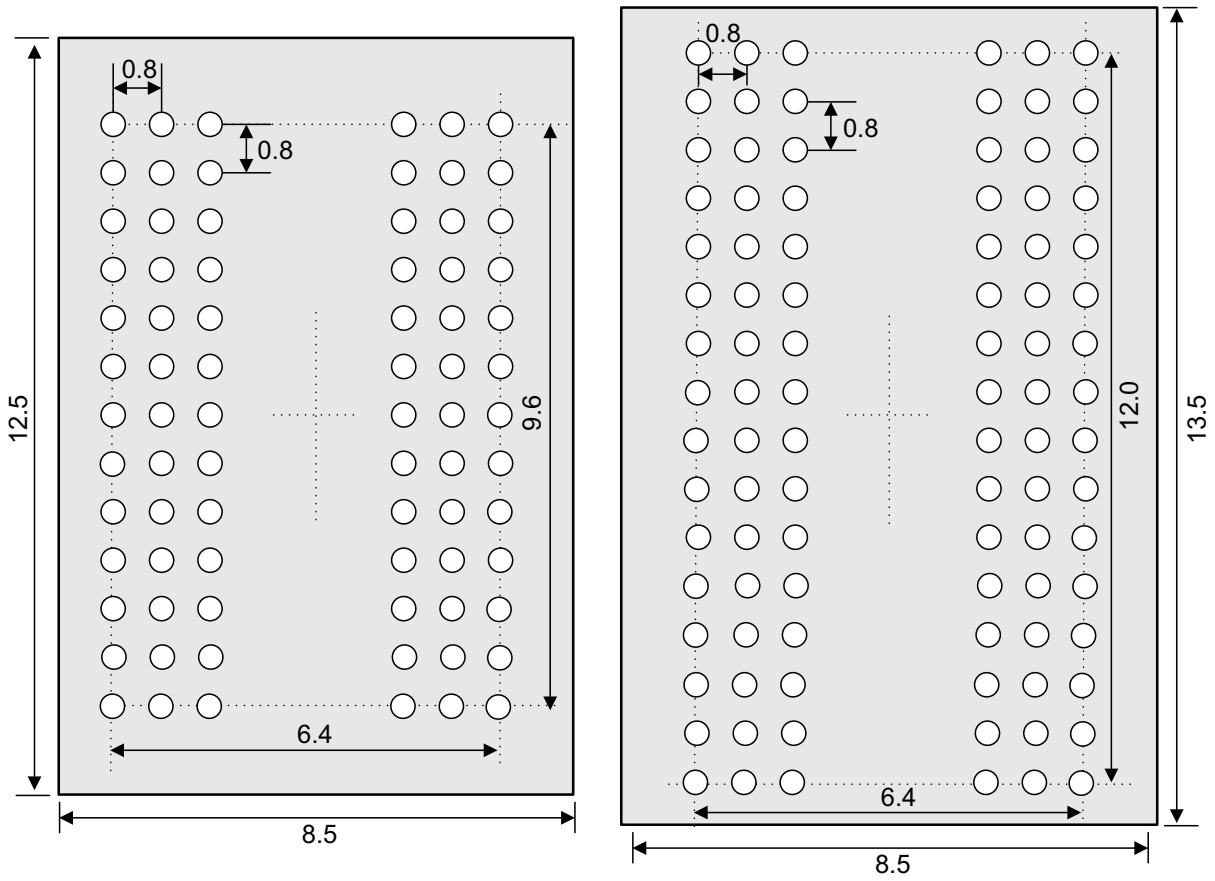
Speed Bin		DDR3-1600H		DDR3-1600J		DDR3-1600K		Unit	Note
CL-n_{RCD}-n_{RP}		9-9-9		10-10-10		11-11-11			
QAG Partnumber Extension		-16H		-16J		-16K			
Parameter	**Symbol**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**		
Average Clock Period with CL = 11; CWL = 7	$t_{CK.AVG.CL11.CWL07}$	RESERVED		RESERVED		RESERVED		ns	1)2)
Average Clock Period with CL = 11; CWL = 8	$t_{CK.AVG.CL11.CWL08}$	1.25	1.5	1.25	1.5	1.25	1.5	ns	1)2)

1) Please refer to "General Notes for Speed Bins" at beginning of this chapter.
2) Max. limits are exclusive. E.g. if $t_{CK.AVG.MAX}$ value is 2.5 ns, $t_{CK.AVG}$ needs to be < 2.5 ns.

5 Package Outline

This chapter contains the package dimension figures.

FIGURE 7
Package Outlines. Left: PG-TFBGA-78 (x4/x8). Right: PG-TFBGA-96 (x16)



6 Product Type Nomenclature

For reference the applicable Qimonda DDR3 component nomenclature is listed in this chapter.

TABLE 35
Example for Nomenclature Fields

Example for	Field Number											
	1	2	3	4	5	6	7	8	9	10	11	12
DDR3 SDRAM Component	ID	SH	1G	—	0	2	A1	F1	C	—	08	E

TABLE 36
DDR3 SDRAM Nomenclature

Field	Description	Value	Coding
1	Qimonda SDRAM Component Prefix	ID	Qimonda SDRAM
2	SDRAM Technology	SH	Standard DDR3
3	Component Density	512	512 Mbit
		1G	1 GBit
		2G	2 GBit
		4G	4 GBit
4	Module Type / ECC Support	—	No ECC support on SDRAM level
5	Number of Chip Select	0	1 Chip Select (2^0)
		1	2 Chip Select (2^1)
6	Number of DQs	2	4 DQ lines (2^2)
		3	8 DQ lines (2^3)
		4	16 DQ lines (2^4)
		5	32 DQ lines (2^5)
7	Die Revision	A1	First Die
8	Package	F1	Planar FBGA, lead- and halogen-free
		F2	Dual Die FBGA, lead- and halogen-free
9	Temperature Range	C	Commercial (0 °C - 95 °C)
10	Reserved For Future Use	—	RFU
11	Band Width Per DQ	08	DDR3–800 = 800 Mbit per ball per second, t_{CK} = 2.5 ns
		10	DDR3–1066 = 1066 Mbit per ball per second, t_{CK} = 1.875 ns
		13	DDR3–1333 = 1333 Mbit per ball per second, t_{CK} = 1.5 ns
		16	DDR3–1600 = 1600 Mbit per ball per second, t_{CK} = 1.25 ns

Field	Description	Value	Coding
12	Latencies	D	CL–RCD–RP = 5–5–5
		E	CL–RCD–RP = 6–6–6
		F	CL–RCD–RP = 7–7–7
		G	CL–RCD–RP = 8–8–8
		H	CL–RCD–RP = 9–9–9
		J	CL–RCD–RP = 10–10–10
		K	CL–RCD–RP = 11–11–11

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