ML4535

Area Detection Based Hybrid Servo Demodulator

GENERAL DESCRIPTION

The ML4535 is a bipolar monolithic hybrid servo circuit that provides area measurement demodulation of both the continuous servo surface (dedicated servo) and the sectored servo data (embedded servo) information in a high end disk drive. It operates on a single +5V supply and is intended to interface to a moderate speed, successive approximation ADC, with multiplexed inputs and sample and holds, like the ML2377 family.

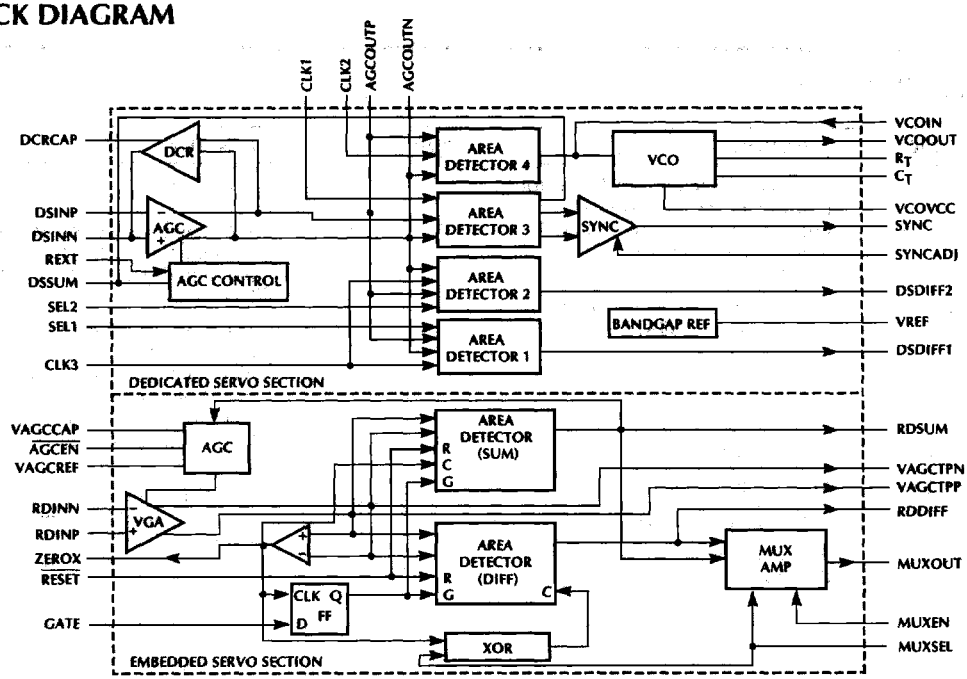
The area detectors are designed to minimize the pipeline transport delay while accurately quantizing the area of servo bursts in high speed servo systems. The data surface (embedded) servo demodulator section consists of Sum and Difference area detectors along with an AGC control loop. The continuous (dedicated) servo demodulator section consists of a variable gain amplifier, variable frequency oscillator and four synchronous area detectors.

The ML4535 provides a high level of integration for designing the complex Hybrid Servo systems becoming popular in disk drives requiring very high bit and track densities, in excess of 3500 TPI.

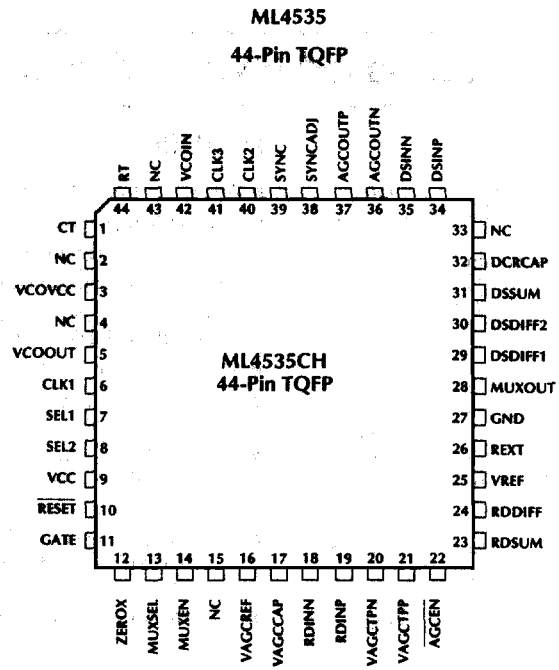
FEATURES

- Allows for area detection of back-to-back bursts
- 2% non-linearity over the input signal range
- Single +5 volt operation
- Internal 2.5V bandgap reference with reference output
- Separate AGC control loop for data surface and servo surface demodulator sections.
- Data surface amplitude control self contained on chip
- Data surface demodulator has muxed/selectable (A-B) and (A+B) outputs.
- Four synchronous area detectors onboard for implementing the continuous servo demodulator.
- Threshold based Sync detector
- Servo surface area detectors (1 & 2) have current output and can be individually selected using the SEL# pins.
- Available in 44-pin TQFP package

BLOCK DIAGRAM



PIN CONNECTION



PIN DESCRIPTION

PIN#	NAME	FUNCTION
1 44	CT RT	Pins to connect a resistor/capacitor network for setting the center frequency of the internal VCO; R from RT to CT, C from CT to VCOVCC
2 4 15 43 33	NC	No connects, It is recommended to Connect these to GND
3	VCOVCC	+ 5V supply for PLL
5	VCOOUT	VCO clock output
6	CLK1	Clock for Area Detector 3 (AGC)
7	SEL1	Active high select signal for area detector 1
8	SEL2	Active high select signal for area detector 2
9	VCC	+ 5V supply (± 5%)
10	$\overline{\text{RESET}}$	Asserting this input pin resets the Area Detector (DIFF) to VREF and the Area Detector (SUM) to VREF/2 (active low)
11	GATE	Asserting this pin defines the SUM and DIFF area detect windows, to measure the area under the curve of the VGA output. This signal is resynchronized internally to ZEROX before application to the area detectors.
12	ZEROX	This is the logic signal output of the carrier comparator, nominally a square wave having transitions coinciding with zero crossings of the VGA output.

PIN DESCRIPTION (Continued)

PIN#	NAME	FUNCTION
13	MUXSEL	Asserting this pin inverts the carrier input of the Difference (A-B) area detector. MUXSEL should be asserted throughout the B burst of the A/B burst pair, to implement (A-B). While this pin is asserted, the Difference (A-B) area detector integrates the B burst in a direction opposite to that in which A is integrated, thus realizing the (A-B) operation. Carrier polarity in the (A+B) area detector is not affected by the state of the MUXEN pin. This pin along with the MUXEN pin, also selects the multiplexer output.
14	MUXEN	This pin in conjunction with the MUXSEL pin governs the multiplexer channel selection as follows: MUXSEL MUXEN MUXOUT X 0 VREF 0 1 Difference (A-B) 1 1 Sum (A+B)
16	VAGCREF	AGC voltage reference
17	VAGCCAP	AGC Loop Filter/Hold Capacitor
18 19	RDINN RDINP	Differential input to VGA from Data surface (embedded servo). Inputs must be AC coupled.
20 21	VAGCTPN VAGCTPP	Test points connected through isolation resistors to the output of the VGA. Max $2V_{p-p}$ differential. Typically around 1V.
22	$\overline{AGCEN}$	AGC enable pin, defines area detect window (active low signal)

PIN#	NAME	FUNCTION
23	RDSUM	The SUM area detector integrating capacitor is connected here.
24	RDDIFF	The DIFF area detector integrating capacitor is connected here.
25	VREF	2.5V Bandgap reference output
26	REXT	A 15.8k (1%) resistor to GND sets the transconductance of all Area Detectors current outputs
27	GND	Ground pin
28	MUXOUT	Output of the multiplexer with DIFF or SUM output
29	DSDIFF1	Area Detector #1 (A,B) or the Normal output
30	DSDIFF2	Area Detector #2 (C,D) or the Quad output
31	DSSUM	Pin for connecting the filter for the AGC loop (Dedicated surface)
32	DCRCAP	DC Restore capacitor
34 35	DSINP DSINN	Differential signal input from Continuous (dedicated) servo surface. Inputs must be AC coupled
36 37	AGCOUTN AGCOUTP	Test points connected through isolation resistors to differential output of servo surface AGC.
38	SYNCADJ	External adjustment of sync threshold below or above the internal setting.
39	SYNC	Servo frame sync signal output
40	CLK2	Clock for Area Detector 4, (PLL)
41	CLK3	Clock for Area Detectors 1 & 2 (POS)
42	VCOIN	Pin for connecting the loop filter for the PLL or external drive

ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage (VCC) ..... –0.3 to +7 VDC
Package Dimension, TA = 25°C
(board mount) ..... TBD mW
Package Lead Temperature
Soldering (10 sec) ..... 260°C
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C
Storage Temperature (tstg) ..... –65 to +150°C

OPERATING CONDITIONS

DC Supply Voltage (VCC) ..... 5+/–5% VDC
Temperature Range ..... 0 to +70°C
Operating Junction Temperature (Tj) ..... +25 to +125 °C

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
DC CHARACTERISTICS					
ICC Supply Current	VAGCCAP = 4.0V	60	89	110	mA
Bandgap Reference voltage, VREF		2.4	2.52	2.60	V
VIH	For CLK1, CLK2, CLK3 GATE, MUXEN, MUXSEL, AGCEN, SEL1, SEL2			2.0	V
VIL	For CLK1, CLK2, CLK3 GATE, MUXEN, MUXSEL, AGCEN, SEL1, SEL2	0.8			V
IIH	For CLK1, CLK2, CLK3 GATE, MUXEN, RESET MUXSEL, AGCEN, SEL1, SEL2	–40	–0.2	+40	µA
IIL	For CLK1, CLK2, CLK3 GATE, MUXEN, RESET MUXSEL, AGCEN, SEL1, SEL2	–400	–2	10	µA
AGC (for dedicated servo)					
DSINPDC, DSINNDC	open	2.4	2.5	2.6	V
AvAGC min Voltage gain from input to test point	DSSUM = 4.0V, Measure DSDIFF1 DSINP – DSINN = 0.5V		0.2	0.4	V/V
AvAGC max	DSSUM = 1.0V DSINP – DSINN = 20mV	75	120		V/V
DCRHIGH (DCR CAP VOLTAGE)	DSSUM = 1.0V DSINP – DSINN = 20mV	3.0	3.9		V
DCRLOW (DCR CAP VOLTAGE)	DSSUM = 1.0V DSINN – DSINP = 20mV	2.3	2.5	2.7	V
DSOFFSET	DSINP – DSINN = 0	–1	0.0001	+1	V
AREA DETECTOR 1 and 2					
DSDIFF HI 1	SEL1, SEL2 = VIH	VCC – 1.0	VCC – 0.5	VCC	V
DSDIFF LO 2	DSINP – DSINN = 0.1 DSSUM = 1V, CLK3=VIH		0.2	1.0	V
DSDIFF LO 1	CLK3 = VIL		0.2	1.0	V
DSDIFF HI 2		VCC – 1.0	VCC – 0.5	VCC	V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
AREA DETECTOR 1 and 2 (continued)					
DSDIFF HI R1	DSINN – DSINP = 0.1	VCC – 1.0	VCC – 0.5	VCC	V
DSDIFF LO R2	CLK3 = V_{IL}		0.2	1.0	V
DSDIFF LO R1	DSINN – DSINP = 0.1		0.2	1.0	V
DSDIFF HI R2	CLK3 = V_{IH}	VCC – 1.0	VCC – 0.5	VCC	V
IDSDIFF HI IDSDIFF LO	DSINP – DSINN = 0.1 DSINP – DSINN = –0.1	–200 100	–133 133	–100 200	µA µA
IDSDIFF1 IDSOFF2	SEL1 = V_{IL} SEL2 = V_{IL}	–1 1	–0.005 0.001	1 –1	µA µA
AREA DETECTOR 3					
SYNC LO	CLK1 = V_{IH}, I_{IL} = 1.6 mA DSSUM = 1.0V DSINN – DSINP = 0.1		0.35	0.5	V
SYNC HI	CLK1 = V_{IH}, I_{IH} = –0.4 mA DSSUM = 1.0V DSINN – DSINP = 0.1	VCC – 2.1	VCC – 0.8	VCC	V
$V_{SYNCADJ}$	$I_{SYNCADJ}$ = 0	0.1	0.18	0.5	V
I DSSUM OFF	DSINN – DSINP = 0V	15	35	70	µA
I DSSUM HI	CLK1= VIH, DSSUM = 1 V DSINP – DSINN = 0.1	–20	–83	–150	µA
I DSSUM LO	DSINN – DSINP = 0.1	100	186	250	µA
AREA DETECTOR 4, VCO					
I VCOIN HI	CLK2= VIH, DSSUM = 1 V DSINP – DSINN = 0.1V	60	136	200	µA
I VCOIN LO	CLK2 = VIL	–200	–135	–60	µA
VCO HI (V_{OH})	CT = 4.0V, VCOIN = 4.0V, I_{OH} = 0.4mA	2.3	2.6		V
VCO LO (V_{OL})	CT = 1.0V, VCOIN = 1.0V, I_{OL} = 1.6mA		0.25	0.5	V
RDINPDC, RDINNDC	open	2.3	2.5	2.7	V
V_{OH} ZEROX	RDINP – RDINN = 2.0V I_{OH} = –0.4 mA	VCC – 2.1	VCC – 0.7	VCC	V
V_{OL} ZEROX	RDINP – RDINN = 2.0V I_{OL} = 2.0 mA		0.36	0.5	V
V_{REXT}	R_{EXT} = 15.9K	2.2	2.48	2.8	V
AGC (for embedded servo)					
VAGCTP	RDINP – RDINN = 2.0 V VAGC = 1.0V	VCC – 1.5	VCC – 2.1	VCC – 2.7	V
Av VGA MIN	RDINP – RDINN = 1.0 V VAGC = 4.0V		0.3	0.5	V/V

ELECTRICAL CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
RESET LOGIC					
Av VGA MAX	RDINP – RDINN = 0.4 V VAGC = 1.0 V	2.0	2.7		V/V
VAGC BIAS	XAGC = 1.0 V	0	40	200	µA
IRESET SUM, DIFF	RESET = V_{IL}	50	100	200	µA
IOFF SUM, DIFF	RESET = V_{IH}	–100		100	nA
VSUM	RESET = V_{IL}	0.9	1.07	1.2	V
VDIFF	RESET = V_{IL}	2.0	2.13	2.3	V
I SUM, DIFF UNBAL	GATE = VIH, CLOCK VAGC 1X, 1 Vp-p swing	–40	0.4	40	µA
IDIFF UNBAL XOR	MUXSEL = VIH	–40		40	µA
I PEAK SUM	RDINP – RDINN = 1.0 V MUXSEL = VIH	–500	–377	–250	µA
I PEAK DIFF P	RDINP – RDINN = 1.0 V MUXSEL = VIH, VAGC = 1V	–500	–377	–250	µA
I PEAK DIFF XOR	RDINP – RDINN = 1.0 V MUXEN = VIH, VAGC = 1.0V	250	377	500	µA
VOHSUM, VOHDIFF	RDINP – RDINN = 1.0V	VCC – 1.0	VCC – 0.5	VCC	V
VOL DIFF, VOLSUM	RDINP – RDINN = 1.0V MUXSEL = VIH	0	0.2	1.0	V
IGATE	GATE = VIH, CLOCK 1X	–100	0	100	nA
MUXAMPLIFIER					
VOS MUXSUM	MUXSEL = MUXEN = VIL	0	5	16	V
VOS MUXDIFF	MUXSEL = VIH, VDIFF = 2.5V,	0	5	16	V
IBIASSUM DIFF	MUXEN = VIL SUM = DIFF = 2.5V	0	200	300	nA
VOHMUX	SUM = 3.9 V	VCC – 1.0	VCC – 0.9	VCC – 0.5	V
VOLMUX	DIFF = 0.95	0	0.9	1.0	V
INSINGMUX	VMUXOUT = VXX	1.5	1.86	2.5	mA
Amplifier settling time - tsmux	Rout = 604 ohms, Cout = 36 pF		0.4	1	µsec
Ileakage				10	nA
Linearity	0 to 1V input with VAGC such that AvVAGC = 1.0V	–5		5	%F.S

FUNCTIONAL DESCRIPTION

The ML4535 provides area measurement demodulation of both the continuous (dedicated) servo surface and the sectored (embedded) servo data on each of the data surfaces of a "hybrid" servo disk drive. It operates on a single +5V supply and is intended to interface to a moderate speed, successive approximation ADC with multiplexed inputs and sample and holds, like the ML2377. In a conventional peak detection based servo scheme, the attack rate of the peak detectors are inherently faster than the decay, high crest factor noise sensitivity is high and rectification must have a very low offset for it to be functionally correct. On the other hand area detection has much better noise rejection and is more tolerant of small AGC rectifier offsets. However it requires that the measurement period be an integer number of signal cycles. Hence when the timing requirements are satisfied, area detection is certainly more accurate than peak detection schemes.

DATA SURFACE OR EMBEDDED SERVO DEMODULATOR SECTION

The data surface (embedded) servo demodulator section of the ML4535 consists of a standalone AGC control loop so that the amplitude control function is self contained on the chip and two area detectors providing the sum (A+B) and difference (A–B) which are output through a mux amplifier.

Input Amplifier and AGC

The input amplifier and AGC circuit operate with differential inputs in the range of 0.25Vp–p to 2Vp–p, from the read channel filter's lowpass outputs. The input impedance of the RDIN inputs is approximately 2.3kΩ. The purpose of the AGC loop is to maintain a constant area detect value that correlates to the zero scale and full scale output values based upon the minimum and maximum burst value. The sensing for the AGC is at the output of the SUM area detector, allowing signal ranging based on the area of the burst rather than the peak level of the burst. The AGC is intended to be updated at every sector of servo position bursts such that the signal variances due to the disk radius and differences in the read channel data frequencies can be corrected. In this closed-loop system, the area detected output voltage is compared with the VAGCREF voltage and fed back to provide a gain control current for charging and discharging the VAGCCAP. The VAGCREF voltage should be set to 80% of the full scale value of the RDSUM voltage output. The gain is varied to secure constant area of the output signal and provide amplitude control. The AGC gain value is held constant when the AGCEN is at logic low. When it is logic high, the level of gain can change up or down. The capacitor from VAGCCAP to ground holds the gain setting when AGCEN is at logic low and the area detector output does not affect the gain setting in this mode.

Zero X Detector

The output of the zero crossing detector (comparator) is provided for system synchronization. It detects zero crossings of the composite signal delivered by the Variable Gain Amplifier, VGA. The output of this comparator controls the synchronous rectification of the composite VGA output, in the area detectors. This signal is internally generated in ECL, but an internal ECL to TTL converter presents this output as a TTL level on the ZEROX pin. Control logic in the servo channel employs the ZEROX signal to produce an area detector enabling gate, which spans an integer number of cycles of the composite signal, thus helping to generate accurate timing. If one of the burst signal is very small then the ZEROX signal will not be generated correctly and the Area Detectors (SUM & DIFF) would stay ON. Hence a single radial (always full amplitude) pulse should be located at the beginning and end of each burst. This also minimizes track pairing.

Area Detectors (Sum & Difference)

The area detectors detect the A and B burst levels by area detection. Two area detectors — one to measure the sum of the A and B bursts (A+B), and a second one to measure the difference (A–B). Each area detector is implemented as a gated current — output synchronous rectifier, driving an external charge accumulating integrating capacitor. Area detection occurs only while the area detector is enabled under the control of the GATE pin. The GATE signal turns the SUM & DIFF Area Detectors ON and OFF. Internally it generates a synchronous signal clocked by the AGC output. When GATE is asserted high, the next rising edge of RDINP will turn ON the Area Detectors. When GATE is asserted low, the next rising edge of RDINP will shut OFF the Area Detectors. Thus GATE edges should occur near the falling edges of ZEROX. One point to note is that if the Area Detector is ON and there is no AGC signal then the internal synchronous signal will not change state even if the GATE signal is driven inactive low and the Area Detector continues to remain ON. When the detector is disabled, the integrating capacitor is effectively floated. The on-chip D Flip-Flop resynchronizes the gating signal to remove any timing error due to logic delays in the external gate control logic. It is important that the Area Detectors are shut off when not integrating a desired field, even if there is no AGC signal as the Area Detector offset currents will modify the Area Detector output voltage. Initial conditions on the integrating capacitors are established prior to an area detecting operation by a reset circuit controlled by the $\overline{\text{RESET}}$ pin. The minimum $\overline{\text{RESET}}$ pulse width will depend on the external capacitor used at RDSUM and RDDIFF pins. The pulse width is given by: t_{MIN} = [(CpF x 3V)/80μA] μsecs. $\overline{\text{RESET}}$ is normally held asserted from just after read out until just before the next sample measurement time. A reset operation forces the voltage on the DIFF area detecting capacitor to equal the voltage applied on the VREF pin and the voltage on the sum area detecting capacitor to equal VREF/2. In actuality when $\overline{\text{RESET}}$ is low the voltage observed on the RDDIFF pin will be in the range of 2V to 2.5V and the voltage observed on the RDSUM pin will be in the range of 1V to 1.2V. This is due to internal design constraints. Determination of the burst difference (A-B) or (–A+B) on

alternating tracks, is accomplished under control of the MUXEN pin, by inverting the phase of the carrier input to the DIFF area detector, while one burst is being detected. The inversion is performed by an XOR gate. Accordingly (A-B) is bipolar relative to VREF, while (A+B) is unipolar.

Multiplexer Amplifier

The multiplexed amplifier drives the MUXOUT pin and allows sequential interrogation of the (A-B) DIFF and (A+B) SUM measurements, the results of which are stored on the external integrating capacitors. The amplifier is implemented as two independently selectable input stages, driving a common output structure, to form a voltage follower. To minimize the droop of the (A-B) and the (A+B) measurements, both input stages are biased off during periods when neither measurement is required to be routed to the MUXOUT pin. The MUXSEL and MUXEN pins govern multiplexer channel selection through a decoding network.

CONTINUOUS OR DEDICATED SERVO DEMODULATOR SECTION

The continuous (dedicated) servo demodulator section of the ML4535 consists of its own variable gain amplifier and AGC loop, a variable frequency oscillator and four synchronous detectors. The DSIN input is usually of the order of 20mV–400mV differential peak to peak and the R_{IN} is approximately 4kohms.

The first synchronous detector (AREA DETECTOR #4) is used as a multiplying phase detector to control the variable frequency oscillator and complete the analog portion of the phase locked loop that recovers the clock. A standard PLL loop filter is connected on the VCOIN pin or an external signal could be used to drive this line. The RT and CT components are used to set the VCO frequency range. Figure 1 shows the graphical representation of the VCOOUT frequency vs VCOIN voltage for a fixed value of RT and CT. It is recommended that CT should be kept as large as possible, say around 50pF, otherwise parasitics could begin to dominate. Also it is recommended that CT should connect to the VCOVCC right at the pin and the VCOVCC should be well decoupled at that point. Stability could be further improved by placing another resistor to ground from the RT pin, allowing smaller RT and hence allowing the increase in CT. Recommended range for RT is 200 ohms to 2k ohms. Recommended VCO frequency range is 10 to 30 MHz with the VCO frequency being set at two or four times the servo pattern fundamental frequency. A typical loop filter circuit at VCOIN is shown at the frontend of figure 3. The gain of the VCO is approximately 10% of the center frequency per volt (MHz/volt). The VCOOUT has a V_{OH} of 2.2V to 2.4V and a V_{OL} of 0.5V which improves symmetry around the 1.4V threshold for the VCO (TTL compatible levels). The duty cycle is symmetrical with large enough swings on the RT and CT associated with the VCO.

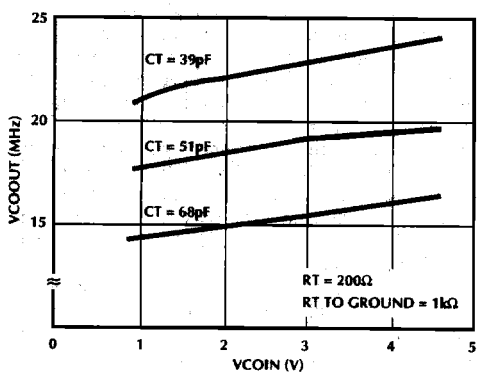


Figure 1. ML4535 VCO Characteristics

The second synchronous detector (AREA DETECTOR #3) is used for measuring the area of the composite signal, to determine its amplitude for comparison with the reference of the AGC loop. The AGC loop consists of the Area Detector 3, external filter capacitor on DSSUM, REXT resistor and internal voltage set reference current on DSSUM and the gain vs. control voltage characteristic of the VGA amplifier. The reference baseline voltage for the AGC output voltage is 2.5V. Area Detector 3 generates a current and when the integral of that current equals a DC current (approx 62µA) set by REXT, the AGC loop is stabilized. The differential output of the servo surface AGC is made available on the AGCOUTP and AGCOUTN pins. An amplitude level comparator is also included on this detector's output to provide the logic level output for Frame sync and Index data. The SYNC detector circuit is threshold based. The threshold level is set internally to 25% of full scale, however this level can be adjusted through the external SYNCADJ pin. Connecting a resistor from the SYNCADJ pin to ground increases the threshold level above 25%, while a resistor to VCC will decrease the threshold level below 25% of full scale. There is a ±20% potential of error on the amount by which the threshold is changed from the internal level using the SYNCADJ pin.

The third and fourth synchronous detectors (AREA DETECTORS #1 & #2) are used to demodulate the normal and quadrature position signals. The Area Detectors 1 & 2 are turned ON by asserting SEL1 and SEL2 lines active high. A logic low on these lines turns them OFF. The normal and quadrature outputs are currents that should be terminated off chip with nominal 19K resistors to VREF or 0.9 VREF. The center value of the nominal output voltage range of DSDIFF1 and DSDIFF2 (the output of Area Detectors 1 & 2) is 2.5V with a range of ±1.5V. The external resistors may be terminated to 2.3V to give maximum swing over supplies (since minimum V_{CC} is 4.5V, hence VCC/2 would be approximately 2.3V). Ripple frequency to slew rate relationship can be improved by adding switches in series with the terminating resistors gated by SEL# in the outputs, although this is usually not required.

The DC requirements of the filter can be reduced by using the configuration where the active filter amplifier does not contribute to the DC offset, for a unity gain configuration. The position detector gain is approximately 1.19. The emitter resistor in the AGC detector is around 16K, giving an I = 62.5μA. This implies that the average voltage out is approximately 1V, which implies that the output ON position with a duty cycle of 3/8 equals (0.375 x 1.19) = 0.466V base to peak based on the resistor ratio of 19K to 15.8K. Making this equal to the half span of the ADC by having a gain in the filter should not have a detrimental effect on the system accuracy because selecting the demodulator clock phase (based on track type) to result in the same polarity of the Position Error Signal (PES) slope and by using the same detector output section for track following results in the cancellation of offsets, with a minimum penalty in the reduction of the PES dynamic range.

Component Selection

The following section outlines the different equations for determining some of the component values associated with the ML4535 design.

VAGCCAP $C = \{(DC)/(2Kohms \times BW)\}$

where DC = Duty cycle of the AGCEN signal (approx 1/10)
BW = AGC loop bandwidth = $2 \times \pi \times f$ (approx 500Hz)

RDSUM Capacitor $C_{SUM} = \{(560\mu A) \times (T_{SAMPLE})/(2.8 \times M)\}$

where M = portion of the full scale voltage to be used in nominal condition (suggested value = 0.8)
T_{SAMPLE} = width of the GATE pulse

RDDIFF Capacitor $C_{DIFF} = \{560\mu A) \times (T_{SAMPLE})/(1.4 \times M)\}$

where M = portion of the full scale voltage to be used in nominal condition (suggested value = 0.8)
T_{SAMPLE} = width of the GATE pulse

DCRCAP $C = \{(0.04 \times 20)/(16Kohms \times BW)\}$

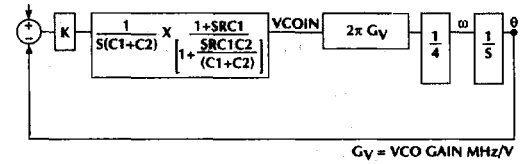
where BW is the AGC restore loop bandwidth = $2 \times \pi \times f$ (range 5 to 10kHz)

DSSUM $C = (16/(BW \times 8Kohm))$

where BW is the bandwidth = $2 \times \pi \times f$ = (range 10 to 50kHz)

EXAMPLE SYSTEM DESCRIPTION

An example continuous servo composite servo encoding and the associated demodulator clock waveforms are shown in figure 2. The VCO operates at twice the frequency of the fundamental of the composite signal and drives two flip flops that generate quadrature and normal phase references. The Clock generation logic circuit and synchronizing circuit for the PLL, to acquire initial lock with type 2 loop, are shown in figure 3. A block diagram of the PLL is shown below with the transfer function based on the loop filter components (refer figure 3).



G_V = VCO GAIN MHz/V

The value of the constant K is given by:

$$K = \frac{62}{\pi} \times \frac{\text{phase compared cycles in the servo frame}}{\text{total cycles in the servo frame}}$$

A type 2 loop has two poles at the origin of the S-plane or two time domain integrations — one in the frequency to phase conversion and one in the loop filter. In figure 3, the DC level at the non-inverting input of the left comparator should be approximately ($0.1V_{CC}$ plus one diode drop). The current supplied by the output resistors and series diodes should be approximately 62μA/4. Time constant is approximately 2 x (1/PLL BW) and the pullup resistors to V_{CC} are approximately 1 Kohm or much less than the value of the other resistors so as to make the output up level approximately equal to V_{CC} during operation. A state counter divides the servo frame into eight intervals which are:

NAME	LENGTH (IN CLOCK CYCLES)
S	2
X_1, X_2, X_3	1
A, B, C, D	*n* where *n* is an integer like *7 or 8*

Note that all peaks of the composite signal are on Quad clock phase boundaries, so it contains only one fundamental frequency, which is easily acquired by the phase locked loop. The sync character is 180° out of phase with all others; thus at phase alignment it causes no disturbances to the phase comparator but gives an easily recognizable reverse polarity ripple in the AGC which is detected with a level detector to provide a frame sync logic signal to initialize the state counter.

The inphase clock is used throughout A, B, C, D but inverted 180° as required by the track type to give A–B, C–D, B–A, D–C without additional analog switching in position 1 demodulator for track following.

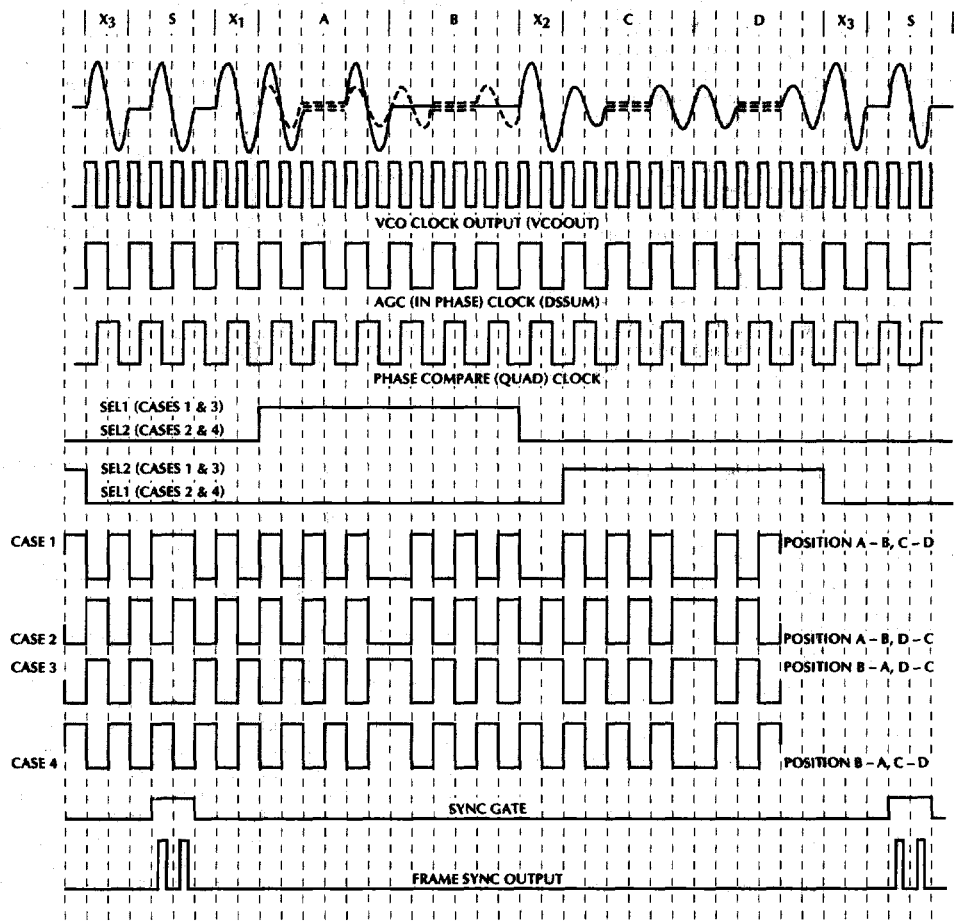


Figure 2. Continuous Servo Encoding and Demodulator Clock Waveforms

Filters are needed on each of the four demodulators for removing the carrier ripple and providing frequency compensation for the gain control and phase locked loop systems. The current output scaling of all four detectors to the AGC output are the same and set by on-chip resistors. The AGC setpoint is a current set by REXT and VREF. Thus a capacitor to ground provides an integrating response for the AGC control loop, as well as ripple filtering. For the phase comparator filter, two capacitors and a resistor provide D.C. integration plus a lead-lag for the PLL control loop compensation. For the position outputs, external 19K nominal resistors to (0.9 x V_{REF}) should be provided and a capacitor to ground is added to form a low pass ripple filter.

The phase compare detector forms phase only (not phase frequency) characteristic, so the loop will not acquire initial lock with an integrating loop filter, which is needed to assure no steady state phase error. Transfer function for the gain of the phase comparator (assuming a sinusoidal servo signal) is given by:

$$\frac{62\mu A}{\pi \text{ rad}} \times \left[\frac{(\text{time of X1, X2, X3}) + (\text{time of A, B, C, D})}{2 \times (\text{time of one frame})}\right]$$

The synchronizing circuit suggested (refer figure 2), senses when the VCO control voltage is near either rail and applies a pulse that ramps it toward the other rail and thus through the operational frequency where it locks. The lock range is much greater than the acquire range, so it retains lock in the presence of the resistor–coupled pulse, with a small phase error, until the pulse goes away and the phase error becomes zero.

It is generally recommended that the servo head magnetic width be equal to two track pitches for best results. In this case for an on-track position one of the four burst patterns becomes almost zero. There is no loss of information on phase when this happens, since then its complement is twice as large so that the sum of the two is constantly independent of position and thus the amount of phase information per frame is also constantly independent of position.

HYBRID SERVO VERSUS ONLY EMBEDDED SERVO

There are a number of merits in using a hybrid servo scheme consisting of a servo surface plus limited data head servo samples over the completely embedded or data head sector servo samples scheme. These are summarized below:

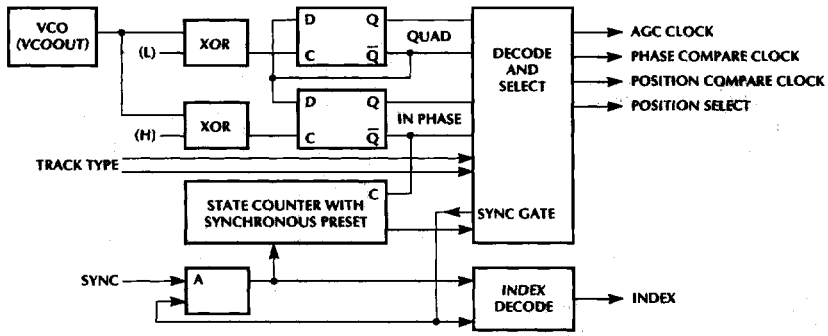
Cost: Lost data surface capacity is less than 1% for a servo surface plus samples compared to 8% for samples only. This suggests that with six or more disks, the servo surface has an advantage. Without a servo surface, it is difficult to generate accurately phase and track center aligned data head (embedded) servo sectors in the drive, requiring them to be done with extra time on an expensive servo writer and moving the cost crossover point nearer to four disks. Drive hardware and costs including assembly and test favour DSP implementations in either case.

Effect on position error sources: These can be very similar for both configurations with optimized control algorithims. The servo surface does have some advantages in being able to obtain higher bandwidths and thus faster settling time and greater reduction of non-repetitive run-out and random disturbances.

Effect on access time: A system with a servo surface has two advantages here. The ability to adjust the control signal at shorter time intervals and a higher small signal bandwidth, both of which reduce settling time. Move times can be equivalent.

Data integrity: Here there is a clear superiority for a servo surface system in preventing writes which destroy existing data. There are at least two ways in which this can happen. Electronic noise in the sector timing causes servo sectors to be over written, so that the head can no longer be positioned to read the track even if the data is intact. This probability can be made acceptably small by redundancy in the electronics. External mechanical shock while writing a data sector can not only cause improper writes of the new data but also overwrite adjacent tracks. Inherently there is no way to prevent this with servo sectors only, as there is no position data measurement available and estimators do no good for random fast disturbances. Dynamically balanced rotary actuators reduce this exposure compared to linear travel positioners but cannot eliminate it completely.

CLOCK GENERATION LOGIC (Implemented in Gate Array)



SYNCHRONIZING CIRCUIT FOR THE PLL (To acquire initial lock with type 2 loop)

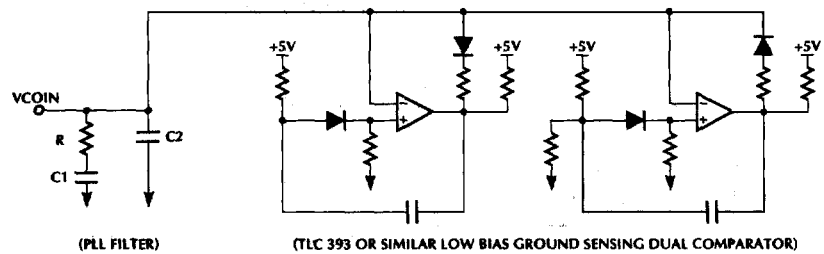


Figure 3. Support Circuitry for the ML4535 Based "Hybrid" Servo Subsystem

SERVO DESIGN SUGGESTIONS FOR A HIGH TRACK DENSITY DISK DRIVE

The best design choices for a high track density disk drive with four or more platters are outlined below and the hybrid servo subsystem based on the ML4535 & ML2377, provides the most optimum solution for implementing these design choices and making track densities greater than 3500 TPI achievable.

1) Continuous servo surface with quadrature signals plus some position samples and/or calibration tracks for each data head.

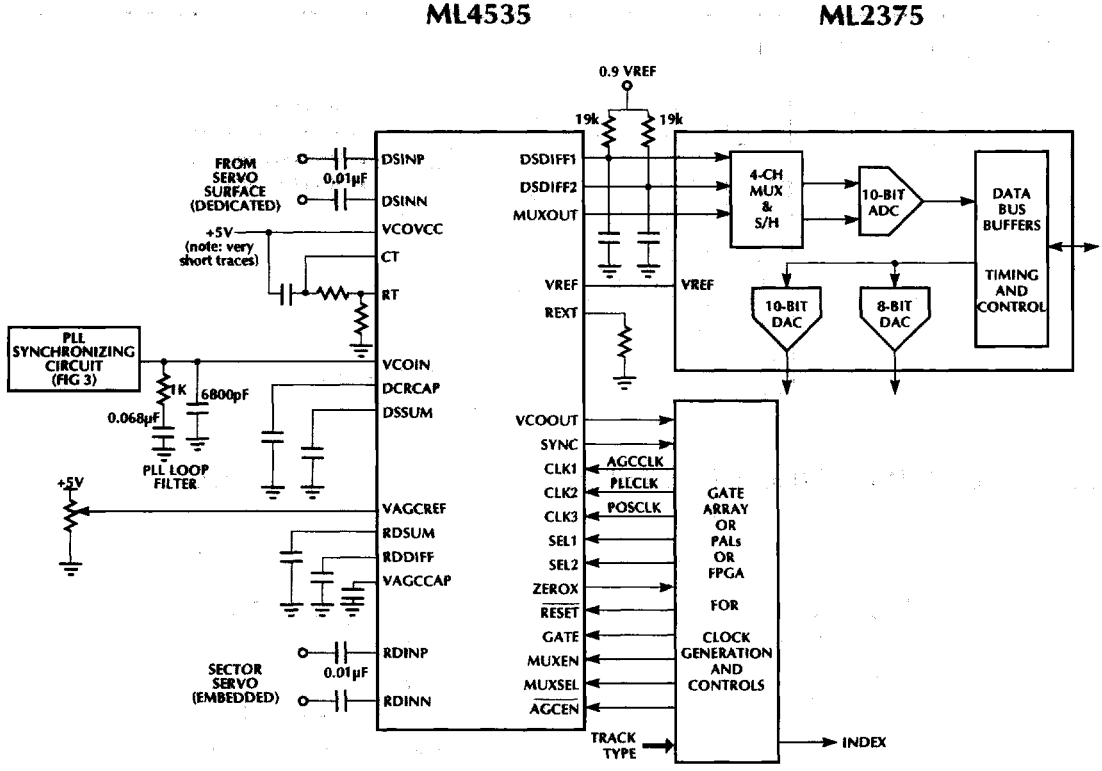
2) DSP implementation of the position control system for best performance of state estimators and adaptive parameter adjustment.

3) Area integration position demodulation on both the servo (dedicated) surface and data head position (embedded) servo samples, for best accuracy and noise rejection.

4) Thin film heads with gap edges aligned and perpendicular to the disk surface.

5) Dynamically balanced rotary actuator for best rejection of external mechanical shock.

ML4535 BASED SYSTEM APPLICATION DIAGRAM



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4535CH	0°C to +70°C	44-Pin TQFP (H44)