

## Read Data Processor

### GENERAL DESCRIPTION

The ML541 is a monolithic bipolar integrated circuit for use in a disk drive system to detect analog pulse peaks generated by the recording head during a Read operation. Connected to the read/write amplifier output, it detects valid data and provides a TTL output to the data separator for further processing. It contains both analog and digital circuitry and supports the reading of MFM and RLL encoded data at rates up to 15 megabits/second.

The primary functional blocks within the device include an AGC amplifier, a level detector, a slope detector, and output logic. Operating modes Read, Write, and Hold are selectable with input logic signals. Read mode is used for pulse peak detection during a Read operation. Write mode disables the device's output during a Write operation, while Hold mode holds the AGC gain constant during recovery of embedded servo information.

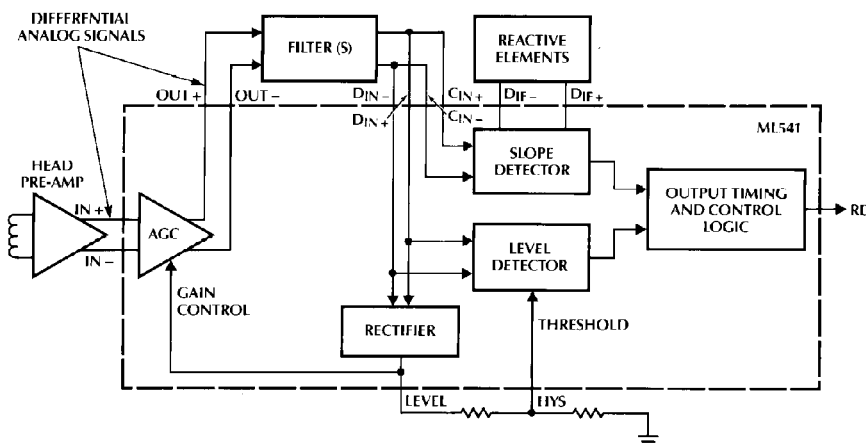
By using both level and slope detection, accurate pulse validation and peak time detection is achieved. The ML541 performance can be adjusted to fit particular needs through external component selection.

The ML541 is available both in a 24-pin PDIP and 28-pin PCC.

### FEATURES

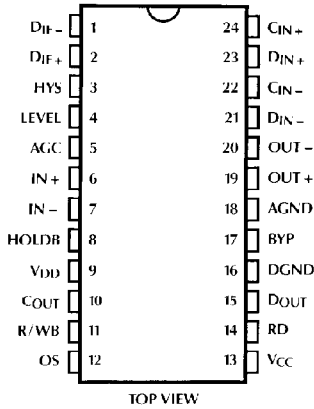
- Second source for SSI 541
- Data rates up to 15 megabits/second
- Supports MFM and RLL encoded read data
- 25 MHz wide-bandwidth AGC amplifier
- Fast AGC region for fast transient recover
- Slow AGC region for minimum zero crossing distortion
- Write to read transient suppression
- Supports embedded servo decoding
- +5V, +12V power supplies

### SIMPLIFIED BLOCK DIAGRAM

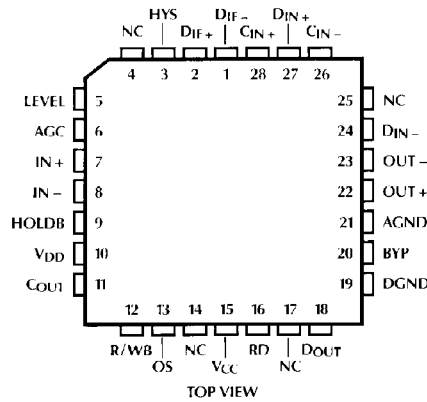


PIN CONNECTIONS

24-Pin DIP and SOIC Package



28-Pin PCC Package



PIN DESCRIPTION

NAME	FUNCTION	NAME	FUNCTION
V <sub>CC</sub>	+5V	HYS	Input for setting hysteresis level of the hysteresis comparator.
V <sub>DD</sub>	+12V	LEVEL	Provides rectified signal level for input to the hysteresis comparator.
AGND	Analog Ground.	D <sub>OUT</sub>	Buffered test point for monitoring D input of the flip-flop.
DGND	Digital Ground.	C <sub>IN+</sub> , C <sub>IN-</sub>	Analog input to the differentiator.
R/WB	TTL compatible Read/Write Control pin.	D <sub>IF+</sub> , D <sub>IF-</sub>	External differentiating network connection pins.
IN+, IN-	Analog Signal Input pins	C <sub>OUT</sub>	Buffered test point for monitoring the clock input to the flip-flop.
OUT+, OUT-	AGC Amplifier Output pins	OS	Connection for read output pulse width setting capacitor C <sub>OS</sub> .
BYP	The AGC timing capacitor C <sub>AGC</sub> is tied between this pin and AGND.	RD	TTL compatible read output.
HOLDB	TTL compatible pin that holds the AGC gain when pulled low.		
AGC	Reference input voltage level for the AGC circuit.		
D <sub>IN+</sub> , D <sub>IN-</sub>	Analog input to the hysteresis comparator.		

TABLE 1 MODE SELECT

R/WB	HOLDB	MODE	DESCRIPTION
1	1	READ	AGC amp section active, Digital section active.
1	0	HOLD	AGC gain constant, Digital section active.
0	X	WRITE	AGC gain maximum, Digital section inactive, Input common mode resistance reduced.

0 = Logic level low  
 1 = Logic level high  
 X = Don't care

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Power Supply Voltage Range	
$V_{CC}$	-0.3 to 6V <sub>DC</sub>
$V_{DD}$	-0.3 to 14V <sub>DC</sub>
Terminal Voltage Range	
R/WB, IN+, IN-, HOLDB	-0.3V to $V_{CC} + 0.3V$
RD	-0.3V to $V_{CC} + 0.3V$ or +12mA
All others	-0.3V to $V_{DD} + 0.3V$
Storage Temperature Range	-65°C to +150°C
Junction Temperature ( $T_J$ )	+135°C
Lead Temperature (Soldering, 10sec)	260°C

**OPERATING CONDITIONS**

Supply Voltage	
$V_{CC}$	5V ± 10%
$V_{DD}$	12V ± 10%
$V_{(C_{IN+}-C_{IN-})}, V_{(D_{IN+}-D_{IN-})}$	1V <sub>P-P</sub>
$V_{HYS}$	1.0V
$C_{OS}$	50 to 200pF
Typical Component Values (Refer to Typical Applications)	
$C_{IN}$	0.001μF
$C_S$	0.01μF
$C_{OUT}$	0.0047μF
$R_{OUT}$	400Ω
$C_{AGC1}$	220pF
$C_{AGC2}$	2000pF
$R_{AGC}$	2.21kΩ
$C_{LEVEL}$	150pF
$R_{LEVEL1}$	1.54kΩ
$R_{LEVEL2}$	6.49kΩ
$C_{OS}$	50pF

**ELECTRICAL CHARACTERISTICS**

The following specifications apply over the recommended operating conditions of  $V_{CC} = 5V \pm 10\%$ ,  $V_{DD} = 12V \pm 10\%$ ,  $0^\circ C < T_A < 70^\circ C$  and external components as specified under recommended operating conditions unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
<b>DC Characteristics</b>						
$I_{CC}$	$V_{CC}$ Supply Current	Outputs unloaded			14	mA
$I_{DD}$	$V_{DD}$ Supply Current	Outputs unloaded			70	mA
$P_D$	Power Dissipation	Outputs unloaded, $T_A = 70^\circ C$			930	mW
<b>Digital Inputs Characteristics (HOLDB, R/WB)</b>						
$V_{IH}$	High Voltage		2			V
$V_{IL}$	Low Voltage				0.8	V
$I_{IH}$	High Current	$V_{IH} = 2.4V$			100	μA
$I_{IL}$	Low Current	$V_{IL} = 0.4V$	-0.4			mA
<b>Digital Outputs Characteristics (<math>C_{OUT}</math>, RD)</b>						
$V_{OL}$	Output Low Voltage	$I_{OL} = 4mA$			0.4	V
$V_{OH}$	Output High Voltage	$I_{OH} = 400\mu A$	2.4			V
<b>WRITE AND HOLD MODE CHARACTERISTICS</b>						
<b>Mode Control</b>						
$t_{RW}$	Read to Write Transition Time				1	μs
$t_{WR}$	Write to Read Transition Time	AGC settling not included, time to high input resistance	1.2		3	μs
$t_{RH}$	Read to Hold Transition Time				1	μs
<b>Write Mode</b>						
$Z_{IC}$	Common Mode Input Impedance (both sides)	R/WB pin = low		250		Ω

# ML541

## ELECTRICAL CHARACTERISTICS (Continued)

The following specifications apply over the recommended operating conditions of  $V_{CC} = 5V \pm 10\%$ ,  $V_{DD} = 12V \pm 10\%$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ ,  $IN+$  and  $IN-$  AC coupled,  $OUT+$  and  $OUT-$  differentially loaded with  $>600\Omega$  and each side loaded with  $<10\text{pF}$  to GND,  $C_{BYP} = 2000\text{pF}$ ,  $OUT+$  and  $OUT-$  AC coupled to  $D_{IN+}$  and  $D_{IN-}$  respectively,  $V_{AGC} = 2.2\text{V}$  unless otherwise specified. (See Note 2.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP NOTE 5	MAX	UNITS
<b>READ MODE CHARACTERISTICS</b>						
<b>AGC Amplifier</b>						
$R_{ID}$	Differential Input Resistance	$V_{(IN+ - IN-)} = 100\text{mV}_{P-P}$ @ 2.5 MHz		5		$k\Omega$
$C_{ID}$	Differential Input Capacitance	$V_{(IN+ - IN-)} = 100\text{mV}_{P-P}$ @ 2.5 MHz			10	$\text{pF}$
$Z_{IC}$	Common Mode Input Impedance (both sides)	R/WB pin high		1.8		$k\Omega$
		R/WB pin low		0.25		$k\Omega$
$A_{VR}$	Gain Range	$1\text{V}_{P-P} \leq V_{OUT\text{ diff}} < 2.5\text{V}_{P-P}$	4		83	V/V
$e_N$	Input Noise Voltage	Gain set to maximum			30	$\text{nV}/\sqrt{\text{Hz}}$
BW	Bandwidth	Gain set to maximum, -3 dB point	25			MHz
$V_{OP}$	Maximum Output Voltage Swing	Set by $V_{AGC}$	3			$V_{P-P}$
$I_{OD}$	$OUT+$ to $OUT-$ Pin Current	No DC path to GND, See Note 3	$\pm 3.2$			$\text{mA}$
$R_O$	Output Resistance			20	30	$\Omega$
$C_O$	Output Capacitance			12		$\text{pF}$
$V_{IP}$ $V_{AGC}$	$(D_{IN+} - D_{IN-})$ Input Voltage Swing VS AGC Input Level	$30\text{mV}_{P-P} \leq V_{(IN+ - IN-)} \leq 550\text{mV}_{P-P}$ , $1.5\text{V} \leq V_{AGC} \leq 3.75\text{V}$		0.48		$V_{P-P}/V$
$V_{IP}$	$(D_{IN+} - D_{IN-})$ Input Voltage Swing Variation	$30\text{mV}_{P-P} < V_{(IN+ - IN-)} < 550\text{mV}_{P-P}$ , AGC Fixed, over supply and temp.			+8	%
$t_D$	Gain Decay Time	See Figure 1a; $V_{IN} = 300\text{mV}_{P-P}$ then $>150\text{mV}_{P-P}$ at 2.5 MHz, $V_{OUT}$ to 90% of final value.		50		$\mu\text{s}$
$t_A$	Gain Attack Time	See Figure 1b; from Write to Read transition to $V_{OUT}$ at 110% of final value, $V_{IN} = 400\text{mV}_{P-P}$ @ 2.5 MHz		4		$\mu\text{s}$
$I_{AGCfc}$	Fast AGC Capacitor Charge Current	$V_{(D_{IN+} - D_{IN-})} = 1.6\text{V}$ , $V_{AGC} = 3.0\text{V}$		1.5		$\text{mA}$
$I_{AGCsc}$	Slow AGC Capacitor Charge Current	$V_{(D_{IN+} - D_{IN-})} = 1.6\text{V}$ , Vary $V_{AGC}$ until slow discharge begins		0.17		$\text{mA}$
		Fast to Slow Attack Switchover Point	$V_{(D_{IN+} - D_{IN-})}$ $V_{(D_{IN+} - D_{IN-})}$ Final		1.25	-
$I_{AGCD}$	AGC Capacitor Discharge Current	$V_{(D_{IN+} - D_{IN-})} = 0.0\text{V}$ Read Mode		4.5		$\mu\text{A}$
		Hold Mode	-0.2		+0.2	$\mu\text{A}$
CMRR	CMRR (Input Referred)	$V_{IN+} = V_{IN-} = 100\text{mV}_{P-P}$ @ 5 MHz, gain at max.	40			dB
PSRR	PSRR (Input Referred)	$V_{CC}$ or $V_{DD} = 100\text{mV}_{P-P}$ @ 5 MHz, gain at max.	30			dB
<b>Hysteresis Comparator</b>						
$V_{IP}$	Input Signal Range				1.5	$V_{P-P}$
$R_{ID}$	Differential Input Resistance	$V_{(D_{IN+} - D_{IN-})} = 100\text{mV}_{P-P}$ @ 2.5 MHz	5		15	$k\Omega$
$C_{ID}$	Differential Input Capacitance	$V_{(D_{IN+} - D_{IN-})} = 100\text{mV}_{P-P}$ @ 2.5 MHz			6.0	$\text{pF}$
$Z_{IC}$	Common Mode Input Impedance	(both sides)		2.0		$k\Omega$
$V_{IO}$	Comparator Offset Voltage	I IYS pin at $-0.5\text{V}$ , $\leq 1.5\text{k}\Omega$ across $D_{IN+}$ , $D_{IN-}$		5		$\text{mV}$

**ELECTRICAL CHARACTERISTICS** (Continued)

The following specifications apply over the recommended operating conditions of  $V_{CC} = 5V \pm 10\%$ ,  $V_{DD} = 12V \pm 10\%$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ , IN+ and IN- AC coupled, OUT+ and OUT- differentially loaded with  $>600\Omega$  and each side loaded with  $<10pF$  to GND,  $C_{BYP} = 2000pF$ , OUT+ and OUT- AC coupled to  $D_{IN+}$  and  $D_{IN-}$  respectively,  $V_{AGC} = 2.2V$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>READ MODE CHARACTERISTICS</b> (Continued)						
<b>Hysteresis Comparator</b> (Continued)						
$V_{HYS}$	Peak Hysteresis Voltage vs HYS pin voltage (input referred)	$1V < V_{HYS} < 3V$		0.21		V/V
$I_I$	HYS Pin Input Current	$1V < V_{HYS} < 3V$	0		-20	$\mu A$
$I_O$	LEVEL Pin Max Output Current		3			mA
$R_O$	LEVEL Pin Output Resistance	$I_{LEVEL} = 0.5mA$		180		$\Omega$
$V_{OL}$	$D_{OUT}$ Pin Output Low Voltage	$T_A = 70^\circ C$	$V_{DD} - 4.0$		$V_{DD} - 2.5$	V
$V_{OH}$	$D_{OUT}$ Pin Output High Voltage	$T_A = 70^\circ C$	$V_{DD} - 2.2$		$V_{DD} - 1.5$	V
$V_{OL}$	$D_{OUT}$ Pin Output Low Voltage	$T_A = 25^\circ C$	$V_{DD} - 4.0$		$V_{DD} - 2.8$	V
$V_{OH}$	$D_{OUT}$ Pin Output High Voltage	$T_A = 25^\circ C$	$V_{DD} - 2.5$		$V_{DD} - 1.6$	V
<b>Active Differentiator</b>						
$V_{IP}$	Input Signal Range				1.5	$V_{P,P}$
$R_{ID}$	Differential Input Resistance	$V_{(C_{IN+} - C_{IN-})} = 100mV_{P,P}$ @ 2.5MHz	5		15	k $\Omega$
$C_{ID}$	Differential Input Capacitance	$V_{(C_{IN+} - C_{IN-})} = 100mV_{P,P}$ @ 2.5MHz			6	pF
$Z_{IC}$	Common Mode Input Impedance	(both sides)		2.0		k $\Omega$
$I_{OD}$	$D_{IF+}$ to $D_{IF-}$ Pin Current	Differentiator Imped must be set so as not to clip signal at this current level	$\pm 1.3$			mA
$V_{IO}$	Comparator Offset Voltage	$D_{IF+}$ , $D_{IF-}$ AC Coupled		5		mV
$V_{OL}$	$C_{OUT}$ Pin Output Low Voltage	$0 \leq I_{OH} \leq 0.5mA$		$V_{DD} - 3$		V
$V_{PO}$	$C_{OUT}$ Pin Output Pulse Voltage	$0 \leq I_{OH} \leq 0.5mA$		0.4		V
$PW_0$	$C_{OUT}$ Pin Output Pulse Width	$0 \leq I_{OH} \leq 0.5mA$		30		ns

The following specifications apply over the recommended operating conditions of  $V_{CC} = 5V \pm 10\%$ ,  $V_{DD} = 12V \pm 10\%$ ,  $0^\circ C \leq T_A \leq 70^\circ C$ ,  $V_{(C_{IN+} - C_{IN-})} = V_{(D_{IN+} - D_{IN-})} = 1.0V_{P,P}$  AC coupled sine wave at 2.5MHz,  $R_{DIF} = 100\Omega$ ,  $C_{DIF} = 65pF$ ,  $V_{HYS} = 1.8V$ ,  $C_{OS} = 60pF$ , 4k $\Omega$  to  $V_{CC}$  and 10pF to GND on pin RD unless otherwise specified.

**Output Data Characteristics** (Refer to Figure 2)

$t_{D1}$	D-Flip-Flop Set Up Time	Min delay from $V_{(D_{IN+} - D_{IN-})}$ exceeding threshold to $V_{(D_{IF+} - D_{IF-})}$ reaching a peak	0			ns
$t_{D3}$	Propagation Delay				110	ns
$t_{D5}$	Output Data Pulse Width	$T_A = 25^\circ C$ , $V_{CC} = 5V$ , $V_{DD} = 12V$		$\pm 15\%$		
$t_{D5}$	Output Data Pulse Width Variation	$C_{OS} = 60pF$ , See Note 4	30		80	ns
$t_{D3} - t_{D4}$	Logic Skew (Pulse Pairing)				3	ns
$t_R$	Output Rise Time	$V_{OH} = 2.4V$			18	ns
$t_F$	Output Fall Time	$V_{OL} = 0.4V$			14	ns

**Note 1:** Absolute maximum ratings are limits beyond which the life of the integrated circuit may be impaired. All voltages unless otherwise specified are measured with respect to ground.

**Note 2:** Limits are guaranteed by 100% testing, sampling, or correlation with worst-case test conditions.

**Note 3:** AGC amplifier output current may be increased as in Figure 4.

**Note 4:**  $t_{D5} = 770$  ( $C_{OS}$ ),  $50pF < C_{OS} < 150pF$ .

**Note 5:** Typicals are parametric norm at  $25^\circ C$

## FUNCTIONAL DESCRIPTION

### Operating Modes

The ML541 has three definitive operation modes which are: Read mode, Write mode and Hold mode. These modes are defined by input pins HOLDB and R/WB as shown in Table 1. Read mode, the mode used normally for pulse detection, is assumed in the following sections unless otherwise noted.

### AGC Amplifier Section

The purpose of the AGC amplifier is to provide a constant read signal level for both the level and slope detectors. Full differential processing of the read signal is used to minimize noise and distortion in the analog signal. A wide gain range is required due to large signal variation when moving the recording head from an inside to outside data track or variations in media.

The differential output voltage level  $V_{OUT}$  from the AGC amp is determined by voltage  $V_{AGC}$  present at pin AGC.  $V_{OUT}$  is full wave rectified and compared against  $V_{AGC}$  to create charge/discharge current for capacitor  $C_{BYP}$  connected at pin BYP. Voltage  $V_{BYP}$  across  $C_{BYP}$  controls the gain in the AGC amplifier.

Two distinct values of  $I_{BYP}$  are possible which determine a fast and slow AGC gain response attack rate. When  $V_{OUT}$  is more than 125% of the set level a high value of  $I_{BYP}$  is sourced which provides a fast AGC attack rate. When  $V_{OUT}$  is within 100% to 125% of the set level a reduced value of  $I_{BYP}$  is sourced which provides a slower attack rate. The fast-slow gain response attack rates provides for an initial quick system response and then minimum zero crossing distortion of the analog signal once the gain is within working range.  $V_{AGC}$  should be set so that the differential input voltage  $V_{DIN}$  into the level comparator is  $1V_{P-P}$  at nominal Read signal conditions. The AGC amp section gain is given by:

$$\frac{A_{V2}}{A_{V1}} = \exp \frac{V_{BYP2} - V_{BYP1}}{5.8 \times V_T}$$

Where:  $A_{V1}$ ,  $A_{V2}$  are initial and final amplifier gain values corresponding to initial and final  $V_{BYP}$  values.

$$V_T = (KT)/Q = 26 \text{ mV at room temperature.}$$

The AGC amp's differential inputs must be AC coupled to the read amplifier (ML117, ML501, etc.) differential outputs. Similarly, AC coupling must be used at the AGC amp outputs.

**AGC Amp During Write Mode**— When the ML541 is put into write mode, the AGC amp's input impedance is lowered to allow a faster dampening of the Write to Read transient from the head pre-amp. The AGC gain is also set to maximum gain so that fast AGC attack will occur when changing back to the Read mode. Internal device timing is controlled so that settling occurs prior to Read mode activation. Minimal value input coupling capacitors should be chosen to reduce settling time, however, bandwidth requirements also need to be considered.

**AGC Amp During Hold Mode** During the Hold mode, the charge/discharge current driving pin BYP is internally disconnected. AGC compensation capacitor  $C_{AGC}$  will then hold the present gain setting. The amplitude of  $V_{OUT}$  will therefore not affect the AGC gain and gain will remain constant.

Hold mode is used so that AGC gain will not be adjusted when embedded servo information is read. This prevents losing the pulse peak amplitude information needed during position decoding, or creating additional gain settling time when again reading data. Embedded servo pulses are normally taken at outputs  $D_{IF-}$  and  $D_{IF+}$ , as shown in the typical application.

### External Filter Network

Filtering for the level and slope detectors can be performed with a single filter or two separate filters. If separate filters are used, care must be used to insure that time delays are matched. A multi-pole Bessell filter is recommended due to the group delay and linear phase characteristics.

### Level Detector

The full wave rectified  $V_{OUT}$  is buffered and available at pin LEVEL. The level detector uses a hysteresis comparator to compare the processed read signal amplitude against a reference voltage derived from voltage  $V_{LEVEL}$  output from pin LEVEL. Using  $V_{LEVEL}$  provides a feed-forward function that allows valid level detection to be performed prior to AGC amp gain settling. The level detector hysteresis value is set in a way that will only allow relatively large read pulse peaks (negative or positive) to be detected.

### Slope Detector

The slope detector uses an external reactive component network to produce a voltage signal proportional to the differential of the read signal. By using a hysteresis comparator to detect zero slope of the read signal, the time occurrence of positive or negative read pulse peak values can be determined.

An external reactive network, shown in the Typical Application, is used between the  $D_{IF+}$  and  $D_{IF-}$  pins to provide the differential function given by:

$$A_V = \frac{-2000Cs}{LCs^2 + (R + 92)Cs + 1}$$

Where: C = External capacitor (20 pF to 150 pF)

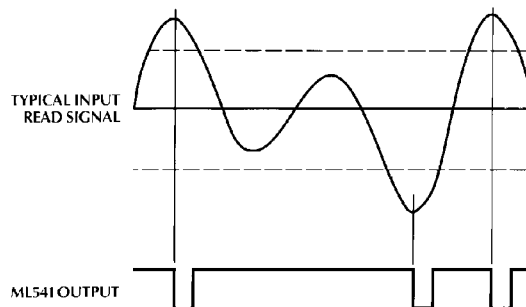
L = External inductor

R = External resistor

s =  $j\omega = j2\pi f$

### Output Logic

The output logic provides a negative TTL pulse at pin RD which begins at the peak of a valid read pulse, as shown below.





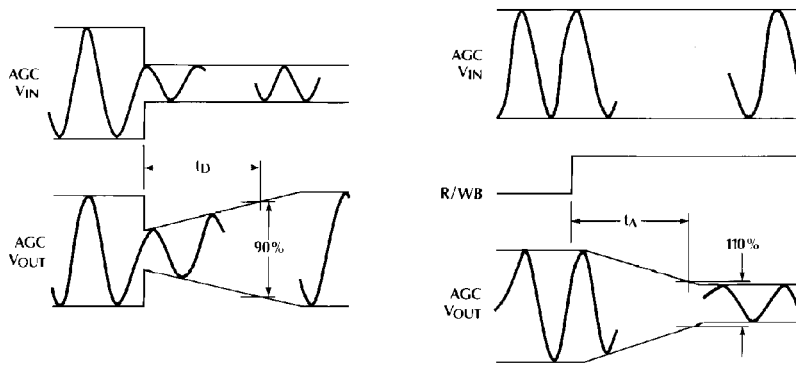


Figure 1. AGC Timing Diagram

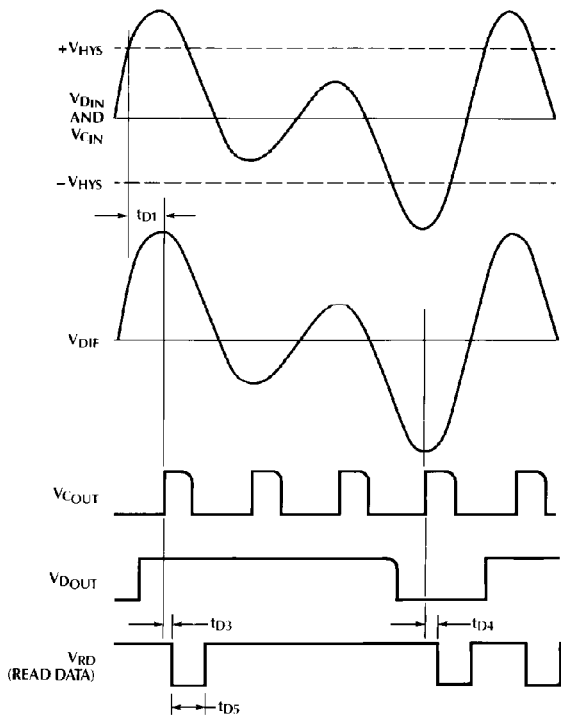


Figure 2. Output Logic Timing Diagram

TYPICAL APPLICATIONS

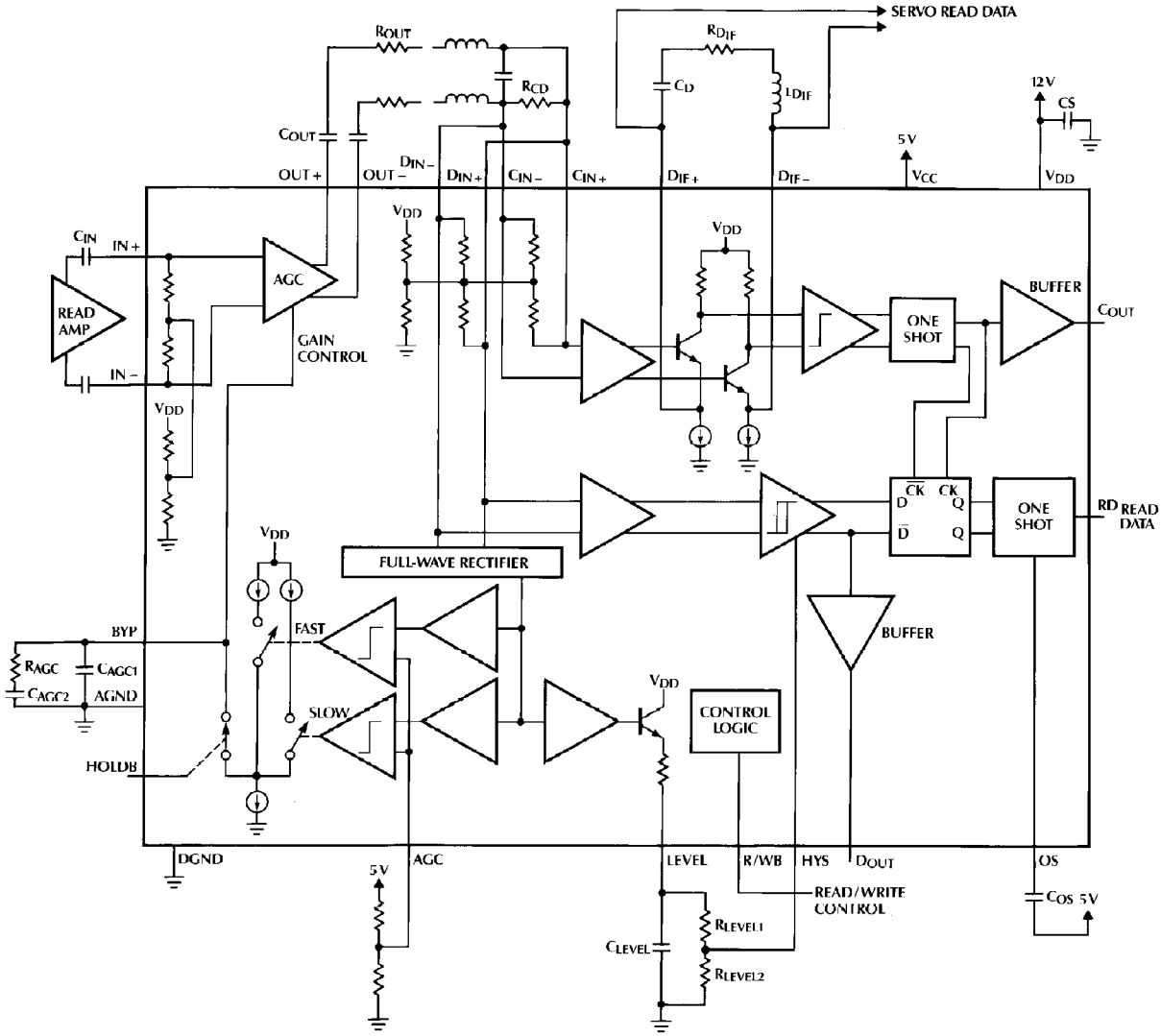


Figure 3. Typical Application Diagram

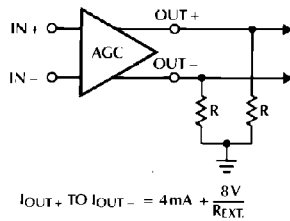


Figure 4. Modification of AGC Amplifier Output to Drive Low Impedance Filters

# ML541

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## ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML541CP	0°C to 70°C	Molded DIP (P24)
ML541CQ	0°C to 70°C	Molded PCC (Q28)
ML541CS	0°C to 70°C	Molded SOIC (S24)

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