NEC

MOS INTEGRATED CIRCUIT

μPD4264805, 4265805

64 M-BIT DYNAMIC RAM
8 M-WORD BY 8-BIT, HYPER PAGE MODE

Description

The μPD4264805, 4265805 are 8,388,608 words by 8 bits CMOS dynamic RAMs with optional hyper page mode. Hyper page mode is a kind of page mode and is useful for the read operation.

The μPD4264805, 4265805 are packaged in 32-pin plastic TSOP(II) and 32-pin plastic SOJ.

Features

- Hyper page mode
- Single +3.3 V±0.3V power supply
- 8,388,608 words by 8 bits organization

Part number	Access time (MAX.)	R/W cycle time (MIN.)	Hyper page mode cycle time (MIN.)
μPD4264805-A50, 4265805-A50	50 ns	84 ns	20 ns
μPD4264805-A60, 4265805-A60	60 ns	104 ns	25 ns
μPD4264805-A70, 4265805-A70	70 ns	124 ns	30 ns

- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, Hidden refresh

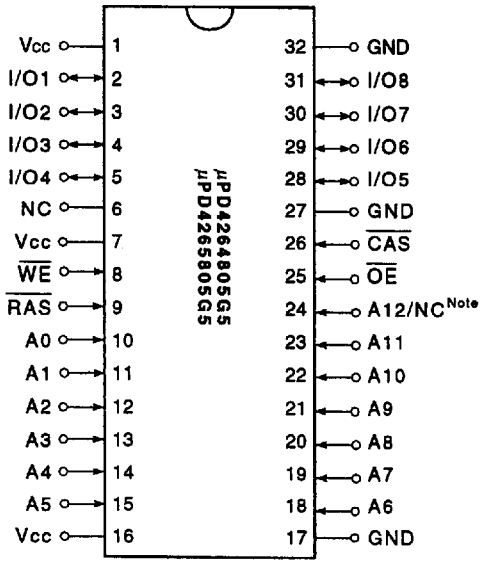
Part number	Row address	Column address	Refresh	Refresh cycle
μPD4264805	A0-A12	A0-A9	$\overline{RAS}$ only refresh, Normal Read / Write	8,192 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	4,096 cycles/64 ms
μPD4265805	A0-A11	A0-A10	$\overline{RAS}$ only refresh, Normal Read / Write	4,096 cycles/64 ms
			$\overline{CAS}$ before $\overline{RAS}$ refresh, Hidden refresh	

Ordering Information

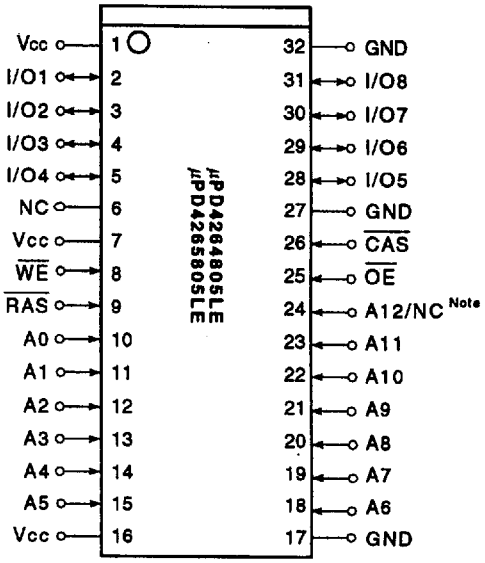
Part number	Access time (MAX.)	Package	Refresh
μPD4264805G5-A50	50 ns	32-pin Plastic TSOP(II) (400 mil)	$\overline{CAS}$ before $\overline{RAS}$ refresh $\overline{RAS}$ only refresh Hidden refresh
μPD4264805G5-A60	60 ns		
μPD4264805G5-A70	70 ns		
μPD4265805G5-A50	50 ns		
μPD4265805G5-A60	60 ns		
μPD4265805G5-A70	70 ns		
μPD4264805LE-A50	50 ns	32-pin Plastic SOJ (400 mil)	
μPD4264805LE-A60	60 ns		
μPD4264805LE-A70	70 ns		
μPD4265805LE-A50	50 ns		
μPD4265805LE-A60	60 ns		
μPD4265805LE-A70	70 ns		

Pin Configurations (Marking Side)

32-pin Plastic TSOP (II) (400 mil)



32-pin Plastic SOJ (400 mil)



Note A12...μPD4264805
NC ... μPD4265805

A0 to A12	:	Address Inputs
I/O1 to I/O8	:	Data Inputs/Outputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
$\overline{OE}$	:	Output Enable
Vcc	:	Power Supply
GND	:	Ground
NC	:	No Connection

Input/Output Pin Functions

The μPD4264805, 4265805 have input pins $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$, Address[Note 1] and input/output pins I/O1 to I/O8.

Pin name	Input/ Output	Function
$\overline{RAS}$ (Row address strobe)	Input	$\overline{RAS}$ activates the sense amplifier by latching a row address and selecting a corresponding word line. It refreshes memory cell array of one line selected by the row address. It also selects the following function. • $\overline{CAS}$ before $\overline{RAS}$ refresh
$\overline{CAS}$ (Column address strobe)		$\overline{CAS}$ activates data input/output circuit by latching column address and selecting a digit line connected with the sense amplifier.
A0 to AX[Note 1] (Address inputs)		Address bus. Input total 23-bit of address signal, upper bits and lower bits in sequence (address multiplex method). Therefore, one word is selected from 8,388,608-word by 8-bit memory cell array. In actual operation, latch row address by specifying row address and activating $\overline{RAS}$. Then, switch the address bus to column address and activate $\overline{CAS}$. Each address is taken into the device when $\overline{RAS}$ and $\overline{CAS}$ are activated. Therefore, the address input setup time (t_{ASR}, t_{ASC}) and hold time (t_{RAH}, t_{CAH}) are specified for the activation of $\overline{RAS}$ and $\overline{CAS}$.
$\overline{WE}$ (Write enable)		Write control signal. Write operation is executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
$\overline{OE}$ (Output enable)		Read control signal. Read operation can be executed by activating $\overline{RAS}$, $\overline{CAS}$ and $\overline{OE}$. If $\overline{WE}$ is activated during read operation, $\overline{OE}$ is to be ineffective in the device. Therefore, read operation cannot be executed.
I/O1 to I/O8 (Data inputs/outputs)	Input/ Output	8-bit data bus. I/O1 to I/O8 are used to input/output data.

Note1.

Part number	Address inputs	Upper bits	Lower bits
μPD4264805	A0-A12	13	10
μPD4265805	A0-A11	12	11

Hyper Page Mode

The hyper page mode is a kind of page mode with enhanced features. The two major features of the hyper page mode are as follows.

1. Data output time is extended.

   In the hyper page mode, the output data is held to the next $\overline{CAS}$ cycle's falling edge, instead of the rising edge. For this reason, valid data output time in the hyper page mode is extended compared with the fast page mode (=data extend function). In the fast page mode, the data output time becomes shorter as the $\overline{CAS}$ cycle time becomes shorter. Therefore, in the hyper page mode, the timing margin in read cycle is lager than that of the fast page mode even if the $\overline{CAS}$ cycle time becomes shorter.

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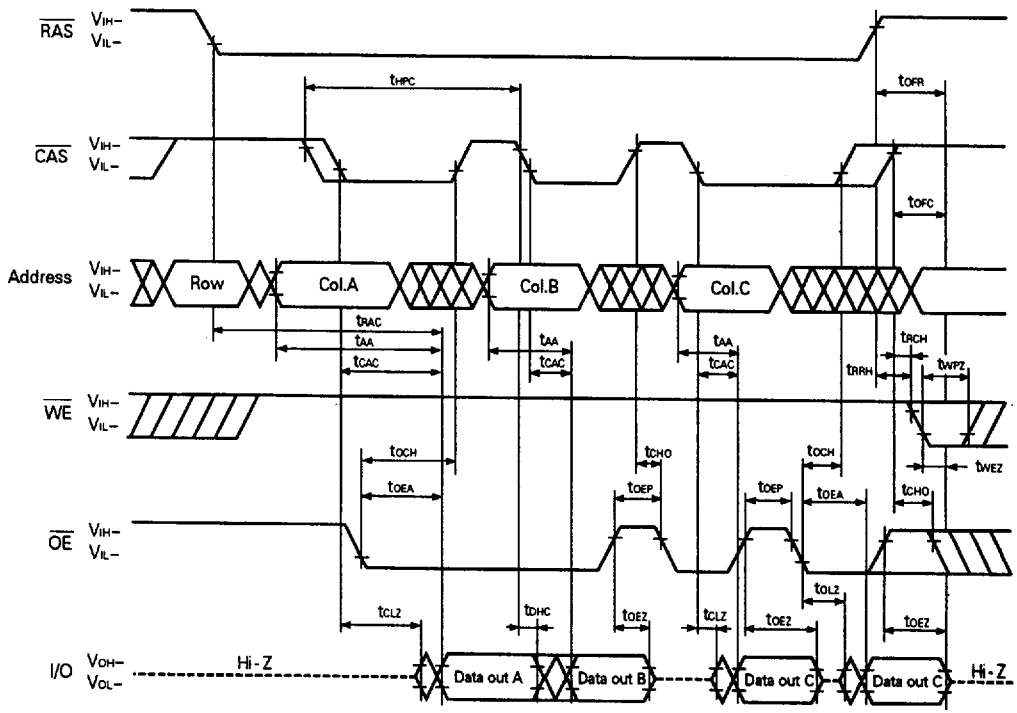
2. **The $\overline{CAS}$ cycle time in the hyper page mode is shorter than that in the fast page mode.**
   In the hyper page mode, due to the data extend function, the $\overline{CAS}$ cycle time can be shorter than in the fast page mode if the timing margin is the same.
   Taking a device whose t_{RAC} is 60 ns as an example, the $\overline{CAS}$ cycle time in the fast page mode is 25 ns while that in the fast page mode is 40 ns.
   In the hyper page mode, read (data out) and write (data in) cycles can be executed repeatedly during one $\overline{RAS}$ cycle. The hyper page mode allows both read and write operations during one cycle, but the performance is equivalent to that of the fast page mode in that case.

The following shows a part of the hyper page mode read cycle. Specifications to be observed are described in the next page.

Hyper Page Mode Read Cycle



Cautions when using the hyper page mode

1. $\overline{CAS}$ access should be used to operate t_{HPC} at the MIN. value.
2. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on the state of each signal.
   (1) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$, $\overline{OE}$: inactive ····· t_{OEZ} is effective.
   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$, $\overline{OE}$: active and either t_{RRH} or t_{RCH} must be met ····· t_{WEZ} and t_{WPZ} are effective.
3. In read cycle, the effective specification depends on the state of $\overline{CAS}$ signal when controlling data output with the $\overline{OE}$ signal.
   (1) $\overline{CAS}$: inactive, $\overline{OE}$: active ····· t_{CHO} is effective.
   (2) $\overline{CAS}$, $\overline{OE}$: active ····· t_{OCH} is effective.

Electrical Specifications

- All voltages are referenced to GND.
- After power up, wait more than 100 μs($\overline{RAS}$, $\overline{CAS}$ inactive) and then, execute eight $\overline{CAS}$ before $\overline{RAS}$ or $\overline{RAS}$ only refresh cycles as dummy cycles to initialize internal circuit.

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Voltage on Any Pin Relative to GND	V_T		−0.5 to +4.6	V
Supply Voltage	V_{CC}		−0.5 to +4.6	V
Output Current	I_O		20	mA
Power Dissipation	P_D		1	W
Operating Ambient Temperature	T_A		0 to +70	°C
Storage Temperature	T_{stg}		−55 to +125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Supply Voltage	V_{CC}		3.0	3.3	3.6	V
High Level Input Voltage	V_{IH}		2.0		V_{CC} +0.3	V
Low Level Input Voltage	V_{IL}		−0.3		+0.8	V
Operating Ambient Temperature	T_A		0		70	°C

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Capacitance	C_{I1}	Address			5	pF
	C_{I2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$			7	pF
Data Input/Output Capacitance	$C_{I/O}$	I/O			7	pF

DC Characteristics (Recommended Operating Conditions unless otherwise noted) [μPD4264805]

Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		105	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		95		
		I_O = 0 mA	t_{RAC} = 70 ns		85		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH (MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		105	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH (MIN.)}$	t_{RAC} = 60 ns		95		
		t_{RC} = $t_{RC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL (MAX.)}$	t_{RAC} = 50 ns		105	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		95		
		t_{HPC} = $t_{HPC (MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2
		t_{RC} = $t_{RC (MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Input leakage current	$I_{I (L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O (L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

[μPD4265805]

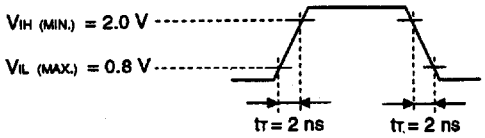
Parameter	Symbol	Test condition		MIN.	MAX.	Unit	Notes
Operating current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2,3
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Standby current	I_{CC2}	$\overline{RAS}$, $\overline{CAS}$ ≧ $V_{IH(MIN.)}$	I_O = 0 mA		1.0	mA	
		$\overline{RAS}$, $\overline{CAS}$ ≧ V_{CC} – 0.2 V	I_O = 0 mA		0.5		
$\overline{RAS}$ only refresh current	I_{CC3}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2,3,4
		$\overline{CAS}$ ≧ $V_{IH(MIN.)}$	t_{RAC} = 60 ns		115		
		t_{RC} = $t_{RC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		105		
Operating current (Hyper page mode)	I_{CC4}	$\overline{RAS}$ ≦ $V_{IL(MAX.)}$	t_{RAC} = 50 ns		105	mA	1,2,5
		$\overline{CAS}$ Cycling	t_{RAC} = 60 ns		95		
		t_{HPC} = $t_{HPC(MIN.)}$ I_O = 0 mA	t_{RAC} = 70 ns		85		
$\overline{CAS}$ before $\overline{RAS}$ refresh current	I_{CC5}	$\overline{RAS}$ Cycling	t_{RAC} = 50 ns		135	mA	1,2
		t_{RC} = $t_{RC(MIN.)}$	t_{RAC} = 60 ns		115		
		I_O = 0 mA	t_{RAC} = 70 ns		105		
Input leakage current	$I_{I(L)}$	V_I = 0 to 3.6 V all other pins not under test = 0 V		–5	+5	μA	
Output leakage current	$I_{O(L)}$	V_O = 0 to 3.6 V Output is disabled (Hi-Z)		–5	+5	μA	
High level output voltage	V_{OH}	I_O = –2.0 mA		2.4		V	
Low level output voltage	V_{OL}	I_O = +2.0 mA			0.4	V	

Notes
1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on cycle rates (t_{RC} and t_{HPC}).
2. Specified values are obtained with outputs unloaded.
3. I_{CC1} and I_{CC3} are measured assuming that address can be changed once or less during $\overline{RAS}$ ≦ $V_{IL(MAX.)}$ and $\overline{CAS}$ ≧ $V_{IH(MIN.)}$.
4. I_{CC3} is measured assuming that all column address inputs are held at either high or low.
5. I_{CC4} is measured assuming that all column address inputs are switched only once during each hyper page cycle.

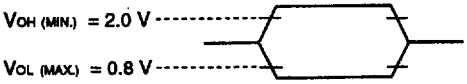
AC Characteristics (Recommended Operating Conditions unless otherwise noted)

AC Characteristics Test Conditions

(1) Input timing specification



(2) Output timing specification



(3) Loading conditions are 100 pF + 1 TTL.

Common to Read, Write, Read Modify Write Cycle

Parameter	Symbol	tRAC = 50 ns		tRAC = 60 ns		tRAC = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	tRC	84	—	104	—	124	—	ns	
$\overline{RAS}$ Precharge Time	tRP	30	—	40	—	50	—	ns	
$\overline{CAS}$ Precharge Time	tCPN	7	—	10	—	10	—	ns	
$\overline{RAS}$ Pulse Width	tRAS	50	10 000	60	10 000	70	10 000	ns	
$\overline{CAS}$ Pulse Width	tCAS	7	10 000	10	10 000	12	10 000	ns	
$\overline{RAS}$ Hold Time	tRSH	10	—	10	—	12	—	ns	
$\overline{CAS}$ Hold Time	tCSH	38	—	40	—	50	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	tRCD	11	37	14	45	14	52	ns	1
$\overline{RAS}$ to Column Address Delay Time	tRAD	9	25	12	30	12	35	ns	1
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	tCRP	5	—	5	—	5	—	ns	2
Row Address Setup Time	tASR	0	—	0	—	0	—	ns	
Row Address Hold Time	tRAH	7	—	10	—	10	—	ns	
Column Address Setup Time	tASC	0	—	0	—	0	—	ns	
Column Address Hold Time	tCAH	7	—	10	—	12	—	ns	
$\overline{OE}$ Lead Time Referenced to $\overline{RAS}$	tOES	0	—	0	—	0	—	ns	
$\overline{CAS}$ to Data Setup Time	tCLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Setup Time	tOLZ	0	—	0	—	0	—	ns	
$\overline{OE}$ to Data Delay Time	tOED	10	—	13	—	15	—	ns	
Transition Time (Rise and Fall)	tT	1	50	1	50	1	50	ns	
Refresh Time	tREF	—	64	—	64	—	64	ms	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. $t_{CRP(MIN.)}$ requirement is applied to $\overline{RAS}$, $\overline{CAS}$ cycles.

Read Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Access Time from $\overline{RAS}$	t_{RAC}	—	50	—	60	—	70	ns	1
Access Time from $\overline{CAS}$	t_{CAC}	—	13	—	15	—	18	ns	1
Access Time from Column Address	t_{AA}	—	25	—	30	—	35	ns	1
Access Time from $\overline{OE}$	t_{OEA}	—	13	—	15	—	18	ns	
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	0	—	0	—	0	—	ns	2
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0	—	0	—	0	—	ns	2
Output Buffer Turn-off Delay Time from $\overline{OE}$	t_{OEZ}	0	10	0	13	0	15	ns	3
$\overline{CAS}$ Hold Time to $\overline{OE}$	t_{CHO}	5	—	5	—	5	—	ns	

Notes 1. For read cycles, access time is defined as follows:

Input Conditions	Access Time	Access Time from $\overline{RAS}$
$t_{RAD} \leqq t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{RAC\ (MAX.)}$	$t_{RAC\ (MAX.)}$
$t_{RAD} > t_{RAD\ (MAX.)}$ and $t_{RCD} \leqq t_{RCD\ (MAX.)}$	$t_{AA\ (MAX.)}$	$t_{RAD} + t_{AA\ (MAX.)}$
$t_{RCD} > t_{RCD\ (MAX.)}$	$t_{CAC\ (MAX.)}$	$t_{RCD} + t_{CAC\ (MAX.)}$

$t_{RAD(MAX.)}$ and $t_{RCD(MAX.)}$ are specified as reference points only ; they are not restrictive operating parameters. They are used to determine which access time (t_{RAC}, t_{AA} or t_{CAC}) is to be used for finding out when output data will be available. Therefore, the input conditions $t_{RAD} \geqq t_{RAD(MAX.)}$ and $t_{RCD} \geqq t_{RCD(MAX.)}$ will not cause any operation problems.

2. Either $t_{RCH(MIN.)}$ or $t_{RRH(MIN.)}$ should be met in read cycles.
3. $t_{OEZ(MAX.)}$ defines the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Hold Time Referenced to $\overline{CAS}$	t_{WCH}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Pulse Width	t_{WP}	7	—	10	—	10	—	ns	1
$\overline{WE}$ Lead Time Referenced to $\overline{RAS}$	t_{RWL}	10	—	10	—	12	—	ns	
$\overline{WE}$ Lead Time Referenced to $\overline{CAS}$	t_{CWL}	7	—	10	—	12	—	ns	
$\overline{WE}$ Setup Time	t_{WCS}	0	—	0	—	0	—	ns	2
$\overline{OE}$ Hold Time	t_{OEH}	0	—	0	—	0	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	3
Data-in Hold Time	t_{DH}	7	—	10	—	10	—	ns	3

Notes 1. $t_{WP(MIN.)}$ is applied to late write cycles or read modify write cycles. In early write cycles, $t_{WCH(MIN.)}$ should be met.

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle.

3. $t_{DS(MIN.)}$ and $t_{DH(MIN.)}$ are referenced to the $\overline{CAS}$ falling edge in early write cycles. In late write cycles and read modify write cycles, they are referenced to the $\overline{WE}$ falling edge.

Read Modify Write Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read Modify Write Cycle Time	t_{RWC}	107	—	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{WE}$ Delay Time	t_{RWD}	64	—	77	—	89	—	ns	1
$\overline{CAS}$ to $\overline{WE}$ Delay Time	t_{CWD}	27	—	32	—	37	—	ns	1
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	39	—	47	—	54	—	ns	1

Note 1. If $t_{WCS} \geqq t_{WCS(MIN.)}$ the cycle is an early write cycle and the data out will remain Hi-Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

Hyper Page Mode

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Notes
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read / Write Cycle Time	t_{HPC}	20	—	25	—	30	—	ns	1
$\overline{RAS}$ Pulse Width	t_{RASP}	50	125 000	60	125 000	70	125 000	ns	
$\overline{CAS}$ Pulse Width	t_{HCAS}	7	10 000	10	10 000	12	10 000	ns	
$\overline{CAS}$ Precharge Time	t_{CP}	7	—	10	—	10	—	ns	
Access Time from $\overline{CAS}$ Precharge	t_{ACP}	—	30	—	35	—	40	ns	
$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	t_{CPWD}	41	—	52	—	59	—	ns	2
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	30	—	35	—	40	—	ns	
Read Modify Write Cycle Time	t_{HPRWC}	52	—	66	—	75	—	ns	
Data Output Hold Time	t_{DHC}	5	—	5	—	5	—	ns	
$\overline{OE}$ to CAS Hold Time	t_{OCH}	5	—	5	—	5	—	ns	
$\overline{OE}$ Precharge Time	t_{OEP}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Delay from $\overline{WE}$	t_{WEZ}	0	10	0	13	0	15	ns	3,4
$\overline{WE}$ Pulse Width	t_{WPZ}	7	—	10	—	10	—	ns	4
Output Buffer Turn-off Delay from $\overline{RAS}$	t_{OFR}	0	10	0	13	0	15	ns	3.4
Output Buffer Turn-off Delay from $\overline{CAS}$	t_{OFC}	0	10	0	13	0	15	ns	3.4

Notes 1. $t_{HPC(MIN.)}$ is applied to access time from $\overline{CAS}$

2. If $t_{WCS} \geqq t_{WCS(MIN.)}$, the cycle is an early write cycle and the data out will remain Hi - Z through the entire cycle. If $t_{RWD} \geqq t_{RWD(MIN.)}$, $t_{CWD} \geqq t_{CWD(MIN.)}$, $t_{AWD} \geqq t_{AWD(MIN.)}$, and $t_{CPWD} \geqq t_{CPWD(MIN.)}$, the cycle is a read modify write cycle and the data out will contain data read from the selected cell. If neither of the above conditions is met, the state of the data out is indeterminate.

3. $t_{OFC(MAX.)}$, $t_{OFR(MAX.)}$ and $t_{WEZ(MAX.)}$ define the time when the output achieves the condition of Hi-Z and is not referenced to V_{OH} or V_{OL}.

4. To make I/Os to Hi-Z in read cycle, it is necessary to control $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ as follows. The effective specification depends on state of each signal.

   (1) $\overline{RAS}$, $\overline{CAS}$: Inactive (at the end of read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: active
   t_{OFC} is effective when $\overline{RAS}$ is inactivated before $\overline{CAS}$ is inactivated.
   t_{OFR} is effective when $\overline{CAS}$ is inactivated before $\overline{RAS}$ is inactivated.

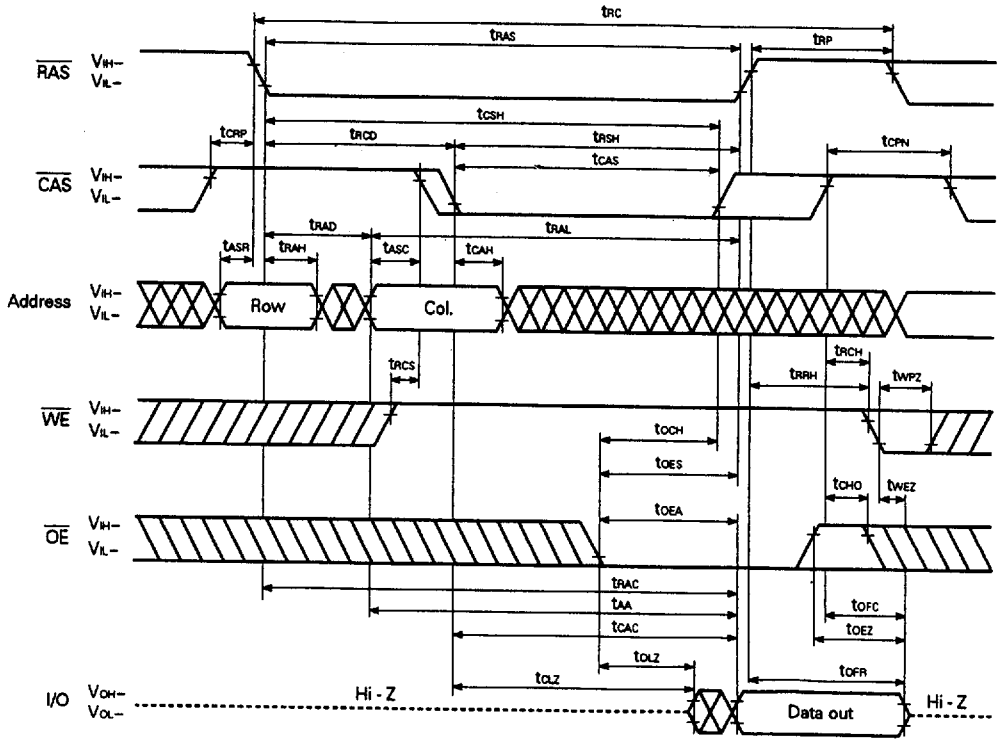
   (2) Both $\overline{RAS}$ and $\overline{CAS}$ are active or either $\overline{RAS}$ or $\overline{CAS}$ is active (in read cycle)
   $\overline{WE}$: inactive, $\overline{OE}$: inactive ··· t_{OEZ} is effective.

   (3) Both $\overline{RAS}$ and $\overline{CAS}$ are inactive or $\overline{RAS}$ is active and $\overline{CAS}$ is inactive (at the end of read cycle)
   $\overline{WE}$,$\overline{OE}$:active and either t_{RRH} or t_{RCH} must be met··· t_{WEZ}, t_{WPZ} are effective.

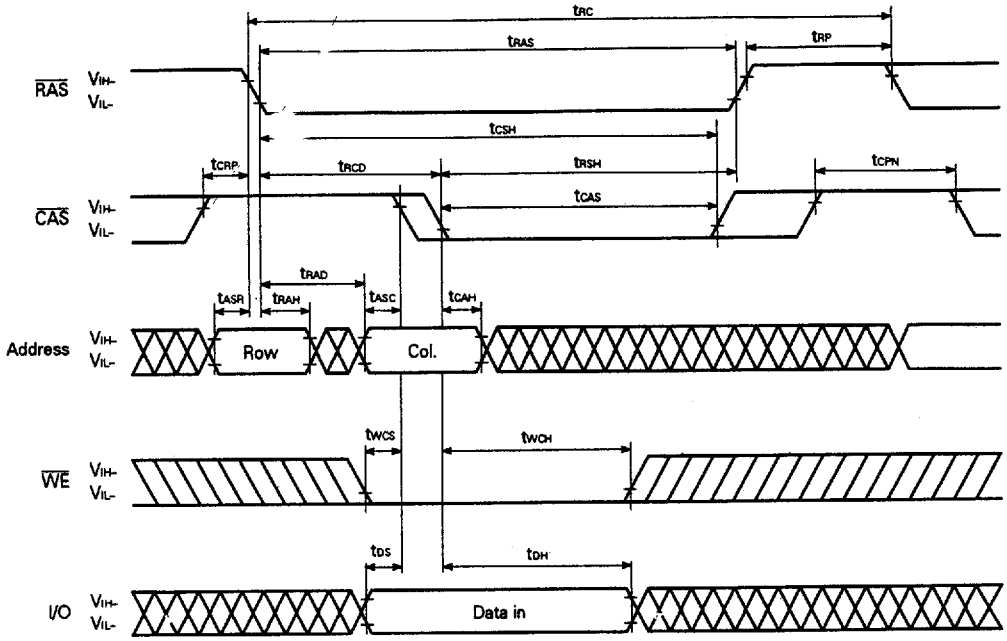
Refresh Cycle

Parameter	Symbol	t_{RAC} = 50 ns		t_{RAC} = 60 ns		t_{RAC} = 70 ns		Unit	Note
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\overline{CAS}$ Setup Time	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{WE}$ Setup Time	t_{WSR}	10	—	10	—	10	—	ns	
$\overline{WE}$ Hold Time (Hidden Refresh Cycle)	t_{WHR}	15	—	15	—	15	—	ns	

Read Cycle

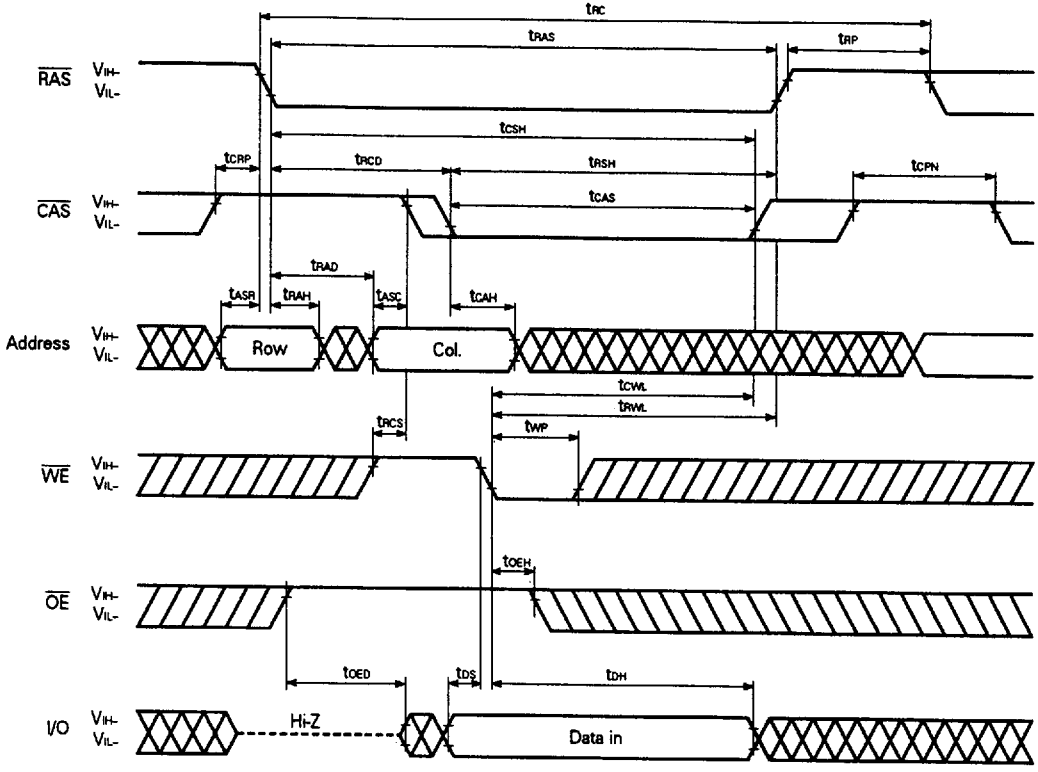

tRC
tRAS
tRP
RAS
VIH–
VIL–
tCSH
tCRP
tRCD
tRSH
tCAS
tCPN
CAS
tRAD
tRAL
tASR
tRAH
tASC
tCAH
Address
Row
Col.
tRCS
tRCH
tRRH
tWPZ
WE
tOCH
tOES
tCHO
tWEZ
OE
tOEA
tRAC
tAA
tCAC
tOFC
tOEZ
tOLZ
tOFR
I/O
VOH–
VOL–
Hi-Z
Data out
Hi-Z

Early Write Cycle

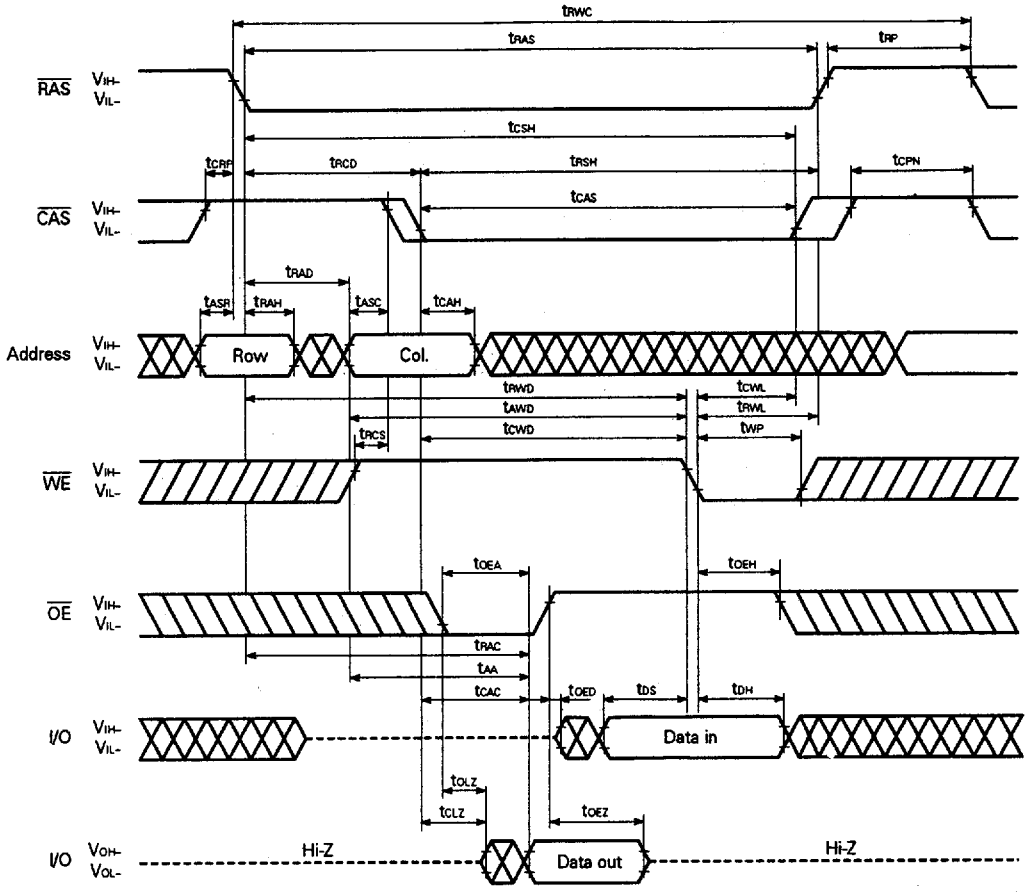


Remark $\overline{OE}$: Don't care

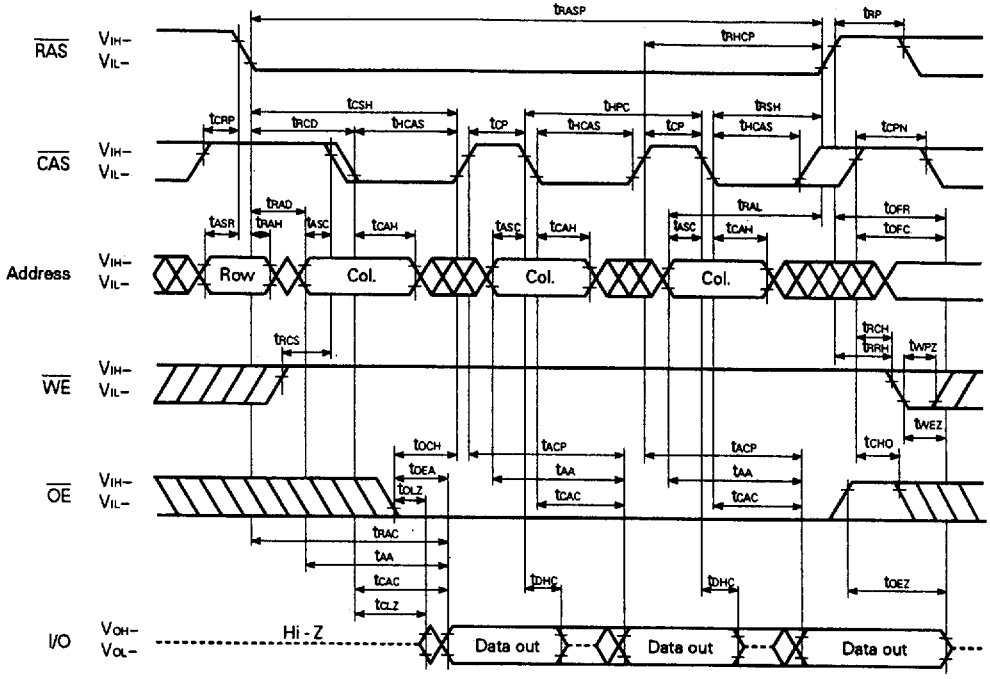
Late Write Cycle



Read Modify Write Cycle

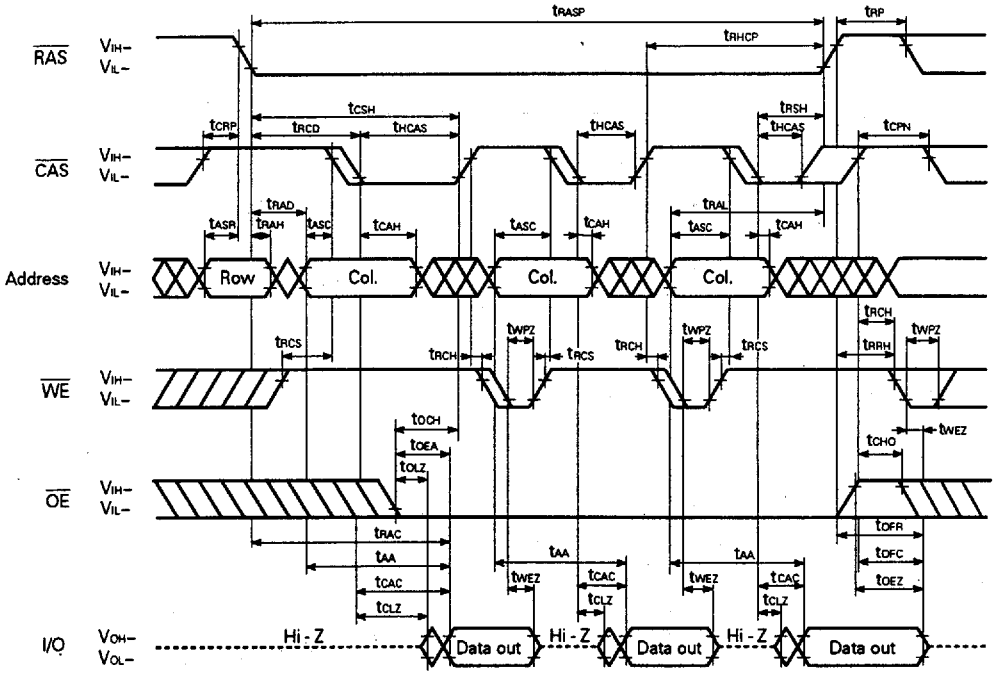


Hyper Page Mode Read Cycle



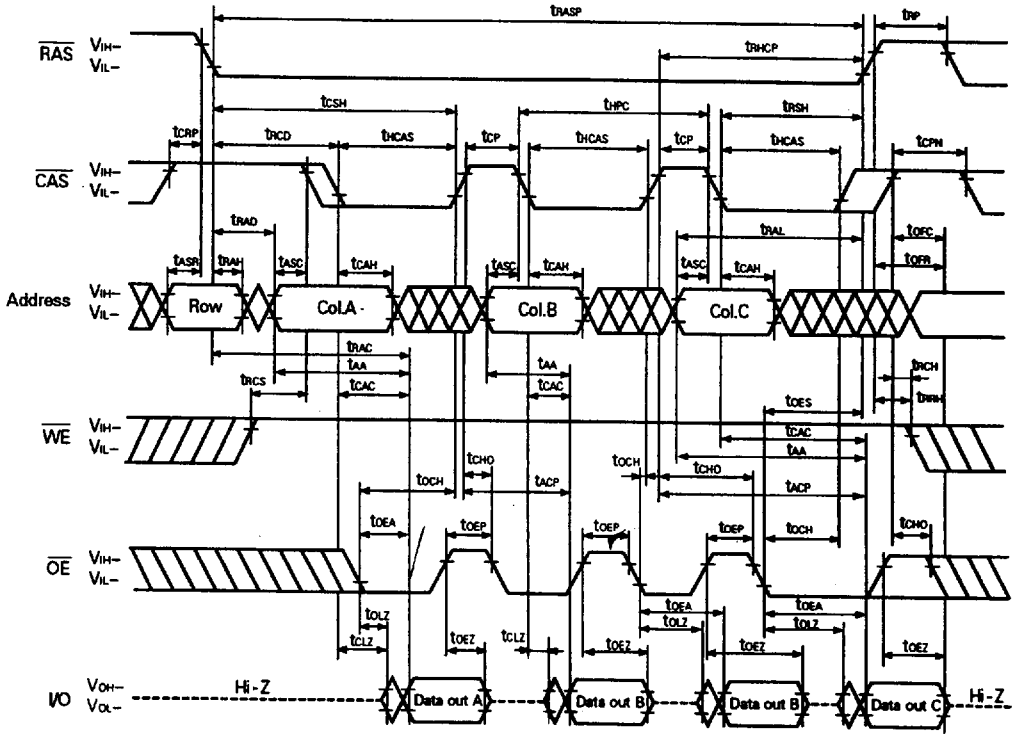
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{WE}$ Control)



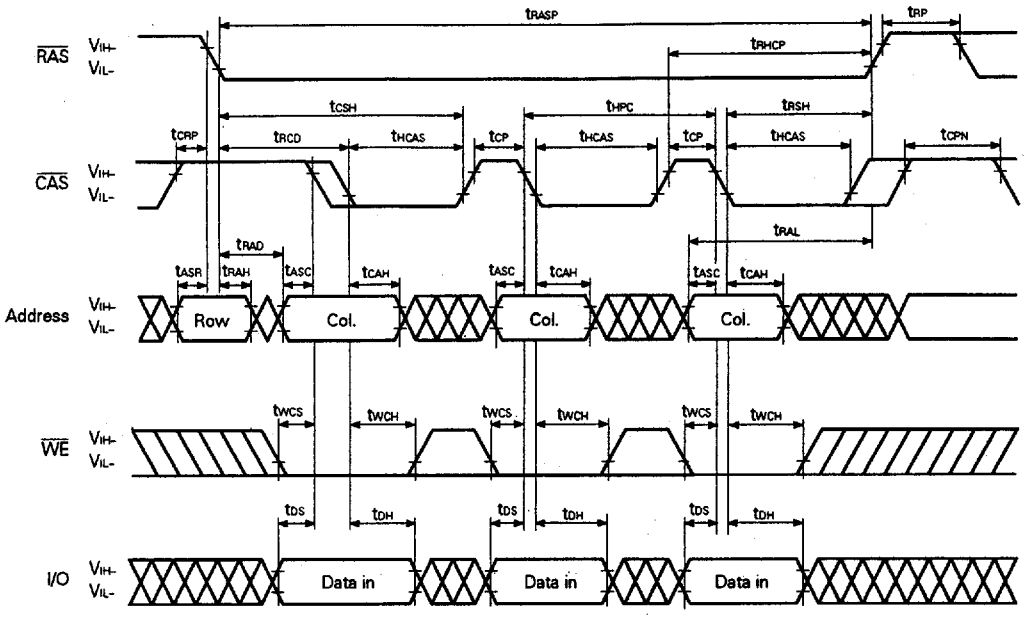
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Cycle ($\overline{OE}$ Control)



Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

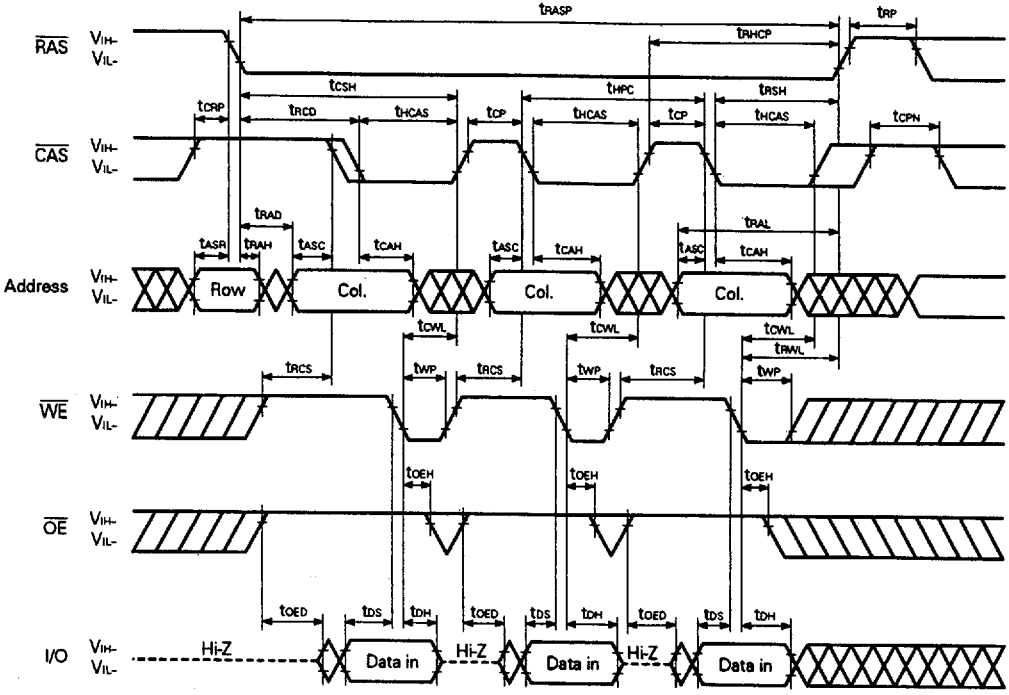
Hyper Page Mode Early Write Cycle



Remarks 1. $\overline{OE}$: Don't care

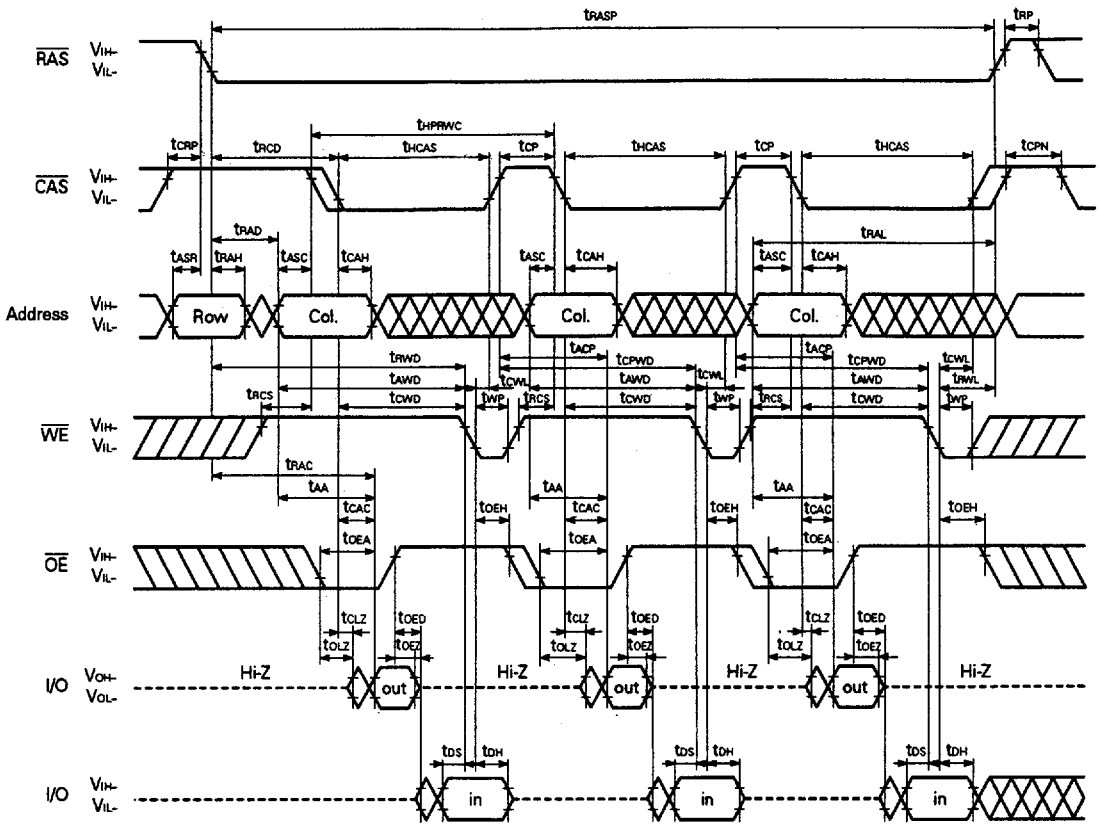
2. In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Late Write Cycle



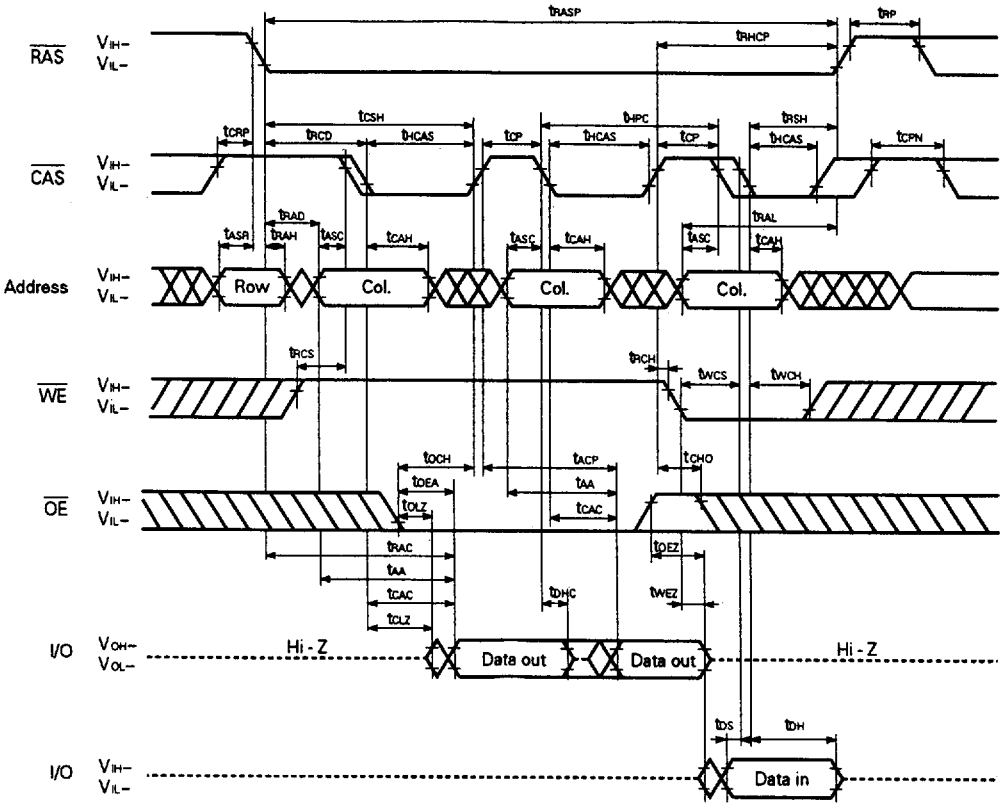
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read Modify Write Cycle



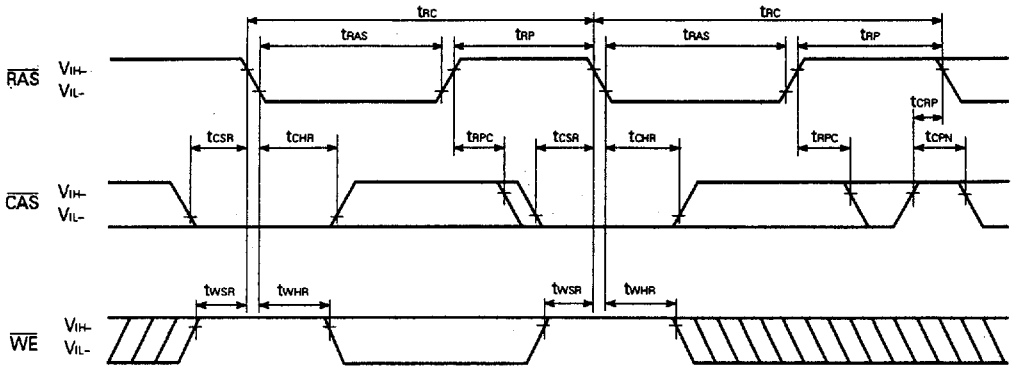
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

Hyper Page Mode Read and Write Cycle



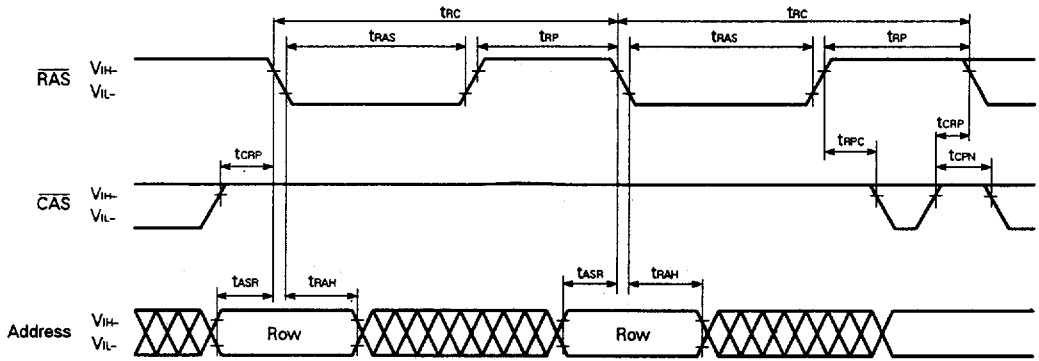
Remark In the hyper page mode, read, write and read modify write cycles are available for each of the consecutive $\overline{CAS}$ cycles within the same $\overline{RAS}$ cycle.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



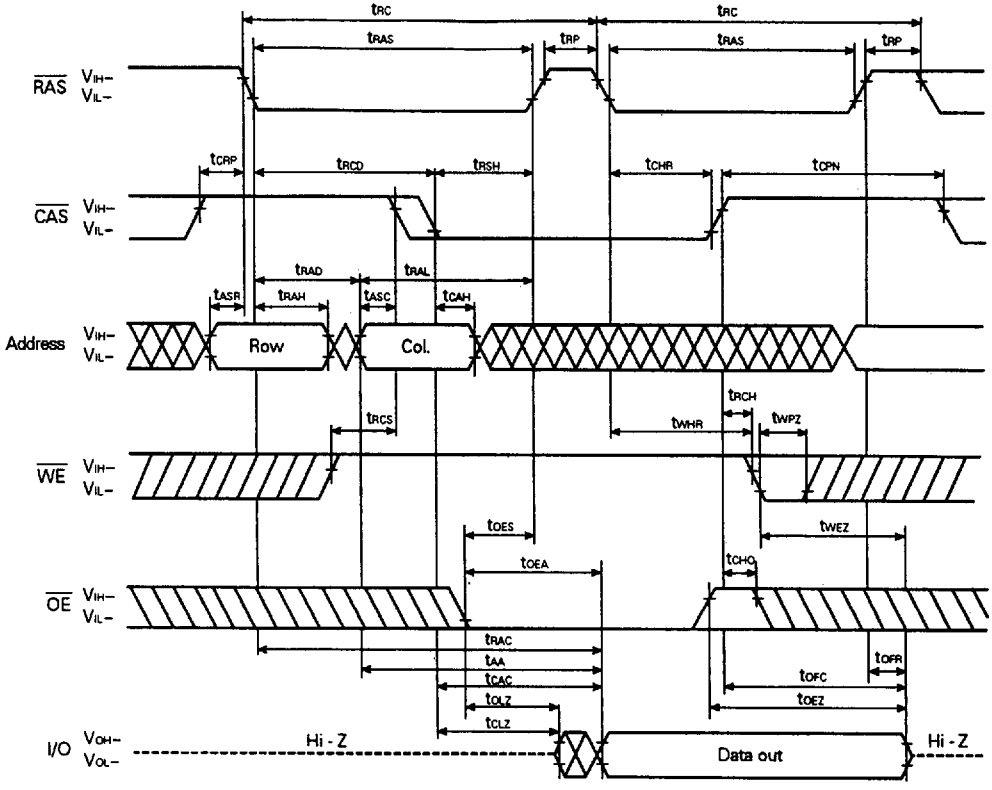
Remark Address, $\overline{OE}$: Don't care I/O: Hi-Z

$\overline{RAS}$ Only Refresh Cycle

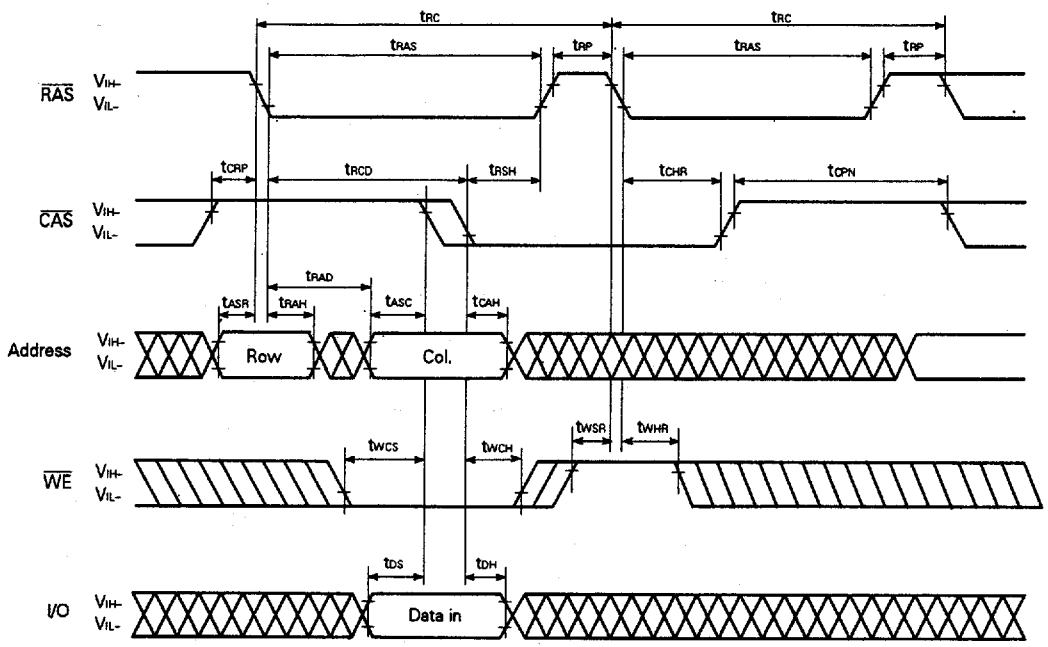


Remark $\overline{WE}$, $\overline{OE}$: Don't care I/O: Hi-Z

Hidden Refresh Cycle (Read)



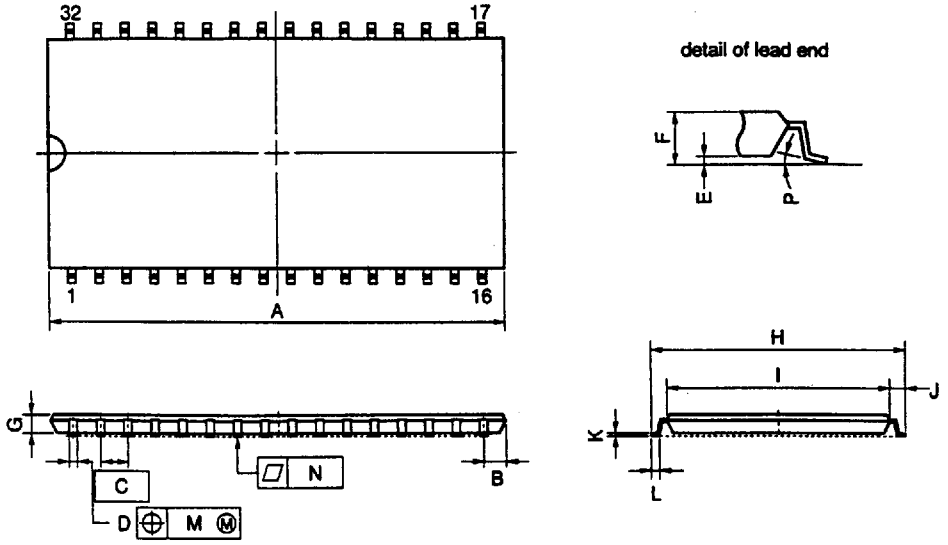
Hidden Refresh Cycle (Write)



Remark $\overline{OE}$: Don't care

Package Drawings

32PIN PLASTIC TSOP(II) (400 mil)



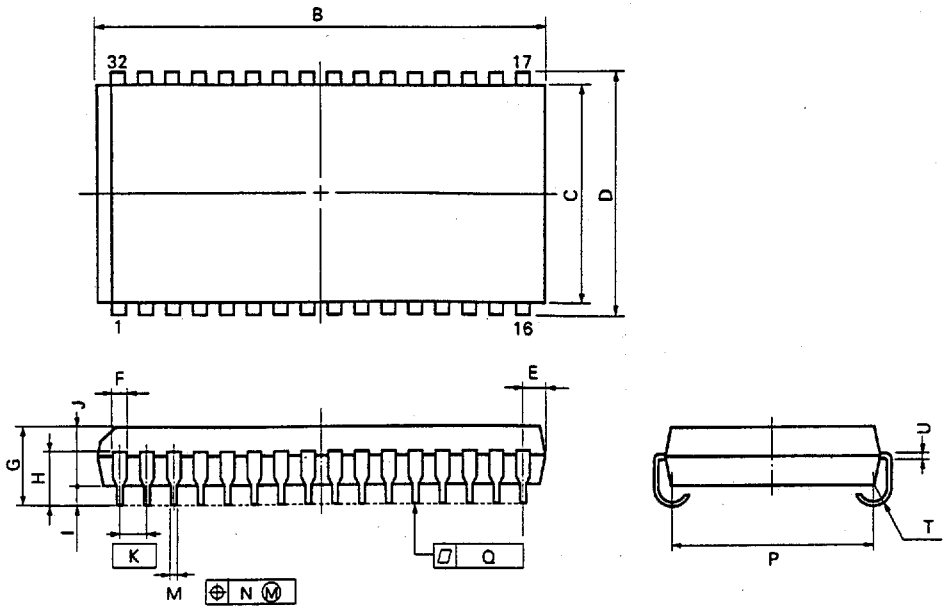
NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	21.17 MAX.	0.834 MAX.
B	1.075 MAX.	0.043 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.42^{+0.08}_{-0.07}$	0.017±0.003
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	0.97	0.038
H	11.76±0.2	0.463±0.008
I	10.16±0.1	0.400±0.004
J	0.8±0.2	$0.031^{+0.009}_{-0.008}$
K	$0.145^{+0.025}_{-0.015}$	0.006±0.001
L	0.5±0.1	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

S32G5-50-7JD2

32 PIN PLASTIC SOJ (400 mil)



P32LE-400A

ITEM	MILLIMETERS	INCHES
B	21.06±0.2	0.829±0.008
C	10.16	0.400
D	11.18±0.2	0.440±0.008
E	1.005±0.1	$0.040^{+0.004}_{-0.005}$
F	0.74	0.029
G	3.5±0.2	0.138±0.008
H	2.545±0.2	0.100±0.008
I	0.8 MIN.	0.031 MIN.
J	2.6	0.102
K	1.27 (T.P.)	0.050 (T.P.)
M	0.40±0.10	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	9.4±0.20	0.370±0.008
Q	0.1	0.004
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.