VTC Inc.
Value the Customer™

VM64110
DIGITAL READ/WRITE CHANNEL

August, 1994

FEATURES

- Channel Rate Operation From 30 to 120 MHz
- Compatible With Any d = 0 RLL Code
- Full Support for Zone Density Recording
- Digitally Controlled VGA for Data and Servo Gain Control
- Digitally Controlled VFO with Zero-Phase-Restart for Clock Recovery
- Programmable Active Filter with Variable Cutoff and Boost
- 6-Bit 120 MSamples/s Flash ADC
- Optional Envelope Follower Servo Demodulation Mode
- Write Precompensation for Three, 3-bit Patterns
- Frequency Synthesizer with 8-Bit Divider Resolution
- Serial-Interfaced Control Registers with Readback Capability
- Power Management Features
- TTL Compatible Control I/O
- Differential ECL-Like Datapath I/O With Programmable Load
- Minimum Number of Off-Chip Discrete Components (5)
- Operation From a Single 5V Supply

DESCRIPTION

The VM64110 is the analog half of a digital read/write channel chip set for hard disk drive applications and can be used with any compatibly designed digital chip. The chip provides for a high degree of user programmability allowing the customization of the chip to suit any specific application.

The VM64110 is fabricated in VTC's PolarMOS process which offers high-performance bipolar and MOS devices for precision analog circuitry, and low-power CMOS technology for digital control functions. The VM64110 operates off a single 5-Volt supply and dissipates between 0.6W and 1.5W depending upon operating conditions. In the sleep mode the power dissipation is reduced to 2.5mW. The VM64110 is available in a 64-pin Plastic Quad Flatpack.

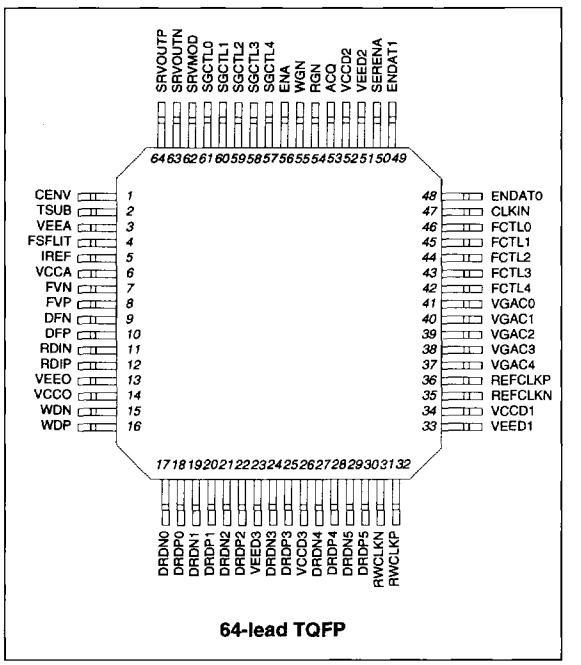
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage:
V_{CC} ..... -0.3V to +7V
Input Voltages:
Digital Input Voltage V_{IN} ..... -0.3V to +7V
Storage Temperature T_{stg} .....-65° to 150°C
Junction Temperature T_J ..... 150°C
Thermal Impedance, Θ_{JA}
64-Lead PQFP ..... 40°C/W

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage:
V_{CC} .....+5V ± 10%
Junction Temperature T_J ..... 0°C to 125°C

CONNECTION DIAGRAM



64-lead TQFP

FUNTIONAL DESCRIPTION

The chip receives differential analog read data input from a read/write preamp on pins RDIP and RDIN, and amplifies it with a digitally controlled variable gain amplifier (VGA). The five VGAC pins, along with five control register bits, control the gain of the VGA. The VGA output is equalized and filtered in a programmable active filter. The user specifies cutoff frequency and boost via the control register. The filter output is sampled by a 6-bit analog-to-digital converter (ADC). The sampling clock is generated by a digitally controlled variable-frequency oscillator (VFO) operating at the channel rate frequency. The 5-bit FCTL bus modulates the frequency of the VFO digitally. The ADC is output on the differential ECL DRD pins while the sampling clock is output on the read/write reference clock RWCLK, also differential ECL compatible. Signal swing on these pins is reduced to 0.5V from the standard 0.9V to reduce power dissipation. Offset through the datapath is minimized by the use of AC coupling capacitors on the filter output and an offset control word in the ADC.

A frequency synthesizer, composed of a charge-pump-based phase-locked loop, provides a reference for the VFO and generates the write reference clock output on RWCLK during write and idle mode. The center frequency for the voltage controlled oscillator (VCO) of the synthesizer is programmed by a digital-to-analog converter (DAC) which scales an external current provided by a resistor connected from V_{CC} to the IREF pin. Two

DATA RECOVERY CIRCUITS

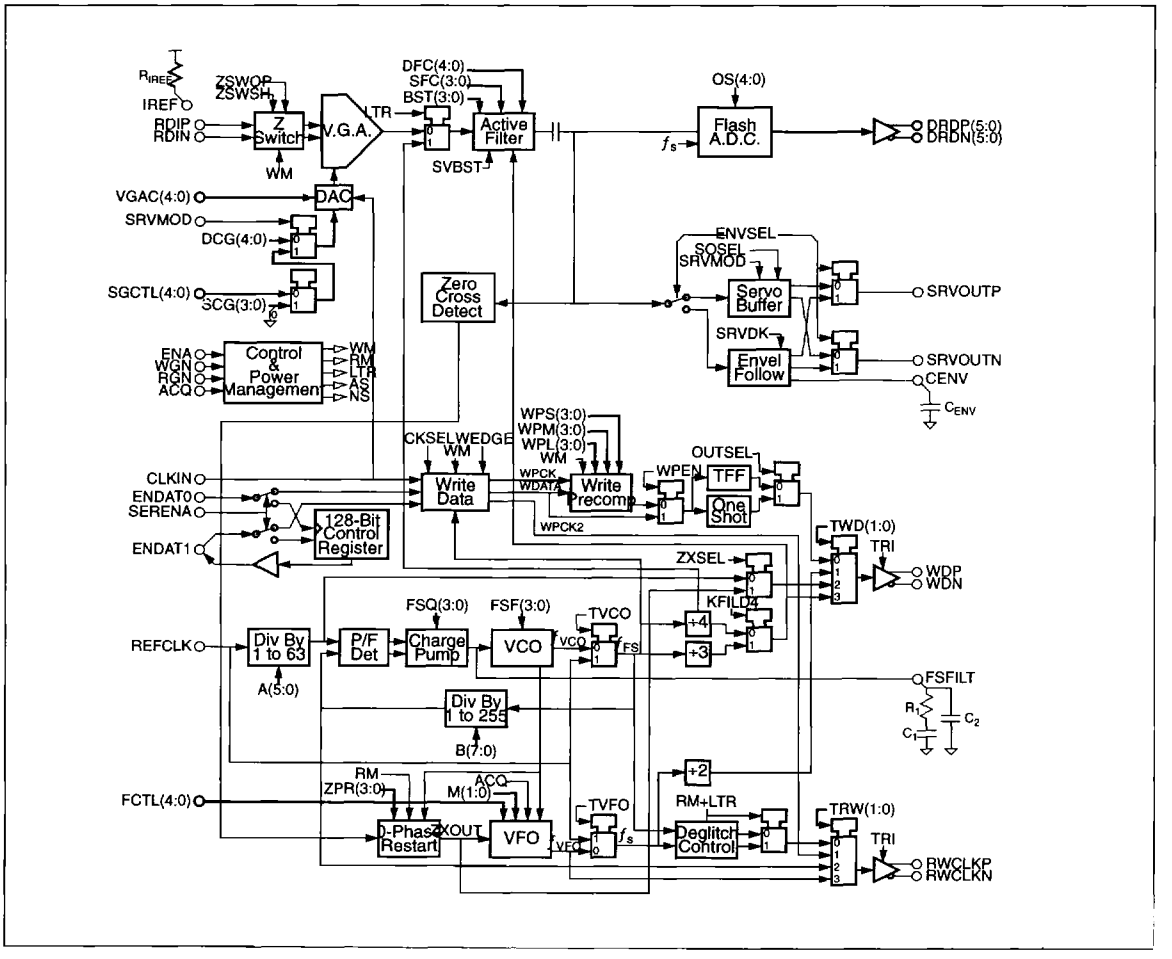
programmable dividers, A and B, allow the input frequency on the REFCLK pin to be multiplied up to the desired frequency with 8-bit resolution. The A and B dividers, the frequency DAC, and a DAC for the charge pump, are all programmed via the control register.

Write Precompensation for non-linear bit shift is provided for the 2-bit parallel write data inputs ENDAT1 and ENDAT0 and output on pins WDP and WDN. A parallel-to-serial conversion is made and a 3-bit pattern is detected. Three different user-programmable 4-bit DAC's control the shift for three unique patterns '010', '110', and '111'. The middle '1' is shifted late by an amount set by the corresponding DAC in the serial control register. A '011' pattern is uncompensated. Serial, precompensated write data is output on WD. A T-flip-flop may be optionally inserted into the output datapath.

Pin SRVMOD places the part in servo mode. A five-bit parallel interface on pins SGCTL(4:0) allows for direct control of the VGA DAC, overriding the serial coarse gain bits and disabling the VGAC fine gain inputs. Separate control bits for filter cutoff and boost are enabled. Pins SRVOUTP,N output the servo filter signal for off-chip demodulation. An optional envelope follower mode is enabled through the ENVSEL bit in the serial control register where the demodulated servo signal is output on the SRVOUTP pin along with appropriate reference voltages on the SRVOUTN pin. A zero-cross detector provides an edge for zero-phase restart corresponding to the positive zero-crossing of the filtered output.

The ENA pin provides for a Sleep mode, or an optional Nap mode, so that the chip can be put into a low power mode (<2.5mW). A Reset mode allows the chip to be reinitialized. A number of control register bits can disable the various blocks of the chip both independently and as a function of mode. The read gate and write gate pins, RGN and WGN, control the mode of the chip (Read, Write, or Idle). An acquisition pin ACQ specifies acquisition or tracking when in read mode and defines a lock-to-reference mode (LTR) when in idle. The serial enable pin (SERENA), along with the serial clock (SERCLK) and serial data pin (SERDAT), controls the loading and readback of the control register via the serial interface. Due to pin limitations, SERCLK and SERDAT are multiplexed with ENDAT0 and ENDAT1 respectively.

BLOCK DIAGRAM



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