July 1990
Edition 3.0

FUJITSU

DATA SHEET

MB8421/8422-90/-90L/-90LL/-12/-12L/-12LL
CMOS 16K-BIT DUAL-PORT SRAM

2K x 8 Bits CMOS Dual-Port Static Random Access Memory

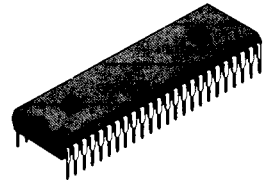
The Fujitsu MB8421 and MB8422 are 2,048 words x 8 bits dual-port high-performance static random access memories (SRAMs) fabricated in CMOS. The SRAMs use asynchronous circuits; thus, no external clocks are required. MB8421 and MB8422 provide the user with two separately controlled I/O ports with independent addresses, Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$), Output Enable ($\overline{OE}$), and I/O functions. This arrangement permits independent access to any memory location for either a Read or Write operation – a useful feature for shared data processing applications. These devices have an automatic power-down feature controlled by $\overline{CS}$.

To avoid data contention on the same address, a $\overline{BUSY}$ input is provided for address arbitration; in addition, MB8421 utilizes an interrupt ($\overline{INT}$) flag which allows communication between systems on either side of the RAM. Both devices use a single +5 V power supply and all pins are TTL-compatible.

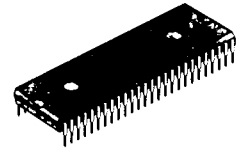
Some typical applications for these memory devices are multiprocessing systems, distributed networks, external register files, and peripheral controllers.

- Organization: 2,048 words x 8 bits
- Static operation: no clocks or timing strobe required
- Access time: $t_{AA} = t_{ACS} = 90$ ns max. (MB8421/22-90)
  (MB8421/22-90L)
  (MB8421/22/-90LL)

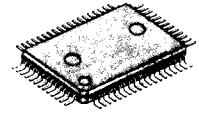
  $t_{AA} = t_{ACS} = 120$ ns max. (MB8421/22-12)
  (MB8421/22-12L)
  (MB8421/22/-12LL)
- Power consumption for the standard version:
  660 mW max. (Both ports active)
  385 mW max. (One port active)
  38.5 mW max. (Both ports standby, TTL)
  11 mW max. (Both ports standby, CMOS)
- Power consumption for the L and LL-versions:
  495 mW max. (Both ports active)
  275 mW max. (One port active)
  27.5 mW max. (Both ports standby, TTL)
  1.1 mW max. (Both ports standby, CMOS)
- Single +5 V power supply ±10% tolerance
- TTL compatible inputs and outputs
- Three-state outputs with OR-tie capacity
- Electrostatic protection for all inputs and outputs
- Address arbitration function: $\overline{BUSY}$ flag
- Interrupt function for communication between systems (*MB8421 only*): $\overline{INT}$ flag
- Data retention voltage: 2 V min.
- Standard Plastic Packages:
  48-pin DIP MB8422-xx(L/LL)P
  52-pin DIP MB8421-xx(L/LL)P
  64-pin QFP MB8421-xx(L/LL)PFQ



DIP-48P-M02
(MB8422)



DIP-52P-M01
(MB8421)



FPT-64P-M06
(MB8421)

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This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

ABSOLUTE MAXIMUM RATINGS [1, 2]

Parameter	Designator	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7	V
Input Voltage on any pin with respect to V_{SS}	VIN	-0.5 to V_{CC} +0.5	V
Output Voltage on any I/O pin with respect to V_{SS}	VOUT	-0.5 to V_{CC} +0.5	V
Output Current	IOUT	± 20	mA
Power dissipation	PD	1.0	W
Temperature Under Bias	TBIAS	-10 to +85	°C
Storage Temperature	TSTG	-40 to +125	

NOTE:
Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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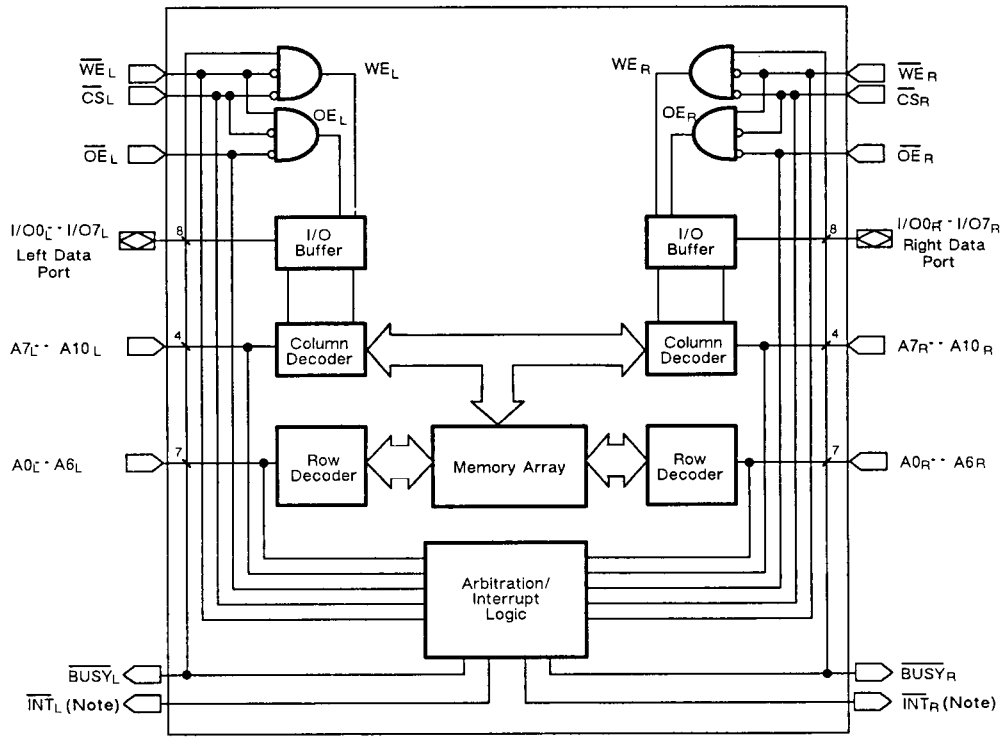
Fig. 1 — BLOCK DIAGRAM OF MB8421/22

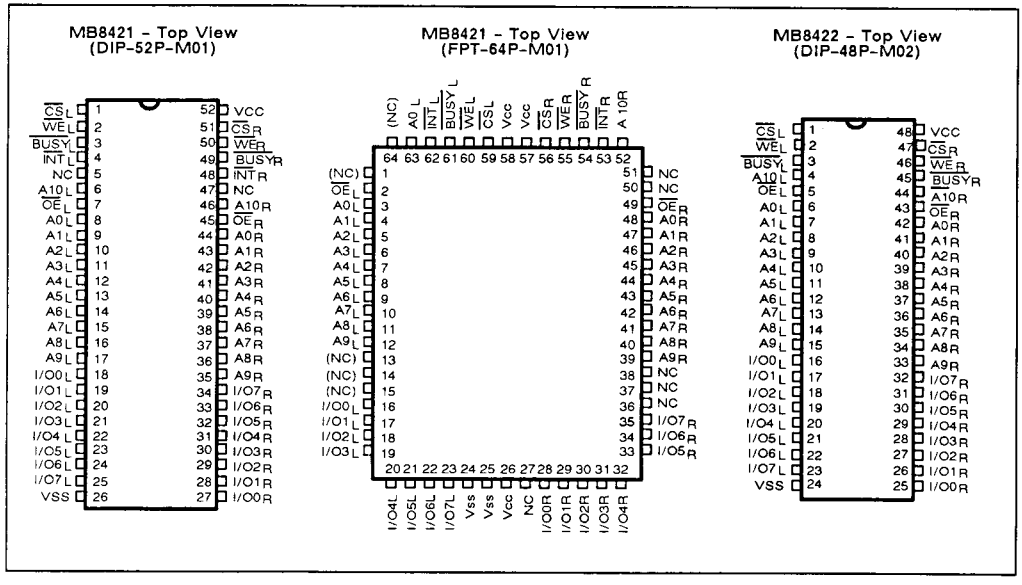


NOTES: MB8421 only.

I/O CAPACITANCE (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit
Input Capacitance (VIN = 0V)	CIN		10	pF
I/O Capacitance (VI/O = 0V)	CI/O		10	pF

PIN ASSIGNMENTS



PIN DESCRIPTIONS

Left Port	Right Port	Function	Left Port	Right Port	Function
$\overline{WE}_L$	$\overline{WE}_R$	Write Enable	$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{CS}_L$	$\overline{CS}_R$	Chip Select	$A0_L$ -- $A10_L$	$A0_R$-- $A10_R$	Address
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable	$I/O0_L$-- $I/O7_L$	$I/O0_R$-- $I/O7_R$	Data Input/Output
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag			
Vcc					Power (Common)
Vss					Ground (Common)

FUNCTIONAL OPERATION

The MB8421 and MB8422 provide two ports with separate control signals, address inputs, and input/output data pins that allow asynchronous read and write operations to any memory location. Each device has an on-chip automatic power-down feature controlled by $\overline{CS}$ that places the respective port in the standby mode when the chip is deselected ($\overline{CS}$ is HIGH).

When a port is enabled, access to the entire memory array is permitted. Each port has an independent Output Enable ($\overline{OE}$) control that is active in the read mode and enables the output drivers. Non-contention Read/Write conditions are shown in the following Truth Table; a simplified block diagram of the dual-port SRAM is shown in Fig. 1.

NON-CONTENTION READ/WRITE CONTROL

LEFT PORT INPUTS[1]			RIGHT PORT INPUTS[1]			FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	H	X	X	X	X	H	H	Left Port in Power Down Mode
X	X	X	X	H	X	H	H	Right Port in Power Down Mode
L	L	X	X	X	X	H	H	Data on Left Port Written Into Memory
H	L	L	X	X	X	H	H	Data in Memory Output on Left Port
X	X	X	L	L	X	H	H	Data on Right Port Written Into Memory
X	X	X	H	L	L	H	H	Data in Memory Output on Right Port

NOTES:
1. $A0_L$-$A10_L \neq A0_R$ - $A10_R$
2. H = HIGH, L = LOW, X = Don't Care

ARBITRATION LOGIC

The arbitration logic resolves an address match or chip-enable match and determines the access priority. In both cases, an active $\overline{BUSY}$ flag is set for the port-in-waiting. Since both ports are asynchronous, there is the possibility of accessing the same memory location from both sides. In the read mode, this condition is not a problem. However, this is a problem when both ports are in a write mode with different data words or when one port is reading and the other is writing. When both ports access the same memory location, the on-chip arbitration logic determines which port has access and the $\overline{BUSY}$ flag for the delayed port is set active LOW and all operations on that port are inhibited.The delayed port can be accessed when the $\overline{BUSY}$ flag becomes inactive. Basic modes of abitration are described in subsequent paragraphs.

1. When addresses for both the left and right ports match and are valid before $\overline{CS}$ is active, the on-chip control logic arbitrates between $\overline{CS}_L$ and $\overline{CS}_R$ for device access. Refer to the following Truth Table for signal states; timing detail is shown later in this data sheet under "Data Contention Cycle No. 2 ($\overline{CS}$ controlled)."
2. When $\overline{CS}_L$ and $\overline{CS}_R$ are LOW before an address match, on-chip control logic arbitrates between the left and right addresses for device access. Signal states for this condition are shown in the following Truth Table; timing detail is shown under "Data Contention Cycle No. 1 (Address Controlled)."

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ARBITRATION WITH ADDRESS MATCH BEFORE $\overline{CS}$

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	LBR	X	MATCH	X	L	X	MATCH	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	MATCH	X	LBL	X	MATCH	L	H	Right Operation Permitted Left Operation Not Permitted
X	LST	X	MATCH	X	LST	X	MATCH	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, LST= Low Same Time, LBR = Low Before Right, LBL = Low Before Left

ADDRESS ARBITRATION WITH $\overline{CS}$ LOW BEFORE ADDRESS MATCH

LEFT PORT				RIGHT PORT				FLAGS		FUNCTION
$R/\overline{W}_L$	$\overline{CS}_L$	$\overline{OE}_L$	$A0_L$-$A10_L$	$R/\overline{W}_R$	$\overline{CS}_R$	$\overline{OE}_R$	$A0_R$-$A10_R$	$\overline{BUSY}_L$	$\overline{BUSY}_R$	
X	L	X	VBR	X	L	X	VALID	H	L	Left Operation Permitted Right Operation Not Permitted
X	L	X	VALID	X	L	X	VBL	L	H	Right Operation Permitted Left Operation Not Permitted
X	L	X	VST	X	L	X	VST	H	L	Arbitration Resolved

NOTES: X = Don't Care, L = Low, H = High, VST = Valid Same Time, VBR = Valid Before Right, VBL = Valid Before Left

When both $\overline{CS}_L$ and $\overline{CS}_R$ are low at the same time ($\overline{CS}$ controlled) or when both left-and-right addresses are valid at the same time (address controlled), the $\overline{BUSY}_R$ flag for the right port is set to the active LOW state and access is granted to the left port.

For the Intel 8086 and Fujitsu's MBL8086 as well as most other microprocessors, the asynchronous $\overline{BUSY}$ signal can be directly tied to the READY input, providing setup-and-hold time requirements are met.

INTERRUPT FUNCTION

The interrupt ($\overline{INT}$) function provides communication between systems on both sides of the dual-port RAM. $\overline{INT}_L$ is set LOW when the processor on the right port writes to address 7FE (A0 = L and A1-A10 = H). When the left port acknowledges by reading address 7FE, $\overline{INT}_L$ is then reset to HIGH. In essence, address 7FE serves as an 8-bit mailbox that transfers information from the right port to the left port. When $\overline{INT}_R$ is set LOW, the processor on the left port writes to address 7FF (A0-A10=H). When the right port acknowledges by reading address 7FF, $\overline{INT}_R$ is then reset to HIGH. Hence, address 7FF serves as a second 8-bit mailbox, transferring information from the left port to the right port.

On power-up, $\overline{INT}_L$ and $\overline{INT}_R$ are set to a HIGH state. However, if one port is in the standby mode, the standby port can still be interrupted by the processor on the other port. But if the $\overline{BUSY}$ flag is set to the LOW state, the port associated with that flag cannot set or reset the $\overline{INT}$ flag.

RECOMMENDED OPERATING CONDITIONS

(Referenced to Vss)

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	Vcc	4.5	5.0	5.5	V
Operating Temperature	TA	0		70	°C

DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted.)

Parameter	Symbol	Condition	MB8421/ MB8422-90/12		MB8421/MB8422 -90L/-90LL/-12L/-12LL		Unit
			Min	Max	Min	Max	
Operating Supply Current (Both ports Active)	ICC	Cycle = Min Duty = 100% IOUT = 0 mA		120		90	mA
Standby Supply Current	ISB1	Both ports at Standby $\overline{CS}_L$ & $\overline{CS}_R$ = VIH		7		5	mA
	ISB2	One port at Standby $\overline{CS}_L$ or $\overline{CS}_R$ =VIH, IOUT = 0 mA		70		50	mA
	ISB3	Both ports at Full Standby $\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc -0.2V		2		0.2	mA
	ISB4	One port at Full Standby $\overline{CS}_L$ or $\overline{CS}_R \geq$ Vcc -0.2V IOUT = 0 mA		70		50	mA
Input Leakage Current	ILI	VIN = 0V to Vcc	-10	10	-10	10	µA
Output Leakage Current	ILO	$\overline{CS}$ = VIH, VOUT = 0V to Vcc	-10	10	-10	10	µA
Input High Voltage	VIH		2.2	Vcc +0.3	2.2	Vcc +0.3	V
Input Low Voltage	VIL		-0.3	0.8	-0.3	0.8	V
Output High Voltage	VOH (Note)	IOUT = -1.0 mA	2.4		2.4		V
Output Low Voltage	VOL	IOUT = 3.2 mA		0.4		0.4	V
Output Low Voltage for Open-Drain	VOL	IOUT = 8 mA		0.4		0.4	V

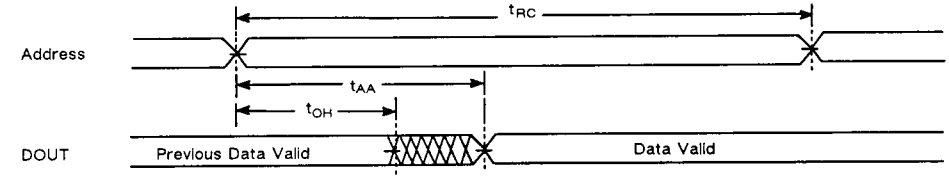
NOTE: The $\overline{BUSY}$ and $\overline{INT}$ pins require pull-up resistors because they are open-drain outputs.

AC CHARACTERISTICS

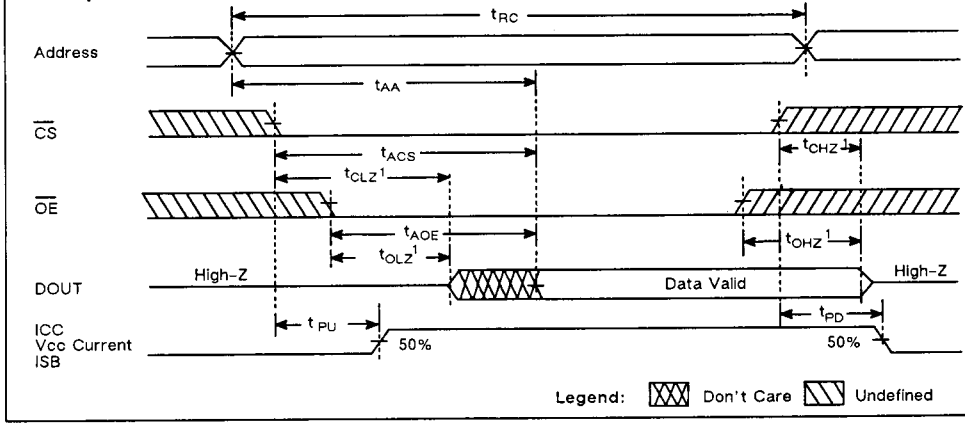
(Recommended Operations Conditions unless otherwise noted.)

Parameter	Symbol	MB8421-90/90L/90LL MB8422-90/90L/90LL		MB8421-12/12L/12LL MB8422-12/12L/12LL		Unit
		Min	Max	Min	Max	
Read Cycle Parameters & Timing Diagrams						
Read Cycle Time	t_{RC}	90		120		ns
Address Access Time	t_{AA}		90		120	ns
Chip Select Access Time	t_{ACS}		90		120	ns
Output Enable Access Time	t_{AOE}		40		50	ns
Output Hold from Address Change	t_{OH}	10		10		ns
Chip Select to Output Low-Z (Note 1)	t_{CLZ}	5		5		ns
Output Enable to Output Low-Z (Note 1)	t_{OLZ}	5		5		ns
Chip Select to Output High-Z (Note 1)	t_{CHZ}		40		50	ns
Output Enable to Output High-Z (Note 1)	t_{OHZ}		40		50	ns
Power up from Chip Select	t_{PU}	0		0		ns
Power down from Chip Select	t_{PD}		50		60	ns

Read Cycle No. 1 [2, 3]:



Read Cycle No. 2 [2]:



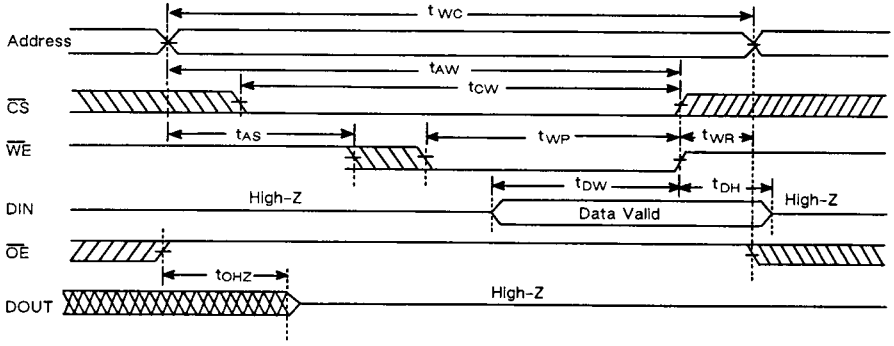
NOTES:

1. Transition is measured at a point of ± 500 mV from steady-state voltage with an output capacitance of 5pF.
2. $\overline{WE}$ is High during read cycle.
3. Device is continuously selected ($\overline{CS}$ = $\overline{OE}$ = VIL).

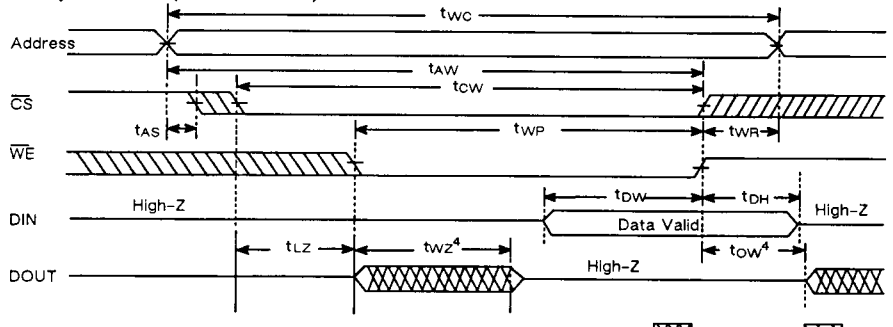
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L/90LL MB8422-90/90L/90LL		MB8421-12/12L/12LL MB8422-12/12L/12LL		Unit
		Min	Max	Min	Max	
Write Cycle Parameters & Timing Diagrams						
Write Cycle Time	t_{WC}	90		120		ns
Address Valid to End of Write	t_{AW}	85		100		ns
Chip Select to End of Write	t_{CW}	85		100		ns
Address Setup Time	t_{AS}	0		0		ns
Write Pulse Width	t_{WP}	60		70		ns
Write Recovery Time	t_{WR}	0		0		ns
Data Valid to End of Write	t_{DW}	40		40		ns
Data Hold Time	t_{DH}	0		0		ns
Write Enable to Output Low-Z (Note 4)	t_{OW}	0		0		ns
Write Enable to Output High-Z (Note 4)	t_{WZ}		40		50	ns

Write Cycle No. 1 ($\overline{WE}$ Controlled) [1,2]



Write Cycle No. 2 ($\overline{CS}$ Controlled) [1,2,3]



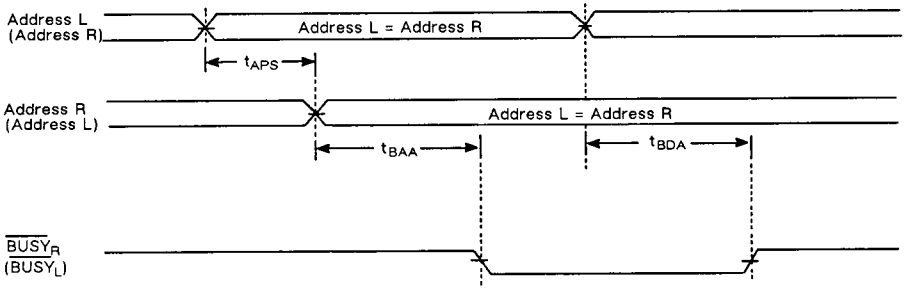
Legend: Don't Care, Undefined

NOTES:
1. The Write Enable ($\overline{WE}$) signal must be high during an address transition.
2. If the Output Enable ($\overline{OE}$) and Chip Select ($\overline{CS}$) signals are in the Read Mode, the associated I/O pins are in the output state; accordingly, input signals of opposite phase must not be applied to the outputs.
3. If $\overline{CS}$ goes high prior to or coincident with the low-to-high transition of $\overline{WE}$, the output remains in high-impedance state.
4. This parameter is specified at a point ± 500 mV from steady-state voltage with an output capacitance of 5 pF.

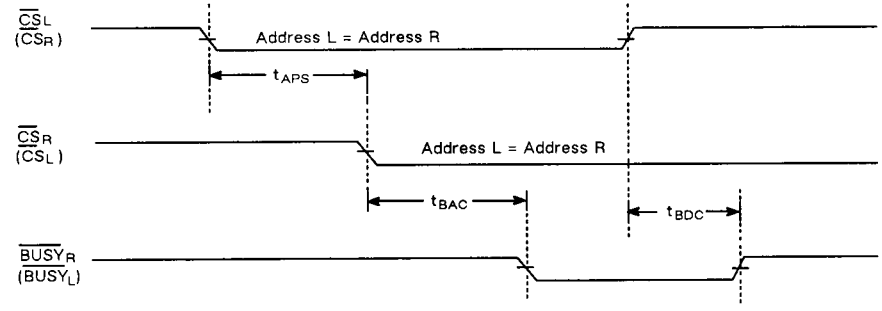
AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
$\overline{BUSY}$ Parameters & Data Contention Timing						
$\overline{BUSY}$ Access Time from Address	t_{BAA}		45		60	ns
$\overline{BUSY}$ Output High-Z from Address	t_{BDA}		45		60	ns
$\overline{BUSY}$ Access Time from $\overline{CS}$	t_{BAC}		45		60	ns
$\overline{BUSY}$ Output High-Z from $\overline{CS}$	t_{BDC}		45		60	ns
Arbitration Priority Set up Time	t_{APS}	20		25		ns

Data Contention Cycle No. 1 (Address Controlled)[1, 2]:



Data Contention Cycle No. 2 ($\overline{CS}$ Controlled)[1, 3]:



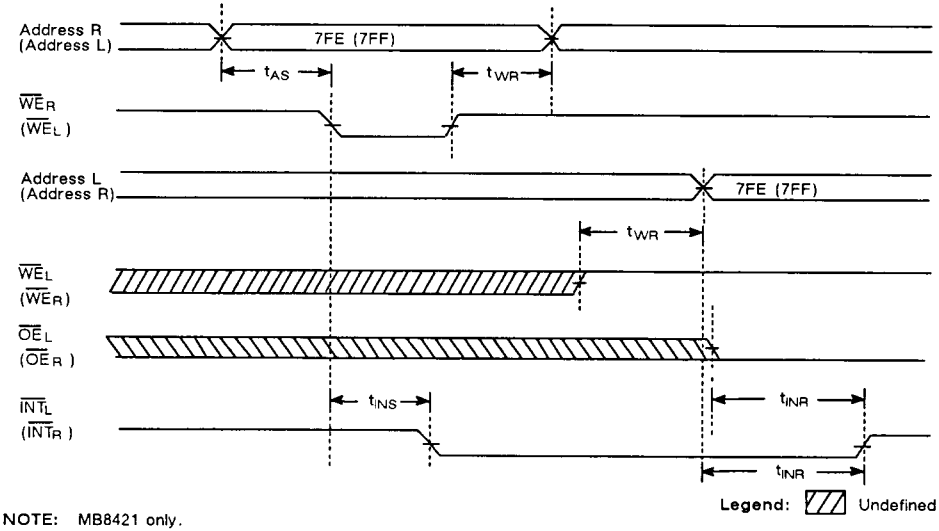
NOTES:

1. In case of dual-access at the same memory location, the port that accesses the RAM first sets the $\overline{BUSY}$ flag HIGH.
2. Chip Select ($\overline{CS}$) signal must be low before or coincident with an address transition.
3. Address is valid prior to or coincidence with the high-to-low transition of $\overline{CS}$.

AC CHARACTERISTICS (Continued)

Parameter	Symbol	MB8421-90/90L MB8422-90/90L		MB8421-12/12L MB8422-12/12L		Unit
		Min	Max	Min	Max	
Interrupt Parameters & Timing Diagram						
$\overline{INT}$ Set Time (Note)	t_{INS}		80		100	ns
$\overline{INT}$ Reset Time (Note)	t_{INR}		80		100	ns

Interrupt Cycle Timing

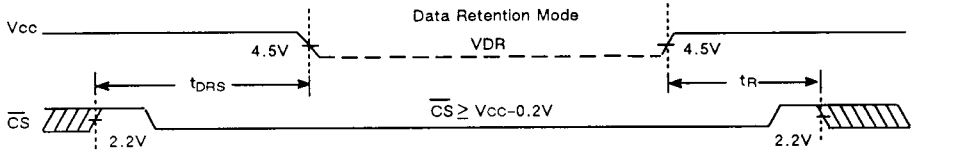


NOTE: MB8421 only.

AC CHARACTERISTICS (Continued)

DATA RETENTION PARAMETERS & TIMING

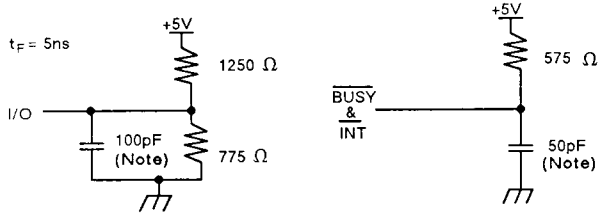
Parameter	Symbol	MB8421-90/12 MB8422-90/12		MB8421-90L/12L MB8422-90L/12L		Unit
		Min	Max	Min	Max	
Data Retention Parameters & Timing						
Data Retention Supply Voltage	VDR	2.0	5.5	2.0	5.5	V
Data Retention Supply Current (Note)	IDR		0.2		0.02	mA
Data Retention Setup Time	t_{DRS}	0		0		ns
Operation Recovery Time	t_R	t_{RC}		t_{RC}		ns



NOTE: Vcc = VDR = 3V
$\overline{CS}_L$ & $\overline{CS}_R \geq$ Vcc - 0.2

AC TEST CONDITIONS

Input Pulse Levels: 0 to 3.0V
Input Pulse Rise & Fall Times: t_R, t_F = 5ns
Timing Reference Levels: 1.5V
Output Loads:



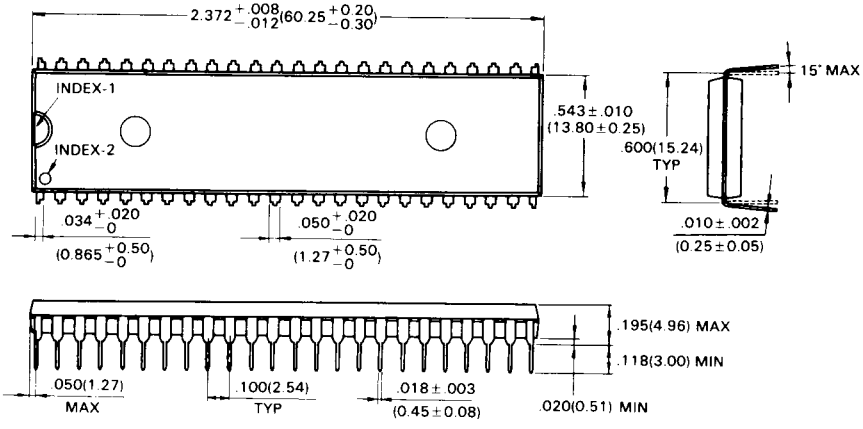
NOTE: Includes jig and stray capacitance.

PACKAGE DIMENSIONS

(Suffix: P)

48-LEAD PLASTIC DUAL IN-LINE PACKAGE

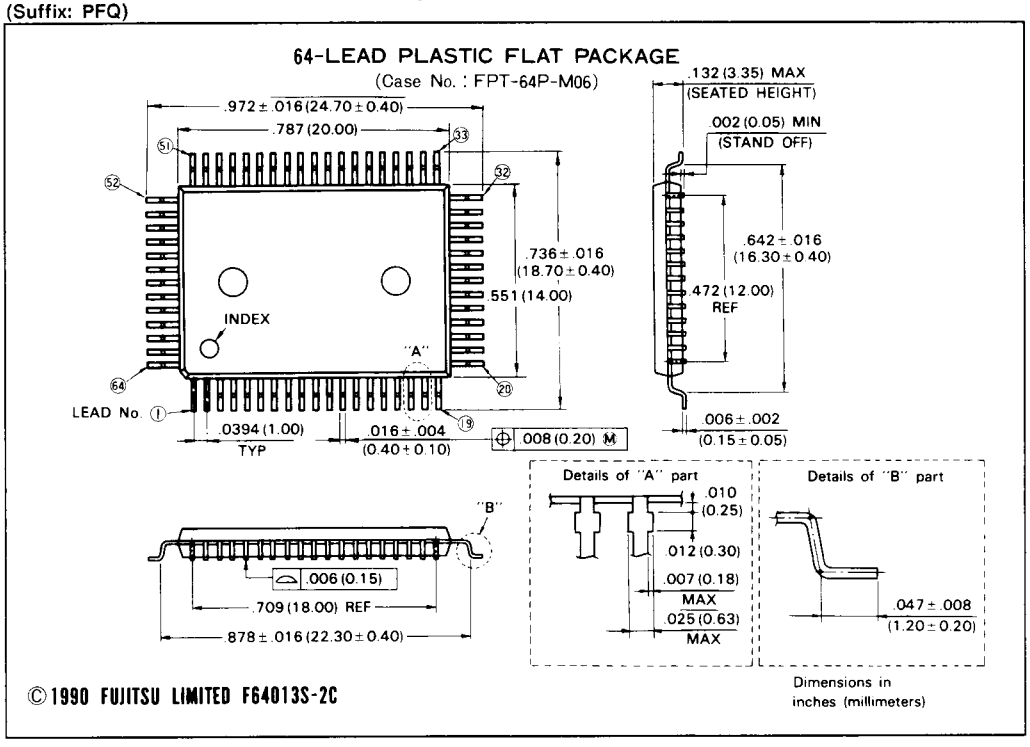
(Case No. : DIP-48P-M02)



Dimensions in
inches (millimeters)

PACKAGE DIMENSIONS (Continued)

(Suffix: PFQ)



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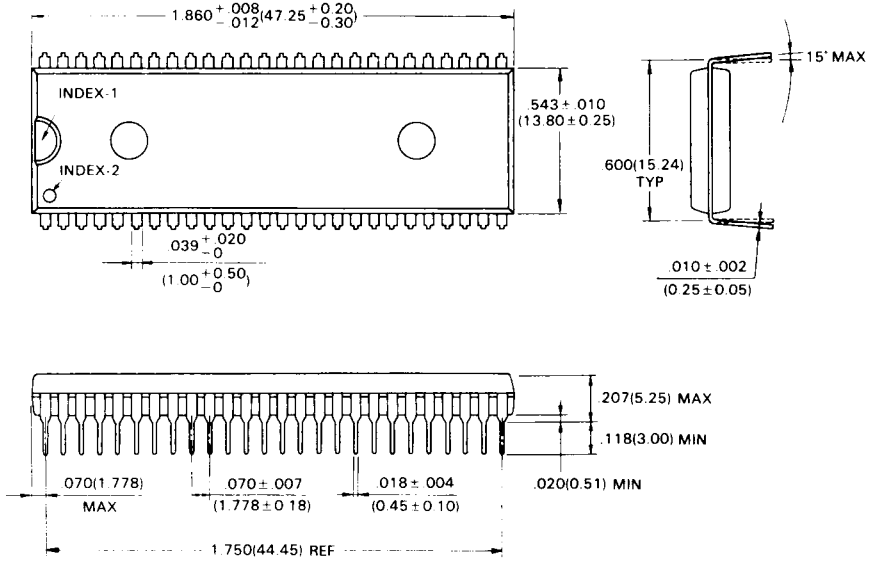
PACKAGE DIMENSIONS (Continued)

(Suffix: P)

52-LEAD PLASTIC DUAL IN-LINE PACKAGE

(Case No. : DIP-52P-M01)



Dimensions in
inches (millimeters)

4