Preliminary TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

T6K41

Column and Row Driver LSI for a Dot Matrix Graphic LCD

The T6K41 is a driver for a small-to-medium-sized dot matrix graphic LCD, especially for four-gray-scale monochromatic STN LCDs. This driver can be interfaced to the MPU via an 8-bit (80/68-series) or a serial interface, and is operated asynchronously with the MPU.

Since the T6K41 contains a CR oscillator, it can generate the timing signals required for the LCD.

The T6K41 has 128 outputs for the LCD drive (segment) signals that constitute the display data, 128 outputs for the LCD drive (common) signals that constitute the scanning signals and 16 bits of static-LCD drive (icon) signals. Furthermore, the T6K41 has 128 × 128 × 2 bits display RAM and 16-bit register. Thus, this single device allows you to drive an LCD panel comprised of up to 128 × 128 + 16 dots with a minimize of power requirement. It also incorporates a gray-scale function.

The display RAM of the T6K41 is a two-port RAM so that the MPU access it without any wait time.

To minimize power consumption, the T6K41 has a display change mode (power save mode) in which only a 16-dot icon can be displayed. Furthermore, it has various built-in analog circuits such as a voltage regulator, voltage divider resistors, power supply op-amp, DC-DC converters (×2 to ×6) and a contrast control (electronic volume) circuit. All these circuits enable the LCD panel to be driven with a single power supply.

Unit: mm

T6K41	Lead Pitch	
	IN	OUT

Please contact your nearest TOSHIBA dealer for individual package dimensions.

No idea

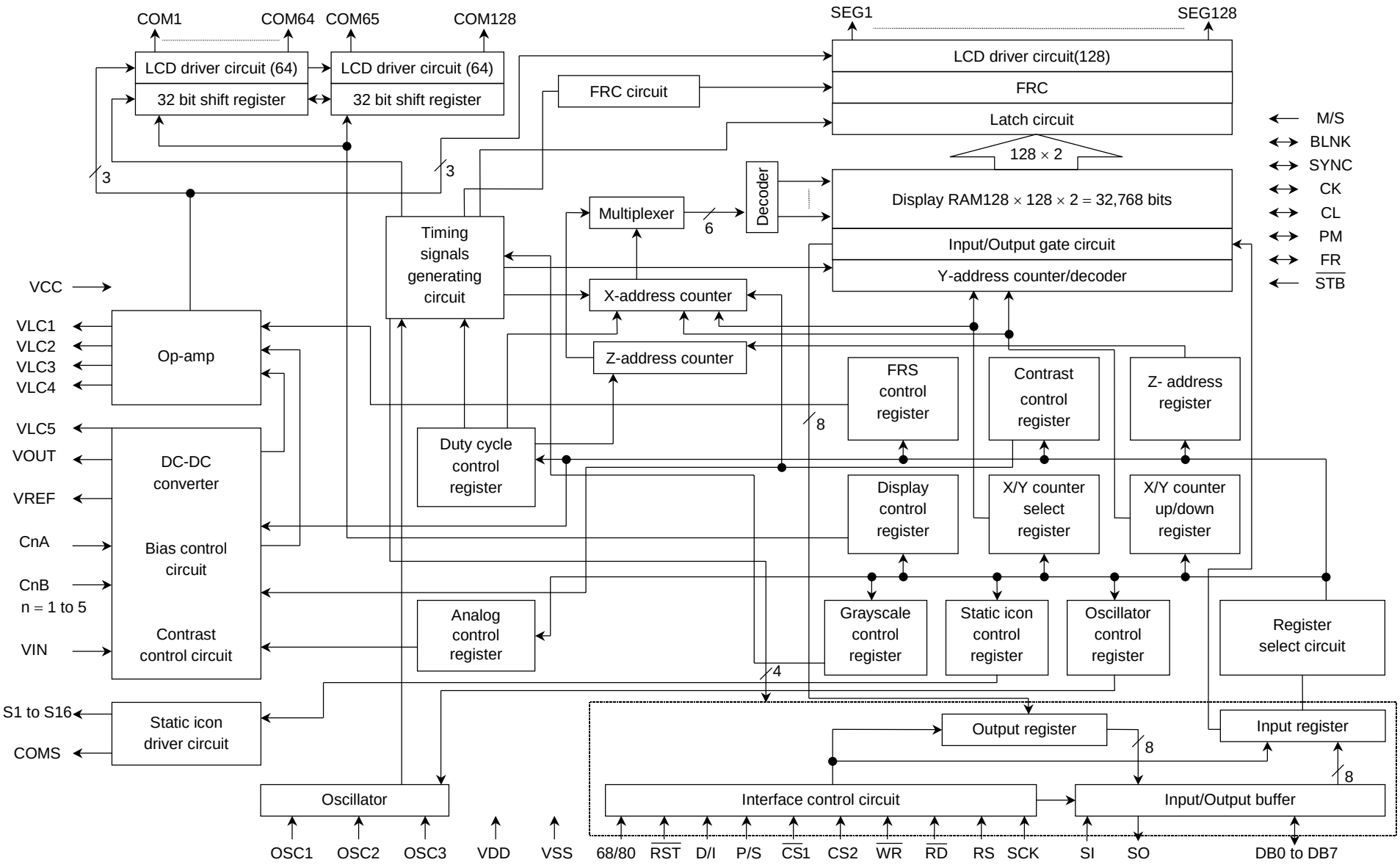
TCP (Tape Carrier Package)

Features

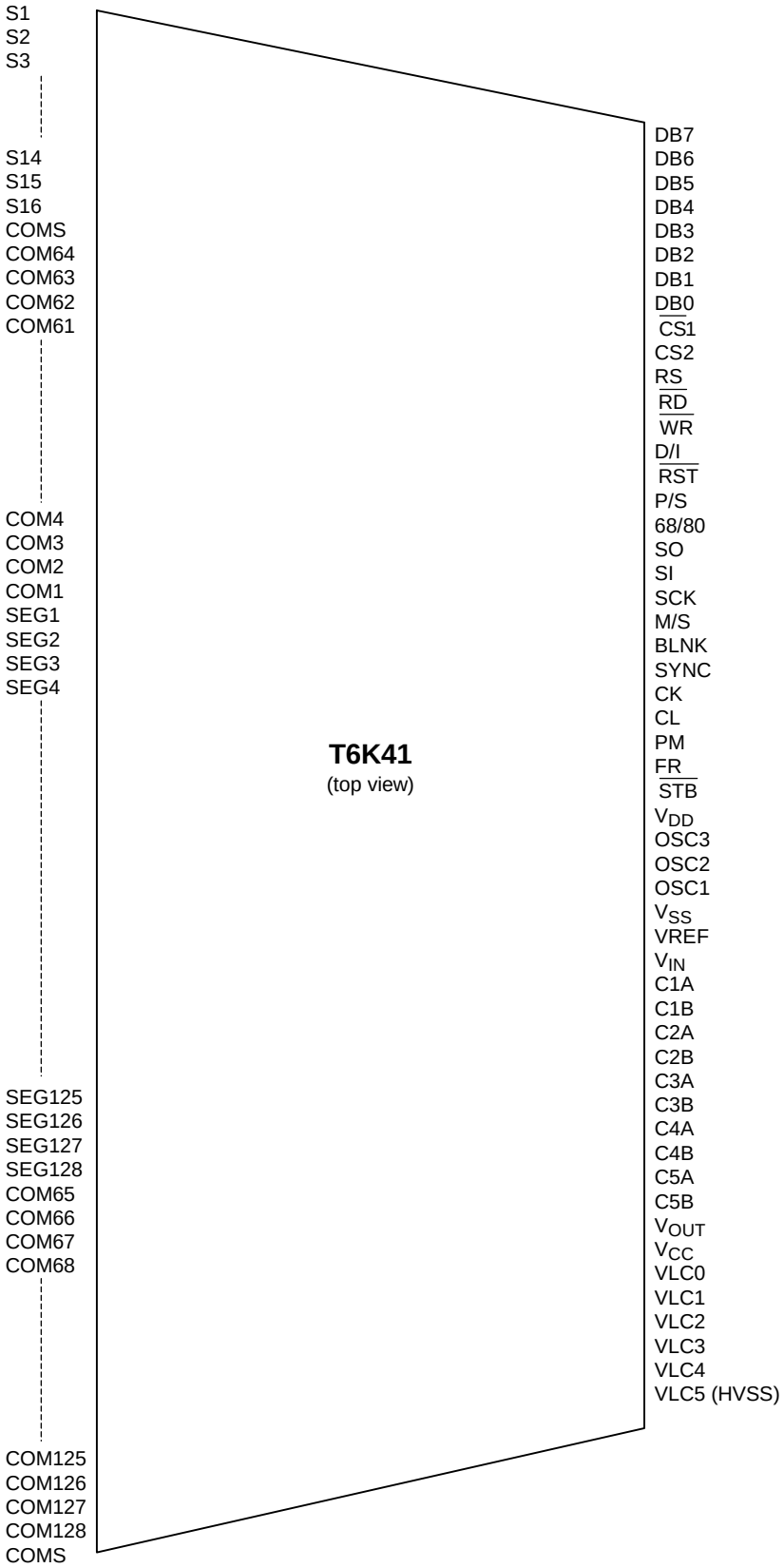
- LCD drive outputs : 128 rows (common) × 128 columns (segment) + 16 icons
- Display RAM : 128 × 128 × 2 = 32,768 bits, 2-port RAM
- Gray scales : 4 gray-scale levels (palette function)
- Word length : 8-bit/word
- Display duty cycle : 1/72, 1/80, 1/100 or 1/128 duty during Normal Mode.
  (Duty cycles in Normal Mode are set in software by the MPU.)
- Display modes : Normal Mode: Full display
  Power Save Mode: Icon display
  Partial Display Mode: Partial display
  Standby Mode: Clock stopped (all internal circuits turned off)
- MPU : 8-bit (68/80 Series) parallel or serial interface
- Oscillator : Built-in CR oscillator with external resistors
- Power supply circuits : Resistors to divide bias voltage, op-amp for LCD drive power supply, DC-DC converters (×2 to ×6), contrast control circuit.
- Operating voltage : V_{DD} = 2.4 V to 3.3 V, V_{IN} = 2.7 V to 3.3 V
- LCD drive voltage : V_{CC} = 16.5 V (max)
  V_{OUT} = 15.4 V (typ.) or V_{OUT} = 13.0 V (typ.) (for internal voltage regulator)
  These voltages can be selected in software.
- CMOS process
- Low power consumption : I_{SS} = 300 μA (typ.)
  Conditions: V_{DD} = V_{IN} = 3.0 V, when DC-DC converter is used (×6 Mode), LCD non-loaded, Ta = 25°C, 1/128 duty, 1/12 bias, fosc = 82 kHz (when internal oscillator is used), voltage regulator ON, op-amp ON, display data = ALL 4-gray-scale checker pattern, no data access from MPU.
- Temperature coefficient of voltage regulator: −0.05%/°C
- Package :

Product	Package
T6K41 (×××, ×××)	TCP (Tape carrier package)
JBT6K41-AS	Gold bump chip

Block Diagram



Pin Assignment



Note 1: The above diagram shows the pin configuration of the LSI chip, not that of the tape carrier package.

Pad Specification

Note 2: Please refer to the T6K41 technical datasheet for pad specification.

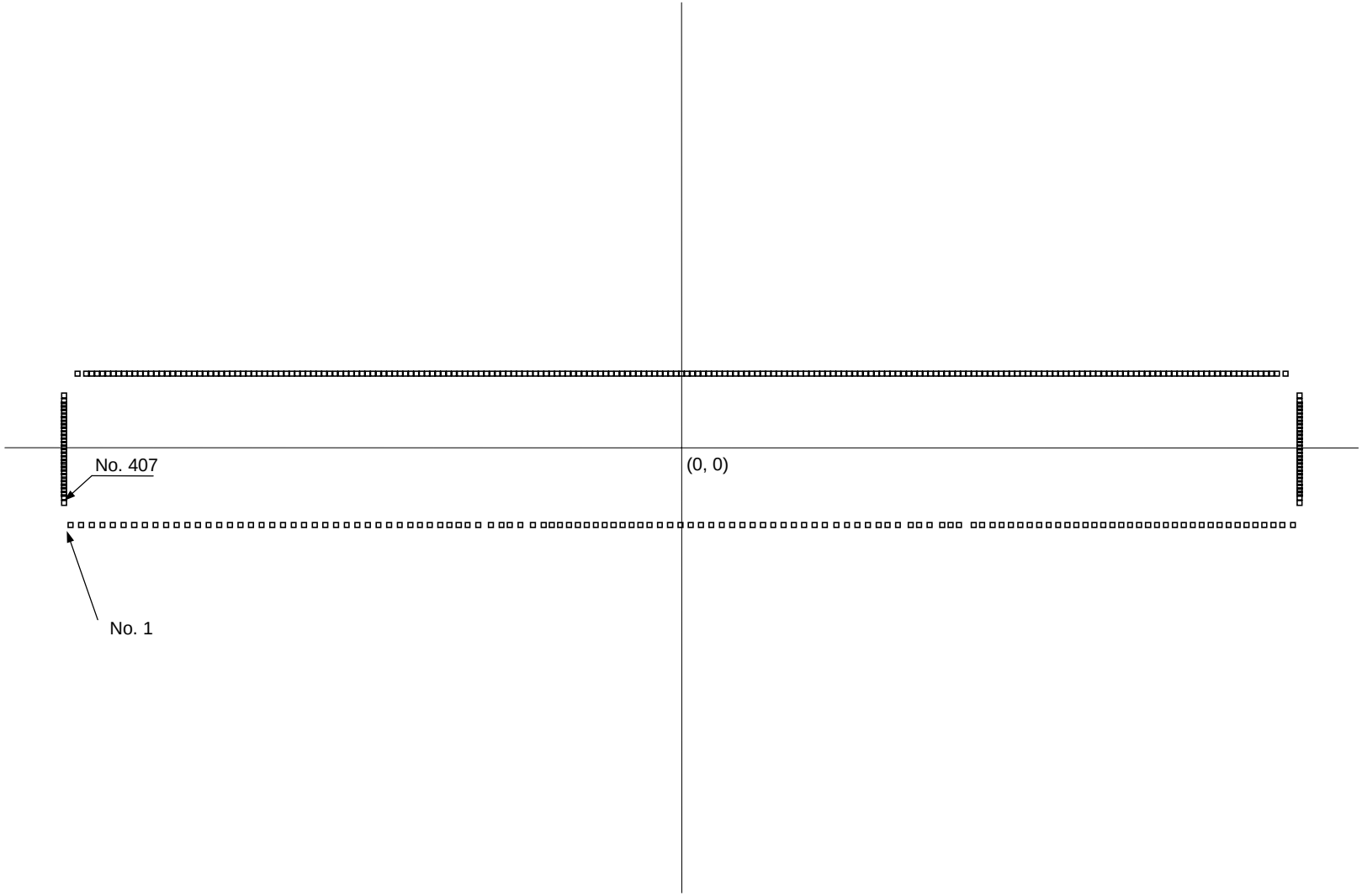
Item		Size	Unit
Chip Size		12300 × 2610	μm
Chip Tip Coordinates	(1)	−6150, −1305	μm
	(2)	−6150, −1305	
	(3)	6150, 1305	
	(4)	6150, −1305	
Bump Pitch		52	μm
Bump Height		14±4	μm

Item	Number of Pins	
Input pin	105 Pins (including Dummy pins)	
Output pin	283 Pins (including Dummy pins)	
TEST Pin	2 Pins	(Note 3)
FUSE Pin	17 Pins	(Note 3)

Note 3: TEST and FUSE pins are LSI test pins, leave these pins open.

Pad Layout

Chip size: 12.3 × 2.61 mm



Note 4: Please refer to the T6K41 technical datasheet for pad layout and coordinates values.

Pad Coordinates (1)

[Unit: μm]

No.	NAME	X-Point	Y-Point
1	VCL5	−5871	−1124
2	VLC5	−5769	−1124
3	VLC5	−5667	−1124
4	VLC5	−5565	−1124
5	VLC4	−5463	−1124
6	VLC4	−5361	−1124
7	VLC3	−5259	−1124
8	VLC3	−5157	−1124
9	VLC2	−5055	−1124
10	VLC2	−4953	−1124
11	VLC1	−4851	−1124
12	VLC1	−4749	−1124
13	VLC0	−4647	−1124
14	VLC0	−4545	−1124
15	VLC0	−4443	−1124
16	VLC0	−4341	−1124
17	VCC1	−4239	−1124
18	VCC1	−4137	−1124
19	VCC1	−4035	−1124
20	VCC1	−3933	−1124
21	TEST2	−3831	−1124
22	VOUT	−3729	−1124
23	VOUT	−3627	−1124
24	C5B	−3525	−1124
25	C5A	−3423	−1124
26	C4B	−3321	−1124
27	C4A	−3219	−1124
28	C3B	−3117	−1124
29	C3A	−3015	−1124
30	C2B	−2913	−1124
31	C2A	−2811	−1124
32	C1B	−2709	−1124
33	C1A	−2607	−1124
34	DMYVSS	−2514	−1124
35	VIN	−2421	−1124
36	VIN	−2319	−1124
37	DMYVSS	−2231	−1124
38	VREG	−2142	−1124
39	TDUMMY1	−2056	−1124
40	TDUMMY2	−1955	−1124
41	TDUMMY3	−1833	−1124
42	TDUMMY4	−1732	−1124
43	TDUMMY5	−1652	−1124
44	TDUMMY6	−1551	−1124
45	TDUMMY7	−1429	−1124
46	TDUMMY8	−1328	−1124
47	DMYVSS	−1249	−1124
48	V_{SS}	−1170	−1124
49	V_{SS}	−1084	−1124
50	V_{SS}	−998	−1124
51	V_{SS}	−912	−1124
52	V_{SS}	−826	−1124
53	TEST3	−740	−1124
54	OSC1	−654	−1124
55	DMYVSS	−568	−1124
56	OSC2	−482	−1124
57	DMYVSS	−396	−1124
58	OSC3	−310	−1124
59	FUSE31	−210	−1124
60	FUSE32	−111	−1124
61	FUSE3G	−12	−1124
62	FUSE33	87	−1124
63	FUSE34	186	−1124
64	FUSE21	285	−1124
65	FUSE22	384	−1124
66	FUSE23	483	−1124
67	FUSE2G	582	−1124
68	FUSE24	681	−1124
69	FUSE25	780	−1124
70	FUSE11	879	−1124
71	FUSE12	978	−1124
72	FUSE13	1077	−1124
73	FUSE1G	1176	−1124
74	FUSE14	1275	−1124
75	FUSE15	1374	−1124
76	V_{DD}	1486	−1124
77	V_{DD}	1587	−1124
78	V_{DD}	1688	−1124
79	V_{DD}	1789	−1124
80	V_{DD}	1890	−1124
81	TDUMMY9	1976	−1124
82	TDUMMY10	2077	−1124
83	TDUMMY11	2199	−1124
84	TDUMMY12	2279	−1124
85	TDUMMY13	2380	−1124
86	TDUMMY14	2502	−1124
87	TDUMMY15	2582	−1124
88	TDUMMY16	2662	−1124
89	TDUMMY17	2805	−1124
90	TDUMMY18	2885	−1124
91	TDUMMY19	2986	−1124
92	/STB	3072	−1124
93	FR	3161	−1124
94	PM	3252	−1124
95	CL	3343	−1124
96	CK	3434	−1124
97	SYNC	3525	−1124
98	BLNK	3616	−1124
99	M/S	3705	−1124
100	SCK	3791	−1124
101	SI	3877	−1124
102	SO	3963	−1124
103	DMYVDD	4049	−1124
104	68/80	4135	−1124
105	DMYVSS	4221	−1124
106	P/S	4307	−1124
107	DMYVDD	4393	−1124
108	/RST	4479	−1124
109	D/I	4565	−1124
110	/WR	4651	−1124
111	/RD	4737	−1124
112	RS	4823	−1124
113	CS2	4909	−1124
114	/CS1	4995	−1124
115	DMYVSS	5081	−1124
116	DB0	5167	−1124
117	DB1	5253	−1124
118	DB2	5339	−1124
119	DB3	5425	−1124
120	DB4	5511	−1124
121	DB5	5597	−1124
122	DB6	5683	−1124
123	DB7	5769	−1124
124	DMYVDD	5871	−1124
125	DUMMY1	5934	−803
126	DUMMY2	5934	−721
127	DUMMY3	5934	−669
128	DUMMY4	5934	−617
129	DUMMY5	5934	−565
130	DUMMY6	5934	−513
131	S1	5934	−461
132	S2	5934	−409
133	S3	5934	−357
134	S4	5934	−305
135	S5	5934	−253

Pad Coordinates (2)

[Unit: μm]

No.	NAME	X-Point	Y-Point
136	S6	5934	−201
137	S7	5934	−149
138	S8	5934	−97
139	S9	5934	−45
140	S10	5934	8
141	S11	5934	60
142	S12	5934	112
143	S13	5934	164
144	S14	5934	216
145	S15	5934	268
146	S16	5934	320
147	COMS2	5934	372
148	DUMMY7	5934	425
149	DUMMY8	5934	477
150	COM64	5934	529
151	COM63	5934	581
152	COM62	5934	633
153	COM61	5934	685
154	COM60	5934	767
155	COM59	5801	1087
156	COM58	5719	1087
157	COM57	5667	1087
158	COM56	5615	1087
159	COM55	5563	1087
160	COM54	5511	1087
161	COM53	5459	1087
162	COM52	5407	1087
163	COM51	5355	1087
164	COM50	5303	1087
165	COM49	5251	1087
166	COM48	5199	1087
167	COM47	5147	1087
168	COM46	5095	1087
169	COM45	5043	1087
170	COM44	4991	1087
171	COM43	4939	1087
172	COM42	4887	1087
173	COM41	4835	1087
174	COM40	4783	1087
175	COM39	4731	1087
176	COM38	4679	1087
177	COM37	4627	1087
178	COM36	4575	1087
179	COM35	4523	1087
180	COM34	4471	1087

No.	NAME	X-Point	Y-Point
181	COM33	4419	1087
182	COM32	4367	1087
183	COM31	4315	1087
184	COM30	4263	1087
185	COM29	4211	1087
186	COM28	4159	1087
187	COM27	4107	1087
188	COM26	4055	1087
189	COM25	4003	1087
190	COM24	3951	1087
191	COM23	3899	1087
192	COM22	3847	1087
193	COM21	3795	1087
194	COM20	3743	1087
195	COM19	3691	1087
196	COM18	3639	1087
197	COM17	3587	1087
198	COM16	3535	1087
199	COM15	3483	1087
200	COM14	3431	1087
201	COM13	3379	1087
202	COM12	3327	1087
203	COM11	3275	1087
204	COM10	3223	1087
205	COM9	3171	1087
206	COM8	3119	1087
207	COM7	3067	1087
208	COM6	3015	1087
209	COM5	2963	1087
210	COM4	2911	1087
211	COM3	2859	1087
212	COM2	2807	1087
213	COM1	2755	1087
214	SEG1	2703	1087
215	SEG2	2651	1087
216	SEG3	2599	1087
217	SEG4	2547	1087
218	SEG5	2495	1087
219	SEG6	2443	1087
220	SEG7	2391	1087
221	SEG8	2339	1087
222	SEG9	2287	1087
223	SEG10	2235	1087
224	SEG11	2183	1087
225	SEG12	2131	1087

No.	NAME	X-Point	Y-Point
226	SEG13	2079	1087
227	SEG14	2027	1087
228	SEG15	1975	1087
229	SEG16	1923	1087
230	SEG17	1871	1087
231	SEG18	1819	1087
232	SEG19	1767	1087
233	SEG20	1715	1087
234	SEG21	1663	1087
235	SEG22	1611	1087
236	SEG23	1559	1087
237	SEG24	1507	1087
238	SEG25	1455	1087
239	SEG26	1403	1087
240	SEG27	1351	1087
241	SEG28	1299	1087
242	SEG29	1247	1087
243	SEG30	1195	1087
244	SEG31	1143	1087
245	SEG32	1091	1087
246	SEG33	1039	1087
247	SEG34	987	1087
248	SEG35	935	1087
249	SEG36	883	1087
250	SEG37	831	1087
251	SEG38	779	1087
252	SEG39	727	1087
253	SEG40	675	1087
254	SEG41	623	1087
255	SEG42	571	1087
256	SEG43	519	1087
257	SEG44	467	1087
258	SEG45	415	1087
259	SEG46	363	1087
260	SEG47	311	1087
261	SEG48	259	1087
262	SEG49	207	1087
263	SEG50	155	1087
264	SEG51	103	1087
265	SEG52	51	1087
266	SEG53	−1	1087
267	SEG54	−53	1087
268	SEG55	−105	1087
269	SEG56	−157	1087
270	SEG57	−209	1087

Pad Coordinates (3)

[Unit: μm]

No.	NAME	X-Point	Y-Point
271	SEG58	−261	1087
272	SEG59	−313	1087
273	SEG60	−365	1087
274	SEG61	−417	1087
275	SEG62	−469	1087
276	SEG63	−521	1087
277	SEG64	−573	1087
278	SEG65	−625	1087
279	SEG66	−677	1087
280	SEG67	−729	1087
281	SEG68	−781	1087
282	SEG69	−833	1087
283	SEG70	−885	1087
284	SEG71	−937	1087
285	SEG72	−989	1087
286	SEG73	−1041	1087
287	SEG74	−1093	1087
288	SEG75	−1145	1087
289	SEG76	−1197	1087
290	SEG77	−1249	1087
291	SEG78	−1301	1087
292	SEG79	−1353	1087
293	SEG80	−1405	1087
294	SEG81	−1457	1087
295	SEG82	−1509	1087
296	SEG83	−1561	1087
297	SEG84	−1613	1087
298	SEG85	−1665	1087
299	SEG86	−1717	1087
300	SEG87	−1769	1087
301	SEG88	−1821	1087
302	SEG89	−1873	1087
303	SEG90	−1925	1087
304	SEG91	−1977	1087
305	SEG92	−2029	1087
306	SEG93	−2081	1087
307	SEG94	−2133	1087
308	SEG95	−2185	1087
309	SEG96	−2237	1087
310	SEG97	−2289	1087
311	SEG98	−2341	1087
312	SEG99	−2393	1087
313	SEG100	−2445	1087
314	SEG101	−2497	1087
315	SEG102	−2549	1087
316	SEG103	−2601	1087
317	SEG104	−2653	1087
318	SEG105	−2705	1087
319	SEG106	−2757	1087
320	SEG107	−2809	1087
321	SEG108	−2861	1087
322	SEG109	−2913	1087
323	SEG110	−2965	1087
324	SEG111	−3017	1087
325	SEG112	−3069	1087
326	SEG113	−3121	1087
327	SEG114	−3173	1087
328	SEG115	−3225	1087
329	SEG116	−3277	1087
330	SEG117	−3329	1087
331	SEG118	−3381	1087
332	SEG119	−3433	1087
333	SEG120	−3485	1087
334	SEG121	−3537	1087
335	SEG122	−3589	1087
336	SEG123	−3641	1087
337	SEG124	−3693	1087
338	SEG125	−3745	1087
339	SEG126	−3797	1087
340	SEG127	−3849	1087
341	SEG128	−3901	1087
342	COM65	−3953	1087
343	COM66	−4005	1087
344	COM67	−4057	1087
345	COM68	−4109	1087
346	COM69	−4161	1087
347	COM70	−4213	1087
348	COM71	−4265	1087
349	COM72	−4317	1087
350	COM73	−4369	1087
351	COM74	−4421	1087
352	COM75	−4473	1087
353	COM76	−4525	1087
354	COM77	−4577	1087
355	COM78	−4629	1087
356	COM79	−4681	1087
357	COM80	−4733	1087
358	COM81	−4785	1087
359	COM82	−4837	1087
360	COM83	−4889	1087
361	COM84	−4941	1087
362	COM85	−4993	1087
363	COM86	−5045	1087
364	COM87	−5097	1087
365	COM88	−5149	1087
366	COM89	−5201	1087
367	COM90	−5253	1087
368	COM91	−5305	1087
369	COM92	−5357	1087
370	COM93	−5409	1087
371	COM94	−5461	1087
372	COM95	−5513	1087
373	COM96	−5565	1087
374	COM97	−5617	1087
375	COM98	−5669	1087
376	COM99	−5721	1087
377	COM100	−5803	1087
378	COM101	−5934	767
379	COM102	−5934	685
380	COM103	−5934	633
381	COM104	−5934	581
382	COM105	−5934	529
383	COM106	−5934	477
384	COM107	−5934	425
385	COM108	−5934	373
386	COM109	−5934	321
387	COM110	−5934	269
388	COM111	−5934	217
389	COM112	−5934	165
390	COM113	−5934	113
391	COM114	−5934	61
392	COM115	−5934	9
393	COM116	−5934	−43
394	COM117	−5934	−95
395	COM118	−5934	−147
396	COM119	−5934	−199
397	COM120	−5934	−251
398	COM121	−5934	−303
399	COM122	−5934	−355
400	COM123	−5934	−407
401	COM124	−5934	−459
402	COM125	−5934	−511
403	COM126	−5934	−563
404	COM127	−5934	−615
405	COM128	−5934	−667
406	DUMMY9	−5934	−719
407	COMS1	−5934	−801

Pin Functions

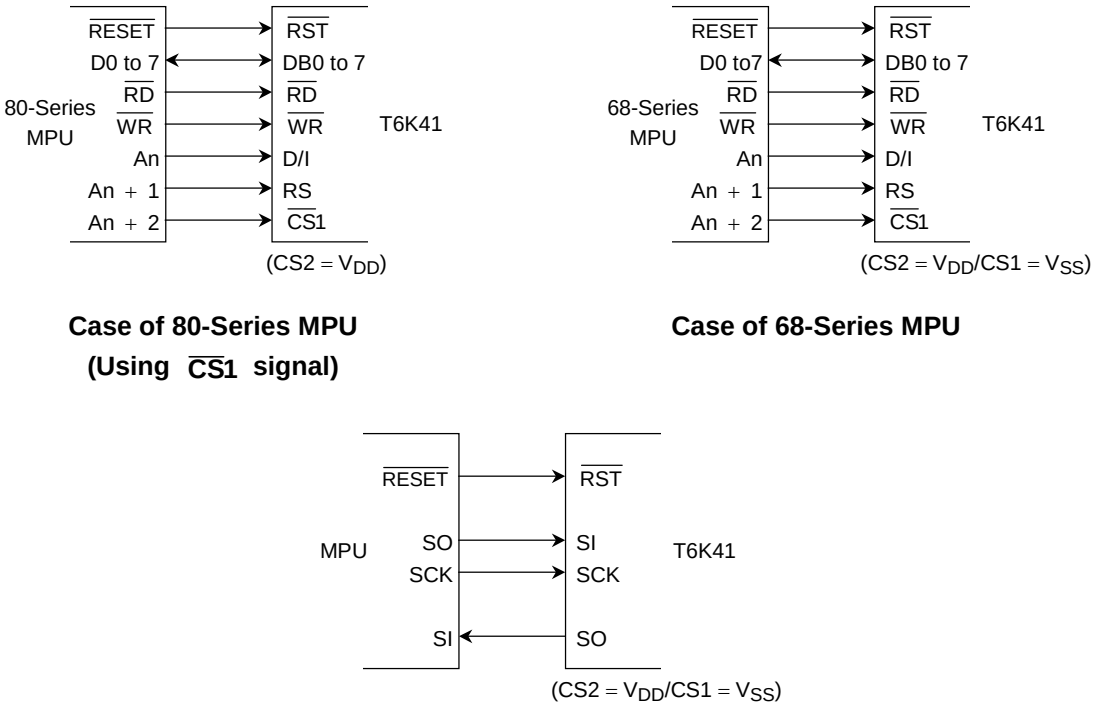
Pin Name	I/O	Functions
SEG1 to SEG128	Output	LCD drive segment signals
COM1 to COM128	Output	LCD drive common signals
S1 to S16	Output	LCD driver segment signals for static icons
COMS	Output	LCD driver common signals for static icons
DB0 to DB7	I/O	Data bus
$\overline{CS1}$	Input	Chip Select Signal 1 Write data: Data on DB0 to DB7 is latched on the rising edge of $\overline{CS1}$. Read data: Data appears on DB0 to DB7 while $\overline{CS1}$ is Low.
CS2	Input	Chip Select Signal 2 Write data: Data on DB0 to DB7 is latched on the falling edge of CS2. Read data: Data appears on DB0 to DB7 while $\overline{CS1}$ is High.
D/I	Input	Input for data/instruction select signal • D/I = High → Indicates that the data on DB0 to DB7 or SI is display data. • D/I = Low → Indicates that the data on DB0 to DB7 or SI is an instruction.
$\overline{WR}$ (R/W)	Input	Input or Write Select signal (Input for Read/Write Select signal) • If 80 Series MPU is selected, data on DB0 to DB7 is latched on the rising edge of $\overline{WR}$ • If 68 Series MPU is selected, data read is selected if R/W = High and data write is selected if R/W = Low.
$\overline{RD}$ (E)	Input	Input for Read Select signal (Input for Enable signal) • If 80 Series MPU is selected, data appears on DB0 to DB7 while $\overline{RD}$ = Low. • If 68 Series MPU is selected, this pin is used for the Input Enable signal.
RS	Input	Input for Register Mode Select signal • If RS = Low, this input is recognized as a register number. • If RS = High, this input is recognized as the data to be written to the register.
P/S	Input	Input for parallel/serial interface select signal • P/S = High → Parallel interface is selected. SI and SCK must be connected to V_{DD} or V_{SS}. • P/S = Low → Serial interface is selected. DB0 to DB7 must be open. $\overline{WR}$ and $\overline{RD}$ must be connected to V_{SS}.
68/80	Input	Input for 68/80 Series Parallel MPU Select signal • 68/80 = High → 68 Series parallel MPU is selected. • 68/80 = Low → 80 Series parallel MPU is selected.
SO	Output	Output for serial data
SI	Input	Input for serial data
SCK	Input	Input for serial clock
$\overline{RST}$	Input	Input for Reset signal • $\overline{RST}$ = Low → Reset state
$\overline{STB}$	Input	Input for Standby signal Usually connected to V_{DD}. • $\overline{STB}$ = Low → T6K41 is in Standby state. Column drive signals and row drive signals are at the V_{SS} level and the on-chip oscillator is stopped. • In standby state T6K41 can be accessed by the MPU.
OSC1	Input	Input for CR oscillator When using an external clock, input the clock to OSC1 and leave OSC2 and OSC3 open.

Pin Name	I/O	Functions
OSC2, OSC3	Output	Output for CR oscillator When using the internal clock oscillator, connect a resistor between OSC1 and OSC2 or between OSC1 and OSC3. OSC1 and OSC2: Oscillator for Normal Display Mode OSC1 and OSC3: Oscillator for Partial Display Mode
V_{IN}	—	Power supply for DC-DC converter Usually connected to V_{DD} The condition $V_{DD} \leqq V_{IN}$ must always be met.
C1A, C1B	—	External capacitor-connecting pin for ×2 DC-DC converter
C2A, C2B	—	External capacitor-connecting pin for ×3 DC-DC converter
C3A, C3B	—	External capacitor-connecting pin for ×4 DC-DC converter
C4A, C4B	—	External capacitor-connecting pin for ×5 DC-DC converter
C5A, C5B	—	External capacitor-connecting pin for ×6 DC-DC converter
V_{OUT}	—	DC-DC converter output pin
VREF	—	LV regulator output pin
V_{CC}	—	LCD driver power supply pin
VLC0 to VLC5	—	LCD drive power supply pin
V_{DD}, V_{SS}	—	Logic circuit power supply pin
M/S	Input	Input for Master/Save Select signal • M/S = High → T6K41 is a master chip. • M/S = Low → T6K41 is a slave chip.
CL	I/O	Input/Output for Shift Clock pulse • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input
PM	I/O	Input/Output for Frame signal • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input
FR	I/O	Input/Output for display alternating signal • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input
CK	I/O	Input/Output for system clock signal • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input
SYNC	I/O	Input/Output for gray-scale data synchronous signal • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input
BLNK	I/O	Input/Output for static icons blinking synchronous signal • Master Mode (M/S = High) → Output • Slave Mode (M/S = Low) → Input

Function Each Block

MPU interface unit

The T6K41 can be operated with an 80-Series MPU, 68-Series MPU or a serial interface.
Figure 1 shows an example of interface.



Case of 80-Series MPU (Using $\overline{CS1}$ signal)

Case of 68-Series MPU

Case of serial interface

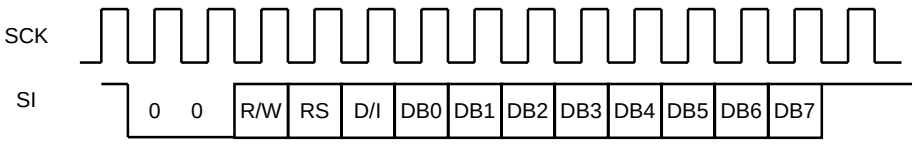
Figure 1

The T6K41 selects an 8-bit parallel or serial interface, allowing for data to transferred from the MPU.

P/S	68/80	Interface Type	$\overline{CS1}$	CS2	D/I	RS	$\overline{WR}$	$\overline{RD}$	SO	SI	SCK	DB0 to 7
H	L	80-Series MPU ($\overline{CS1}$)	An + 2	H	An	An + 1	$\overline{WR}$	$\overline{RD}$	Open	L/H	L/H	DB0 to 7
		80-Series MPU (CS2)	L	An + 2	An	An + 1	$\overline{WR}$	$\overline{RD}$	Open	L/H	L/H	DB0 to 7
	H	68-Series MPU	L	H	An	An + 1	R/W	E	Open	L/H	L/H	DB0 to 7
L	L	Serial	L	H	L/H	L/H	L/H	L/H	SO	SI	SCK	Open

Note 5: H denotes the V_{DD} level; L denotes the V_{SS} level.

<WRITE>



<READ>

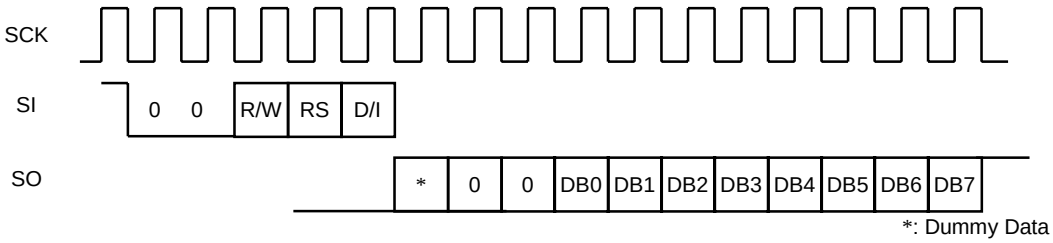


Figure 2

Register select circuit

This circuit transfers a register chosen by command to the data. T6K41 has R0 to R31 registers. The R23 to R31 registers are provided for test. Do not choose these registers.

Input register

This register stores 8-bit data from the MPU. The D/I signal discriminate between command data and display data.

X-address counter

The X-address counter is a 128-Up/Down counter. It holds the row address of the display RAM. When this counter is selected by a command, it is automatically incremented or decremented each time data is read or written to the display RAM.

Y (page) -address counter

The Y (page) -address counter is a 32-Up/Down counter. It holds the column address of the display RAM. When this counter is selected by a command, it is automatically incremented or decremented each time data is read or written to the display RAM.

Z-address counter

The Z-address counter is a 128-Up counter used to supply the display data stored in the display RAM to the LCD drive circuit. This counter is incremented by CL signal. The data held in the Z-address register is loaded into this counter as Z-address. For instance, when Z start address is 16, the counter increment like this: 16, 17, ,18···, 127, 128, 1, 2···, 14,15,16. Therefore, the display start line is 16-line of the display RAM.

X/Y counter up/down register

This register holds the data that selects the up-count or down-count mode for the X and Y counters.

X/Y counter select register

The register holds the data that selects the X or Y counter to be used.

Display ON/OFF register

This register holds the data that determines whether the display be turned ON or OFF. When turned OFF, the output data turns to default level. When turned ON, the display data appears according to the display RAM data. The display ON or OFF state does not affect the data of display RAM.

Duty cycle control register

This register holds the data that sets one of the four duty cycles that can be used.

FRS control register

This register holds FRS control data.

Contrast control register

This register holds contrast control data.

Oscillator control register

This register holds the data that controls oscillator.

Static icon control register

This register holds the data that controls static icons. The static icons are usually independent of the LCD drive circuit for a normal display, and holds contrast control data, display ON/OFF data, and blink control data.

Analog circuit ON/OFF register

This register holds the data that determines whether the internal analog circuit be turned ON or OFF.

Z-address register

This register holds the data that determines the display start line. By setting Z-address in this register successively, it is possible to scroll the display up or down.

Shift register

T6K41 has two 64-bit shift registers necessary to shift the turn-on data required for the LCD drive common signals.

Latch circuit

The circuit latches the data from the display RAM.

LCD drive circuit (segment)

The segment driver circuit consists of 128 driver circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the display data transferred from the latch circuit. Details of segment driver circuit are shown in Figure 3.

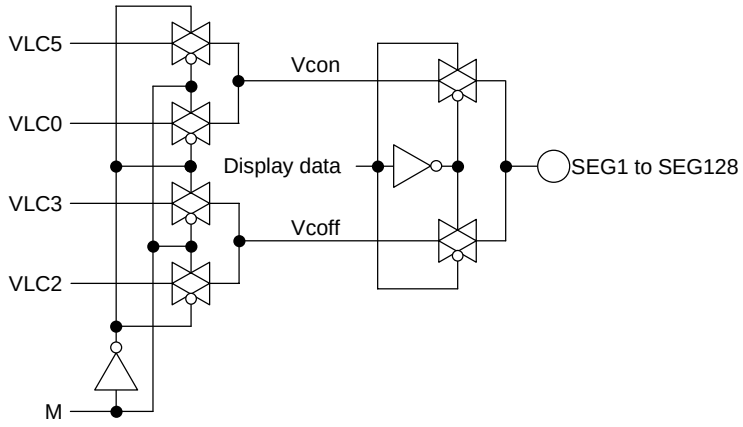


Figure 3

LCD driver circuit (common)

The common driver circuit consists of 128 driver circuits. One of the four LCD driving level is selected by the combination of M (internal signal) and the data from the shift register. Details of common driver circuit are shown in Figure 4.

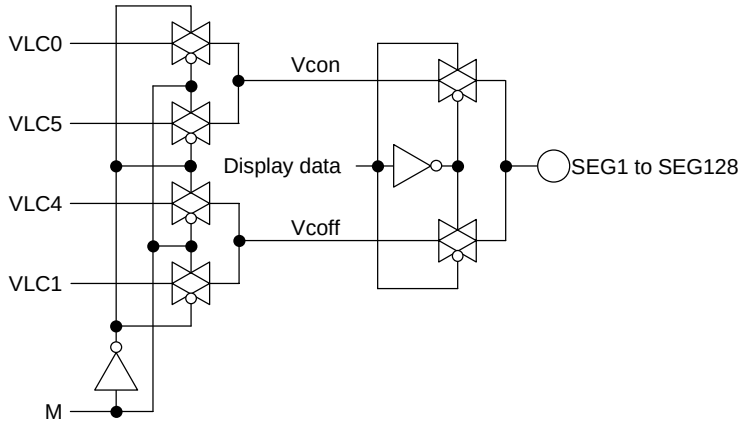


Figure 4

FRC (Frame Rate Control) circuit

The circuit controls ON/OFF of PWM data in each frame for generating the gray scale level. PWM (Pulse Width Modulation) is performed by gray scale data (the 2-bit display RAM data correspond to gray scale data). The gray scale data also determines whether PWM data is assigned to which frame.

Timing generation circuit

The circuit divides the signals from the oscillator and generates display timing signals and operating clock.

Op-Amp, Bias control circuit and Voltage divider resistors

The T6K41 has five op-amp for supplying LCD driving levels. To maintain good LCD contrast, connect a capacitor between the op-amp output and V_{SS}. The value of the capacitor should normally be 0.1 μF.
One of four biases can be selected by a bias control command.

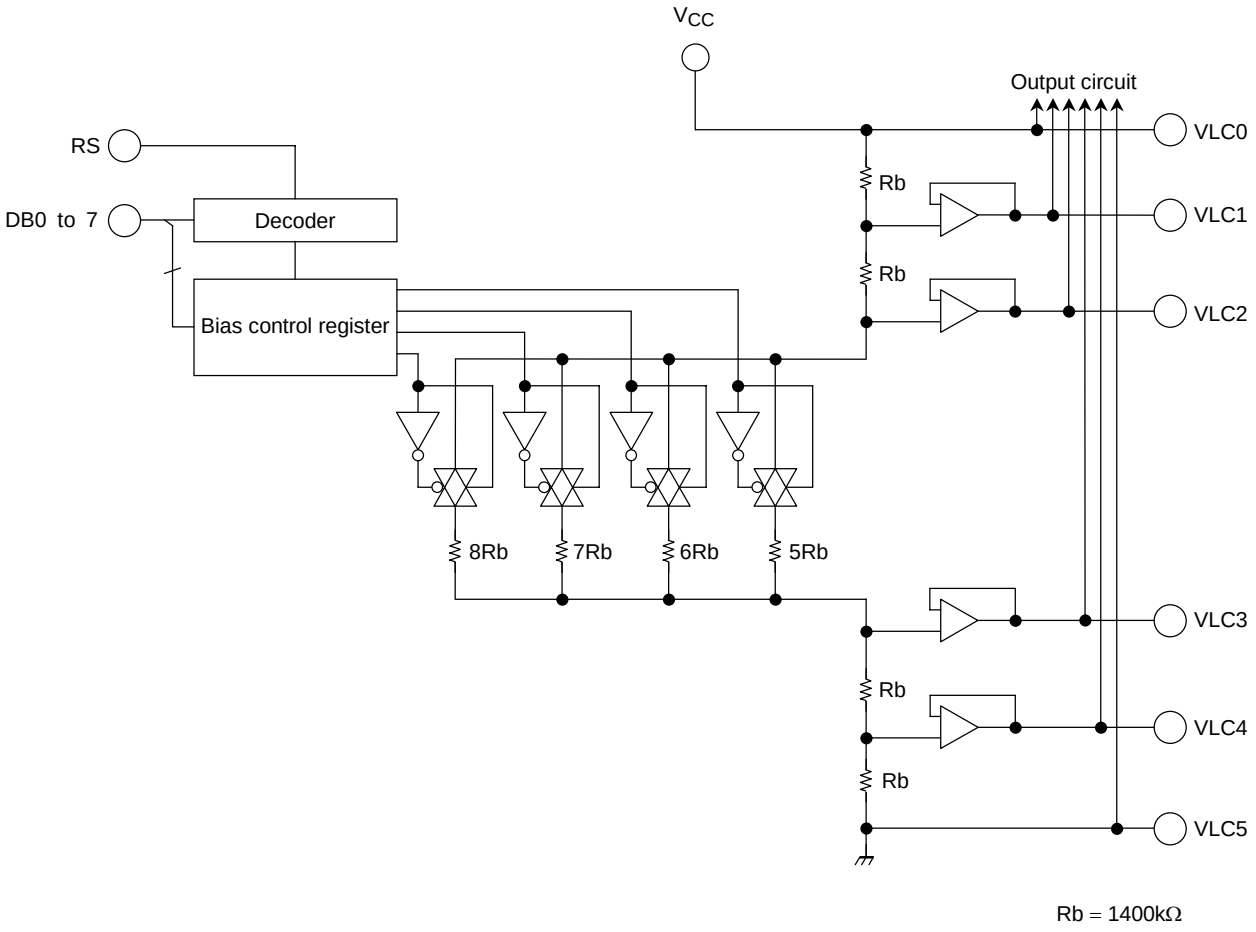


Figure 5

Oscillator

The T6K41 has two oscillators for normal display mode and partial display mode. When using internal oscillators, connect an external resistor for normal display mode between OCS1 and OSC2 and connect an external resistor for partial display mode between OSC1 and OSC3. When using external clock, input the clock to OSC1 after setting up Oscillation control resister data, as shown in Figure 7.

<CR oscillator>

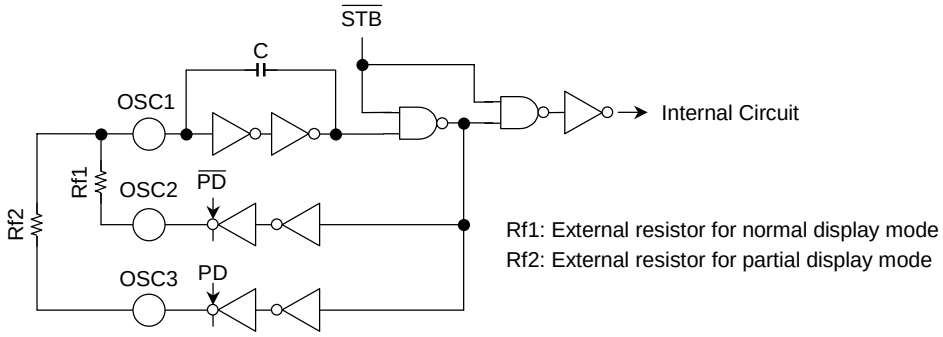


Figure 6

<External clock supply>

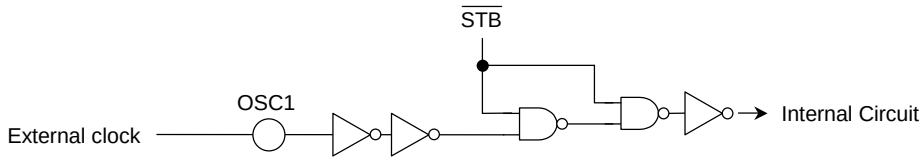


Figure 7

Static icon driver circuit

T6K41 has 16 static icons. Since this circuit is driven on logic system voltage (V_{DD}), the terminal of S1 to S16 and COMS outputs the LCD drive waveform of the level between V_{DD} to V_{SS}. The static icon is driven by 1/2duty and contrast adjustment is performed by changing the phase of an output waveform, as shown in Figure 8.
The ON period ratio of the drive voltage for the static icon is adjusted by changing the phase of the waveform between the COMS pin and S1 to S16 pins.

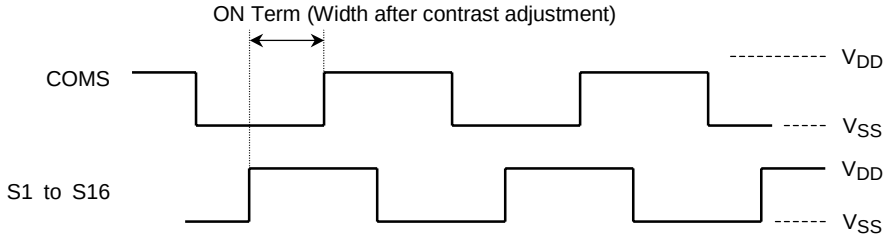


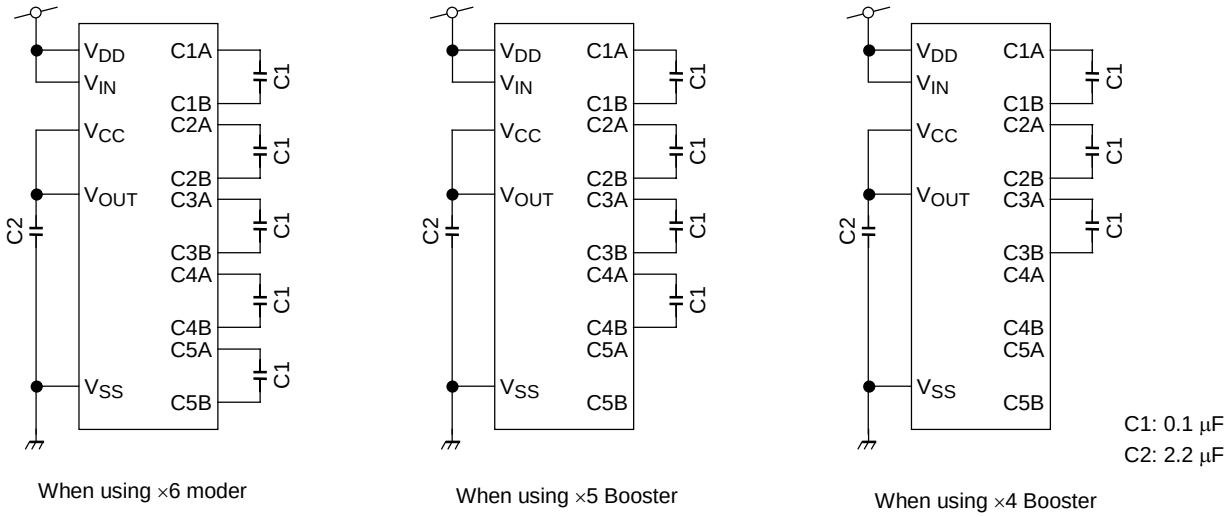
Figure 8

DC-DC converter

T6K41 contains a ×4/5/6 DC-DC converter. This circuit boosts by an external capacitor (charge pump system). By supping voltage to V_{IN}, this circuit can generate the boosted voltage selected by the command, and outputs the voltage from V_{OUT}. The boosted voltage is fed back to DC-DC converter circuit and the voltage adjusted by contrast control circuit is again outputted from V_{OUT}.

When using a DC-DC converter, short V_{OUT} and V_{CC}. As for the output voltage of V_{OUT}, 15.4 V or 13.0 V is the maximum value after a contrast control setup. Since more than 15.4 V or more than 13.0 V is not outputted, please be careful. In partial display mode, the DC-DC converter automatically changes to ×2 or ×3 mode. The output voltage of V_{OUT} is V_{IN} level in a standby state (/STB = "L") or a reset state (/RST = "L").

Refer to Figure 9 for the capacitor connection.



Note 6: Please set the capacitor value of C1 and C2 as the following ratio to suit the circuit characteristic.

C1:C2 = 1:More than 20

Figure 9

Contrast control circuit

The contrast control circuit feeds back the voltage outputted from V_{OUT} through built-in variable resistance, and outputs again contrast adjustment voltage to V_{OUT}. Therefore, the output voltage of V_{OUT} is the maximum of LCD drive voltage adjusted by contrast control circuit.

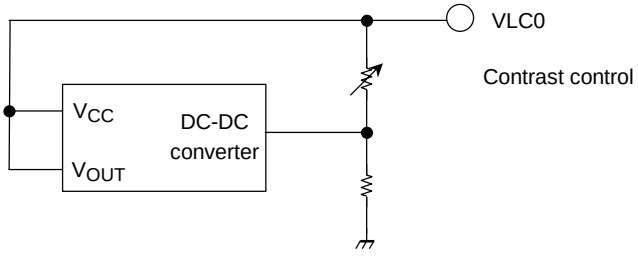


Figure 10

Command Definition

Command	Reg. No.	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set register	—	0	0	0	1	0	0	0	Register (0 to 31)				
Status read	—	0	0	1	0	*	*	PD	N/F	SI	DP	Y/X	U/D
Counter mode	R0	0	1	0	1	0	0	0	0	0	0	Y/X	U/D
Display mode	R1	0	1	0	1	0	CDR	SDR	0	PD	SI	N/F	DP
Set power control	R2	0	1	0	1	×6/×5/×4		×3/×2	0	0	Hi/Lo	OP	DC
Set duty/bias	R3	0	1	0	1	0	0	BIAS		0	0	DUTY	
Oscillator control	R4	0	1	0	1	0	0	0	0	0	0	EXT	OSC
Set X/Y-address	R5	0	1	0	1	1	X-address (0 to 127)						
		0	1	0	1	0	0	0	Y-address (0 to 31)				
Set Z-address	R6	0	1	0	1	0	Z-address (0 to 127)						
Set normal display contrast	R7	0	1	0	1	Contrast control for normal display (0 to 255)							
Set static icon contrast	R8	0	1	0	1	0	0	Contrast control for static icon display (0 to 63)					
Set static icon register (1)	R9	0	1	0	1	S4 state		S3 state		S2 state		S1 state	
Set static icon register (2)	R10	0	1	0	1	S8 state		S7 state		S6 state		S5 state	
Set static icon register (3)	R11	0	1	0	1	S12 state		S11 state		S10 state		S9 state	
Set static icon register (4)	R12	0	1	0	1	S16 state		S15 state		S14 state		S13 state	
Set partial display mode	R13	0	1	0	1	BIAS		Partial area size	Partial start area (0 to 15)				
Set alternating period	R14	0	1	0	1	0	0	0	0	0	FRS Control (0 to 7)		
Gray scale pallet for normal display	R15	0	1	0	1	Gray scale data for normal display (1) GS data to RAM data “00”							
	R16	0	1	0	1								
	R17	0	1	0	1	Gray scale data for normal display (2) GS data to RAM data “01”							
	R18	0	1	0	1								
	R19	0	1	0	1	Gray scale data for normal display (3) GS data to RAM data “10”							
	R20	0	1	0	1								
	R21	0	1	0	1	Gray scale data for normal display (4) GS data to RAM data “11”							
	R22	0	1	0	1								
Test mode	R23 to R31	0	1	0	1	Test mode (Do not access these registers.)							
Data write	—	1	1	0	1	Write data							
Data read	—	1	1	1	0	Read data							

- Set register

  T6K41 has registers for command (R0 to R31). But, R23 to R31 registers are provided for LSI test. Do not access these registers. If you access these registers inadvertently, you must be execute a re-setup of a register after executing reset function of T6K41.

- R0: Counter mode

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	0	0	Y/X	U/D

Y/X: Selects Y-Counter or X-Counter.
Y/X = 1: Y-Counter is selected.
Y/X = 0: X-Counter is selected.
U/D: Selects Up mode or Down mode.
U/D = 1: Up mode is selected.
U/D = 0: Down mode is selected.

- R1: Display mode

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	CDR	SDR	0	PD	SI	N/F	DP

CDR: Sets the common data scanning direction.
CDR = 1: Data is scanned in the direction COM1 → COM128.
CDR = 0: Data is scanned in the direction COM128 → COM1.
SDR: Sets the segment data direction.
SDR = 1: SEG1 → SEG4 with respect to the data direction DB7 → DB0.
SDR = 0: SEG1 → SEG4 with respect to the data direction DB0 → DB7.

Note 7: For details, see Figure 11 on Function Description.

PD: Turns partial display ON or OFF.
DP = 1: Partial display is turned ON
DP = 0: Partial display is turned OFF. (Normal display)
SI: Turns static icons ON or OFF.
SI = 1: Static icons are turned ON.
SI = 0: Static icons are turned OFF.
N/F: Selects between normal display and icon display modes.
N/F = 1: Normal display mode is selected.
N/F = 0: Icon display mode is selected.

Display mode

Display Mode	Normal Display	Static Icons
Normal display mode	valid	valid
Power save mode	invalid	valid

Note 8: When power save mode (icon display mode) is selected, only static icon can be displayed.

DP: Turns display ON or OFF.
DP = 1: Display is turned ON.
DP = 0: Display is turned OFF.

- R2: Set power control

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	×6/×5/×4		×3/×2	0	0	Hi/Lo	OP	DC

×6/×5/×4: Selects booster level in Normal Display mode

DB7	DB6	Booster
1	0	×6
0	1	×5
0	0	×4

×3/×2: Selects booster level in Partial Display mode.
×3/×2 = 1: ×3 booster
×3/×2 = 0: doubler

Hi/Lo: Selects LCD drive voltage (V_{OUT}).
Hi/Lo = 1: V_{OUT} = 15.4 V (typ.)
Hi/Lo = 0: V_{OUT} = 13.0 V (typ.)

OP: Controls op-amp for driving LCD.
OP = 1: Op-amp for driving LCD ON
OP = 0: Op-amp for driving LCD OFF
(Externally supply V_{CC} and VLC1 to VLC4 via op-amp.)

DC: Controls booster (DC-DC converter).
DC = 1: Booster ON
DC = 0: Booster OFF

- R3: Set Duty/Bias
Sets duty/bias in Normal Display mode.

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	BIAS (0 to 3)		0	0	DUTY (0 to 3)	

BIAS: Sets a power supply bias for LCD drive.

DB5	DB4	
1	1	Set to 1/12 bias.
1	0	Set to 1/11 bias.
0	1	Set to 1/10 bias.
0	0	Set to 1/9 bias.

DUTY : Sets a display duty cycle.

DB1	DB0	
1	1	Set to 1/128 duty
1	0	Set to 1/100 duty
0	1	Set to 1/80 duty
0	0	Set to 1/72 duty

- R4: Oscillation control

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	0	0	EXT	OSC

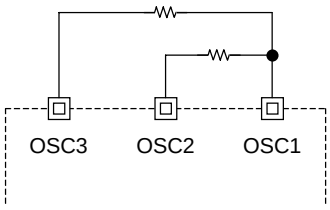
EXT: Switches input.
EXT = 1: Inputs external clock.
EXT = 0: Uses internal oscillator.
OSC: Controls internal oscillator.
OSC = 1: Internal oscillator ON
OSC = 0: Internal oscillator OFF

Switching between Normal Display and Partial Display modes switches oscillator resistor when an internal oscillator is used (EXT = 0).
Normal Display mode: resistor between OSC1 and OSC2
Partial Display mode: resistor between OSC1 and OSC3

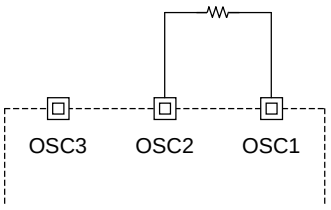
Divides the frequency from the selected oscillator to obtain the static icon clock.

To switch between Normal Display and Partial Display modes using external clock input, the clock frequency must be changed according to the display mode.

<Example when internal oscillator is used>

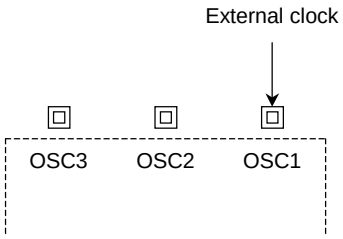


In Partial Display mode



In Non-Partial Display mode

<External clock input>



Recommended frequency
(V_{DD} = 3.0 V, FR = 70 Hz, Ta = 25°C)

Display Mode	Duty	Frequency (typ.)
Normal display	1/128	Fosc2 = 80.64 kHz
	1/100	Fosc2 = 63.0 kHz
	1/80	Fosc2 = 50.4 kHz
	1/72	Fosc2 = 45.36 kHz
Partial display mode	1/32	Fosc3 = 20.16 kHz
	1/24	Fosc3 = 15.12 kHz
	1/16	Fosc3 = 10.08 kHz
	1/8	Fosc3 = 5.04 kHz

- R5: Set X/Y-address

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	1	X-address (0 to 127)						
					0	0	0	Y-address (0 to 31)				

(1) Set X-address

Setting DB7 to 1 acknowledges an X-address. The address is controlled as a vertical address of the screen image. Using the X-up/down counter automatically enables write and read. The X-up/down counter counts addresses on the specified horizontal line only.

(2) Set Y-address

Setting DB7 to 0 acknowledges a Y-address. The address is controlled as a horizontal address of the screen image. Using the Y-up/down counter automatically enables write and read. The Y-up/down counter counts addresses on the specified vertical line only.

- R6: Set Z-address

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	Z-address (0 to 127)						

Sets the start line of display RAM. Setting this address enables vertical scrolling. For the scroll function, see the detailed description.

- R7: Set normal display contrast

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Contrast control (0 to 255)							

Sets contrast control of the Normal Display area. When set to 0, contrast is the minimum. When set to 255, contrast is the maximum.

Note 9: that if a doubler is selected in Partial Display mode, set DB7 = 1 and set a step from 1 to 128.

- R8: Set static icon contrast

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	Contrast control (0 to 63)					

Sets contrast control of the static icon area. When set to 0, contrast is the minimum. When set to 63, contrast is the maximum. The ON period ratio of the drive voltage for the static icon area is adjusted by changing the phase of the waveform between the COMS pin and pins S1 to S16.

- R9: Set static icon register (1)

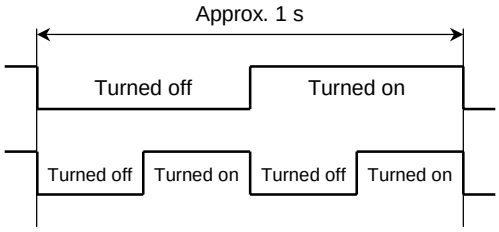
	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	S4 state		S3 state		S2 state		S1 state	

Sets ON/OFF of static icons S1 to S4. When a static icon is ON (R1: SI = 1), S1 to S4 are turned on according to the setting of this register. When a static icon is OFF (R1: SI = 0), the display is off regardless of the setting of this register.

Static icon states vary as shown below according to the 2-bit data.

S1 to S16 state

0	0	OFF
0	1	ON (Blinks at intervals of about 1 second)
1	0	ON (Blinks at intervals of about 0.5 seconds)
1	1	ON



- R10: Set static icon register (2)

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	S8 state		S7 state		S6 state		S5 state	

Sets ON/OFF of the static icons S5 to S8. When a static icon is ON (R1: SI = 1), S5 to S8 are turned on according to the setting of this register. When a static icon is OFF (R1: SI = 0), the display is off regardless of the setting of this register.

- R11: Set static icon register (3)

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	S12 state		S11 state		S10 state		S9 state	

Sets ON/OFF of the static icon S9 to S12. When a static icon is ON (R1: SI = 1), S9 to S12 are turned on according to the setting of this register. When a static icon is OFF (R1: SI = 0), the display is off regardless of the setting of this register.

- R12: Set static icon register (4)

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	S16 state		S15 state		S14 state		S13 state	

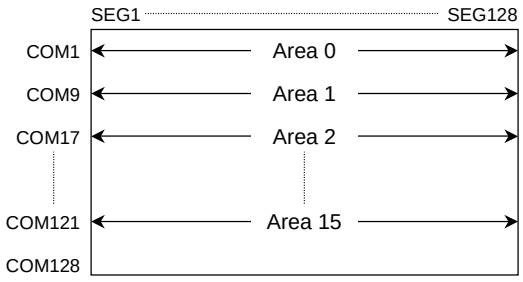
Sets ON/OFF of the static icon S13 to S16. When a static icon is ON (R1: SI = 1), S13 to S16 are turned on according to the setting of this register. When a static icon is OFF (R1: SI = 0), the display is off regardless of the setting of this register.

- R13: Set partial display mode

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Bias		Partial area size		Partial start area			

Set partial start area

DB3	DB2	DB1	DB0	Start Area
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	1
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14



Sets the partial display start area. The partial display start area can be specified in units of 8 lines (8 COMs).

Set partial area size

DB5	DB4	Partial Area Size
0	0	8 lines mode
0	1	16 lines mode
1	0	24 lines mode
1	1	32 lines mode

Sets the partial display area size. A partial display area of the set size is displayed from the partial display start area.

Set bias

DB7	DB6	BIAS
0	0	1/4 bias
0	1	1/5 bias
1	0	1/6 bias
1	1	1/7 bias

Sets bias in Partial Display mode.

- R14: Set alternating period

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	0	0	0	0	0	FRS Control (0 to 7)		

This command sets the number of lines at which intervals the polarity of the frame signal (alternating signal) is switched over.

DB2	DB1	DB0	
1	1	1	FR signal inverts on every 19 lines.
1	1	0	FR signal inverts on every 17 lines.
1	0	1	FR signal inverts on every 13 lines.
1	0	0	FR signal inverts on every 11 lines.
0	1	1	FR signal inverts on every 7 lines.
0	1	0	FR signal inverts on every 5 lines.
0	0	1	FR signal inverts on every 3 lines.
0	0	0	In case 1/n duty is selected by R3, FR signal inverts on every n lines.

- R15 to R22: Gray scale pallet for normal display

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	R15/16: Gray scale data for normal display (1)							
					R17/18: Gray scale data for normal display (2)							
					R19/20: Gray scale data for normal display (3)							
					R21/22: Gray scale data for normal display (4)							

This register stores the data for generating the gray scale level. The gray scale is created by pulse width modulation (PWM) and frame rate control (FRC). Use two registers for each gray scale level. Set the PWM data for the first to fourth frames in these registers. Four bits of PWM data are eliminated from a frame. Four frames are used to display one gray scale level. Frames (1) to (4) above correspond to display data 00, 01, 10 and 11, respectively. Any gray scale level is assigned to the display data values (00, 01, 10 and 11).

Frame Rate control (FRC) setting

The T6K41 determines the gray scale level by specifying the PWM to be performed in the four frames. The correspondence between frame control order and the registers is shown in the table below.

Register	Data Bus							
	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R15/R17/R19/R21	Data eliminated from second frame				Data eliminated from first frame			
R16/R18/R20/R22	Data eliminated from fourth frame				Data eliminated from third frame			

Note 10: Eliminated data are PWM data.

PWM (pulse width modulation) setting

The T6K41 determines the gray scale level by dividing the segment data ON waveform by nine. The data to be written to the register are selected from the gray scale levels listed below.

BIN	HEX	PWM (on width)	Note
0000	00	0 (0/9)	
0001	01	1/9	
0010	02	2/9	
0011	03	3/9	
0100	04	4/9	
0101	05	5/9	
0110	06	6/9	
0111	07	7/9	
1000	08	8/9	
1001	09	1 (9/9)	
1010 to 1111	0A to 0F	0 (0/9)	These data select off level (0 level).

Note 11: Optimization by combination of PWM and FRC data depends on the characteristics of the LCD.

- R23 to R31: Test mode

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Test mode							

This command selects a test mode, so do not use it. If you've used this test command inadvertently, deassert it by pulling the $\overline{RST}$ input low

- Data Write

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	0	1	Write data							

Writes 8-bit data to display RAM. Using the X/Y counter automatically counts up/down addresses after specifying the start address so that data can be written.

- Data Read

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	1	0	Read data							

Reads 8-bit data from display RAM. Using the X/Y counter automatically counts up/down addresses after specifying the start address so that data can be read.

- Status read

	D/I	RS	$\overline{WR}$	$\overline{RD}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	0	*	*	*	N/F	SI	DP	Y/X	U/D

N/F (DB4): Identifies Normal Display mode or Power Save mode.
N/F = 1: Indicates Normal Display mode.
N/F = 0: Indicates Power Save mode.
SI (DB3): Identifies static icon ON/OFF.
SI = 1: Static icon ON
SI = 0: Static icon OFF
DP (DB2): Identifies display ON/OFF.
DP = 1: Display ON
DP = 0: Display OFF
Y/X (DB1): Identifies Y or X counter.
Y/X = 1: Y counter is selected.
Y/X = 0: X counter is selected.
U/D (DB0): Identifies Counter Up or Down mode.
U/D = 1: Counter Up mode
U/D = 0: Counter Down mode

Reset Function

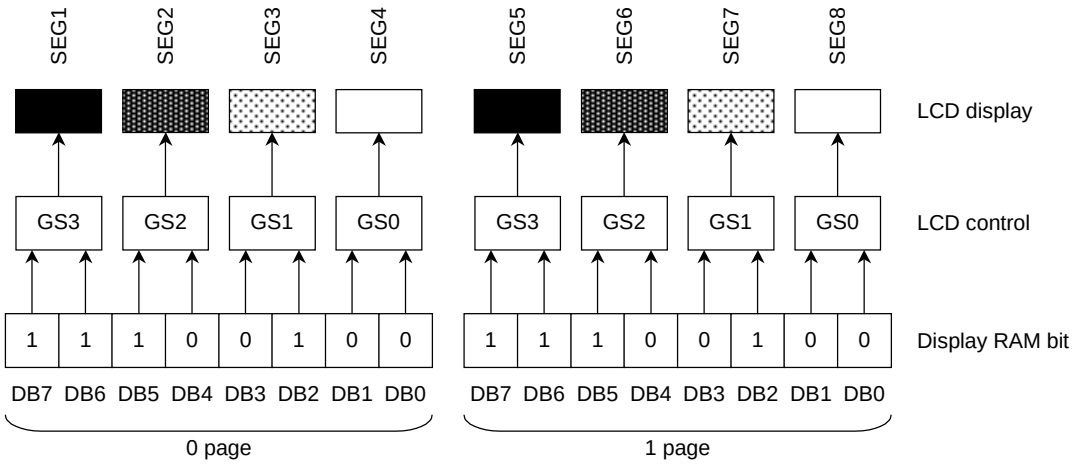
The T6K41 has a $\overline{\text{RST}}$ pin. When input to this pin is pulled low, the T6K41 is reset, with its internal circuits (register contents) initialized as shown below.

Command	Reg. No.	D7	D6	D5	D4	D3	D2	D1	D0
Counter mode	R0	0	0	0	0	0	0	1	1
		*	*	*	*	*	*	Y/X	U/D
Display mode	R1	0	1	1	0	0	0	1	0
		*	CDR	SDR	*	PD	SI	N/F	DP
Power control	R2	1	0	0	0	0	1	0	0
		×6/×5/×4		×3/×2	*	*	Hi/Lo	OP	DC
Set Duty/Bias	R3	0	0	1	1	0	0	1	1
		*	*	BIAS		*	*	DUTY	
Oscillator setting	R4	0	0	0	0	0	0	1	1
		*	*	*	*	*	*	EXT	OSC
Set X/Y-address	R5	0	0	0	0	0	0	0	0
		*	X-address/Y-address						
Set Z-address	R6	0	0	0	0	0	0	0	0
		*	Z-address						
Contrast setting in Normal Display mode	R7	0	0	0	0	0	0	0	0
		Contrast control data for normal display							
Contrast setting for static icon	R8	0	0	0	0	0	0	0	0
		*	*	Contrast control for static icon					
Static icon setting	R9 to R12	0	0	0	0	0	0	0	0
		S1 to S16 states (specify in two bits)							
Partial display setting	R13	0	0	0	0	0	0	0	0
		BIAS		Area size	Display start area				
Alternating current signal setting	R14	0	0	0	0	0	0	0	0
		*	*	*	*	*	Alternating current signal		
Setting of gray scale pallet for normal display	R15 to R22	0	0	0	0	0	0	0	0
		Gray scale data for normal display							

Function Description

- Display data bit

(1) When SDR = 1



(2) When SDR = 0

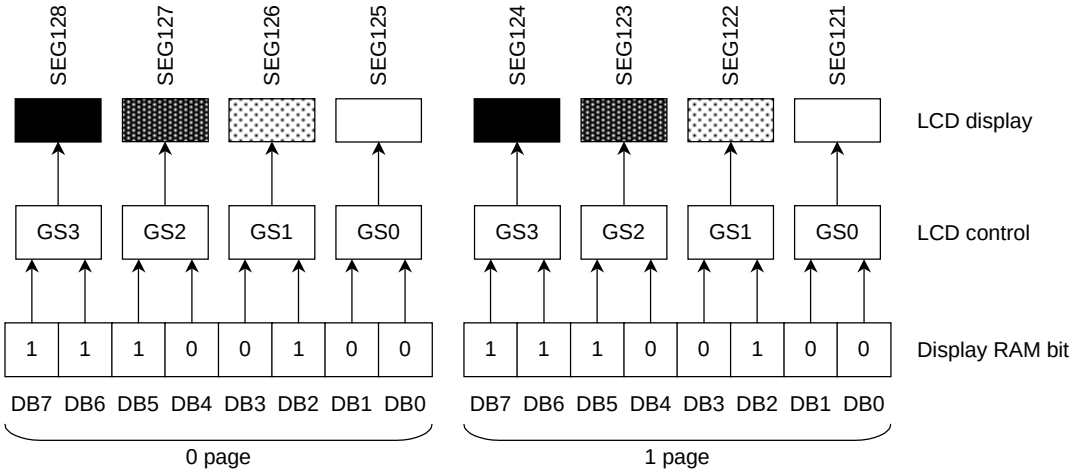


Figure 11

- The relationship between the Duty and the LCD drive common signal output
  T6K41 can change Duty by command setup. When CDR = 1, assignment of LCD drive common signal output (COM) pins are as shown below.

Duty	Assignment of COM pins	Number of using pins
1/128 duty	COM1···COM128	128
1/100 duty	COM1 ··· COM50, COM65 ··· COM114	100
1/80 duty	COM1 ··· COM40, COM65 ··· COM104	80
1/72 duty	COM1 ··· COM36, COM65 ··· COM100	72

- Partial Display function
  The T6K41 has the partial display function for displaying arbitrary area by command setup. The partial display area size can be selected from 8 lines, 16 lines, 24 lines, or 32 lines. The partial start area (start line) can be selected from the following table.

R13	Partial Start Area No	Display Start Line	R13	Partial Start Area	Display Start Line
x0H	0	COM1	x8H	8	COM65
x1H	1	COM9	x9H	9	COM73
x2H	2	COM17	xAH	10	COM81
x3H	3	COM25	xBH	11	COM89
x4H	4	COM33	xCH	12	COM97
x5H	5	COM41	xDH	13	COM105
x6H	6	COM49	xEH	14	COM113
x7H	7	COM57	xFH	15	COM121

Note 12: x: Invalid

Z address determines the effective display RAM area. For instance, when the partial display area size is set to 16 lines and the partial start area no. is set to 0, the data of effective display RAM area shown below by Z-address setup is displayed on 16 lines from COM1.

When Z-address (ZAD) is set to 0, the range of XAD = 0 to XAD = 15 are effective

When Z-address (ZAD) is set to 30, the range of XAD = 30 to XAD = 46 are effective.

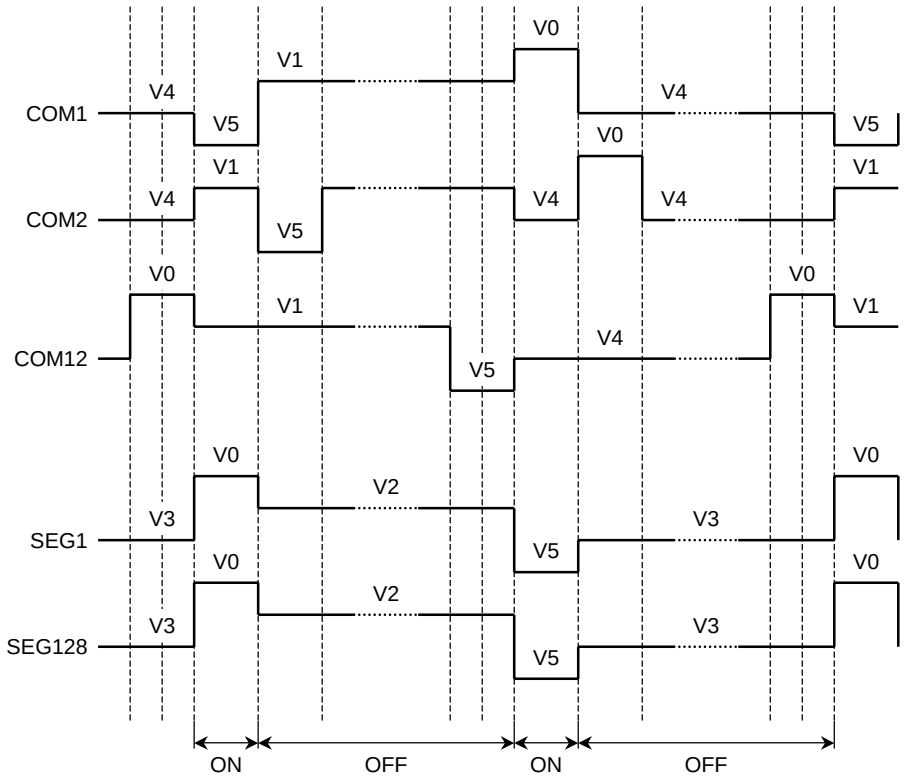
- Expansion function
  The T6K41's expansion function, allows two, T6K41s to drive an LCD panel of up to 256 by 128 dots. The table below shows the timing signals state by using M/S pin.

M/S	Timing signal output/input for Expansion					
	CL	PM	FR	CK	SYNC	BLNK
H	Output	Output	Output	Output	Output	Output
L	Input	Input	Input	Input	Input	Input

The table below shows the selectable function by using M/S pin.

M/S	
H	L
・ Single-chip mode Disable expansion mode ・ Two-chip mode (Master chip) Timing signals and power voltage supply to Slave chip.	・ Two-chip mode (Slave chip) Timing signals and power voltage are supplied from Master chip.

LCD Drive Waveform (Normal Display mode)



LCD Drive Timing Chart (1/128 duty)

Maximum Ratings

Characteristics	Symbol	Rating	Unit
Power supply voltage (1)	V_{DD}, V_{IN} (Note 13)	−0.3 to 6.0	V
Power supply voltage (2)	VLC0, 1, 2, 3, 4, 5, V_{CC}, V_{OUT}	V_{SS} + 18.0 to V_{SS} − 0.3	V
Input voltage	Vinp (Note 13, 14)	−0.3 to V_{DD} + 0.3	V
Operating temperature	T_{opr}	−30 to 85	°C
Storage temperature	T_{stg}	−55 to 125	°C

Note 13: Value based on V_{SS} = 0 V

Note 14: Applies to input and data bus excluding V_{CC}, V_{OUT}, VLC0, VLC1, VLC2, VLC3, VLC4 and VLC5.

Electrical Characteristics (1)

(Test Conditions: Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable
Operating voltage (1)		V_{DD}	—	—	2.4	—	3.3	V	V_{DD}
Operating voltage (2)		V_{IN}	—	—	2.7	—	3.3	V	V_{IN}
Operating voltage (3)	Normal display	V_{CC}	—	—	6.0 – V_{SS}	—	16.5 – V_{SS}	V	V_{CC}, V_{OUT}
	Partial display	V_{CC}	—	—	4.0 – V_{SS}	—	16.5 – V_{SS}	V	V_{CC}, V_{OUT}
Input voltage	High level	V_{IH}	—	—	0.8 × V_{DD}	—	V_{DD}	V	DB0 to DB7, D/I, $\overline{WR}$, $\overline{RD}$, $\overline{CS1}$, CS2, RS, P/S, 68/80, SI, SCK, $\overline{RST}$, $\overline{STB}$, CL, PM, FR, SYNC, CK, BLNK
	Low level	V_{IL}	—	—	0	—	0.2 × V_{DD}	V	
Output voltage	High level	V_{OH}	—	I_{OH} = –400 μA	V_{DD} – 0.2	—	V_{DD}	V	DB0 to DB7, SO, CL, PM, FR, SYNC, CK
	Low level	V_{OL}	—	I_{OL} = 400 μA	0	—	0.2	V	
Segment driver on-resistance	Normal Display mode	Rcol	—	(Note 15)	—	—	7.5	kΩ	SEG1 to SEG128
Common driver on-resistance	Normal Display mode	Rrow	—	(Note 15)	—	—	1.5	kΩ	COM1 to COM128
Static icon on-resistance	Low Power Consumption mode	Ricon	—	(Note 16)	—	—	7.5	kΩ	COMS, S1 to S16
Input leakage current		I_{IL}	—	Vinp = V_{DD} to GND	–1	—	1	μA	DB0 to DB7, D/I, $\overline{WR}$, $\overline{RD}$, $\overline{CS1}$, CS2, RS, P/S, 68/80, SI, SCK, $\overline{RST}$, $\overline{STB}$, CL, PM, FR, SYNC, CK, BLNK
Operating frequency		fosc	—	(Note 22)	—	80.64	—	kHz	OSC1
External clock input frequency		fex	—	(Note 22)	—	80.64	—	kHz	OSC1
External clock duty		fduty	—	—	45	50	55	%	OSC1
External clock rise/fall time		t_r/t_f	—	—	—	—	50	ns	OSC1
Current consumption (1)		I_{SS1}	—	(Note 17)	—	300	450	μA	V_{SS}
Current consumption (2)		I_{SS2}	—	(Note 18)	—	60	90	μA	V_{SS}
Current consumption (3)		I_{SS3}	—	(Note 19)	—	4	6	μA	V_{SS}
Current consumption (4)		I_{SS4}	—	(Note 20)	—	500	700	μA	V_{SS}
Current consumption (5)		I_{SSSTB}	—	(Note 21)	–1	—	1	μA	V_{SS}

Note 15: V_{CC} = 10.3 V, Load current ± 100 μA, 1/9 bias

Note 16: V_{DD} = 3.0 V, Load current ± 100 μA, 1/4 bias

Note 17: V_{DD} = 3.0 V, V_{OUT} = 15.4 V (×6 booster), no data access, internal clock (OSC = 80.64 kHz), no load, 1/12 bias, 1/128 duty, op-amp on, regulator on, Normal Display mode (Gray Scale), display pattern: check

Note 18: V_{DD} = 3.0 V, V_{OUT} = 5.2 V (doubler), no data access, internal clock (OSC = 5 kHz), no load, 1/4 bias, 1/8 duty, op-amp on, regulator on, Partial Display mode, display pattern: check

Note 19: V_{DD} = 3.0 V, no data access, internal clock (OSC = 5.04 kHz), no load, op-amp off, regulator off, Low Power Consumption mode

Note 20: V_{DD} = 3.0 V, V_{OUT} = ×6 booster, data access cycle (f/CE = 1 MHz), internal clock (OSC = 82 kHz), no load, 1/12 bias, 1/128 duty, op-amp on, regulator on

Note 21: V_{DD} = 3.3 V, V_{CC} – V_{SS} = 16.0 V, $\overline{STB}$ = "L"

Note 22: 1/128 duty, fFR = 70 Hz

Electrical Characteristics (2)

(Test Conditions: Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = V_{IN} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable
Regulator reference high voltage (1) (Hi/Lo = 1)	VHR1	—	Ta = 25°C (Note 23)	15.3	15.4	15.5	V	V_{OUT}
Regulator reference high voltage (2) (Hi/Lo = 0)	VHR2	—	Ta = 25°C (Note 24)	12.9	13.0	13.1	V	V_{OUT}
Regulator reference high voltage (3) (Partial display mode)	VHR3	—	Ta = 25°C (Note 24)	7.9	8.0	8.1	V	V_{OUT}
Regulator reference high voltage temperature gradient	VHRINC	—	Ta = −20 to 60°C (Note 23)	TBD	−0.05	TBD	%/°C	V_{OUT}

Note 23: V_{DD} = V_{IN} = 3.0 V, contrast = max, no display load, Normal Display mode

Note 24: V_{DD} = V_{IN} = 3.0 V, contrast = max, no display load, Partial Display mode

Electrical Characteristics (3)

(Test conditions: unless otherwise specified, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

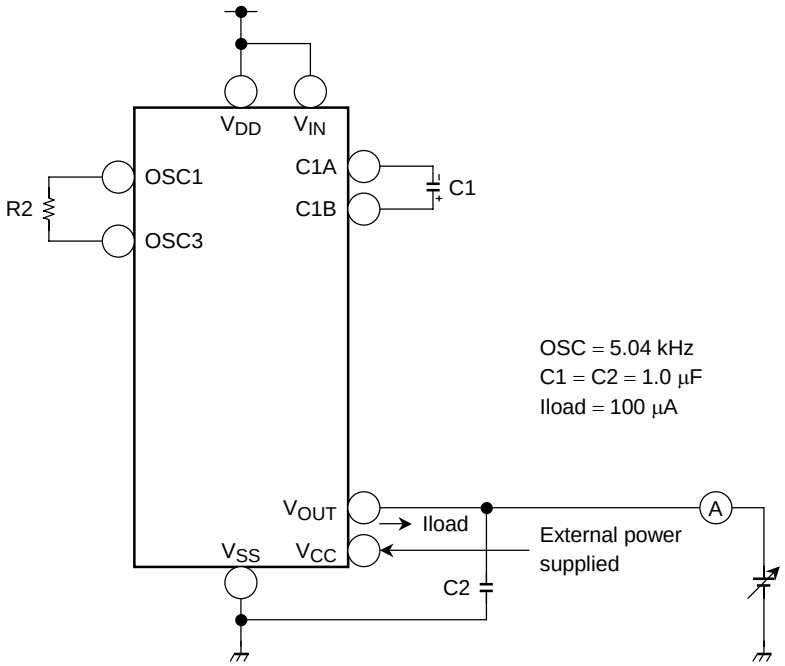
Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit	Applicable
Op-amp output voltage offset (1)	Vopoff	—	(Note 25)	−100	—	100	mV	VLC0, VLC1, VLC2, VLC3, VLC4
Op-amp output voltage offset (2)	Vopoffs1	—	(Note 26)	−100	—	100	mV	VLC0, VLC1, VLC2, VLC3, VLC4
Op-amp output voltage offset (3)	Vopoffs2	—	Iload = ±100 μA	−130	—	130	mV	VLC0, VLC1, VLC2, VLC3, VLC4

Note 25: V_{DD} = 2.7 to 3.3 V, V_{SS} = 0 V, 1/12 bias, 1/128 duty, V_{CC} = 15.4 V, op-amp on, no load
VLC0: VLC0 = Vopoff
VLC1: (VLC0 × 11/12) − VLC1 = Vopoff
VLC2: (VLC0 × 10/12) − VLC2 = Vopoff
VLC3: (VLC0 × 2/12) − VLC3 = Vopoff
VLC4: (VLC0 × 1/12) − VLC4 = Vopoff

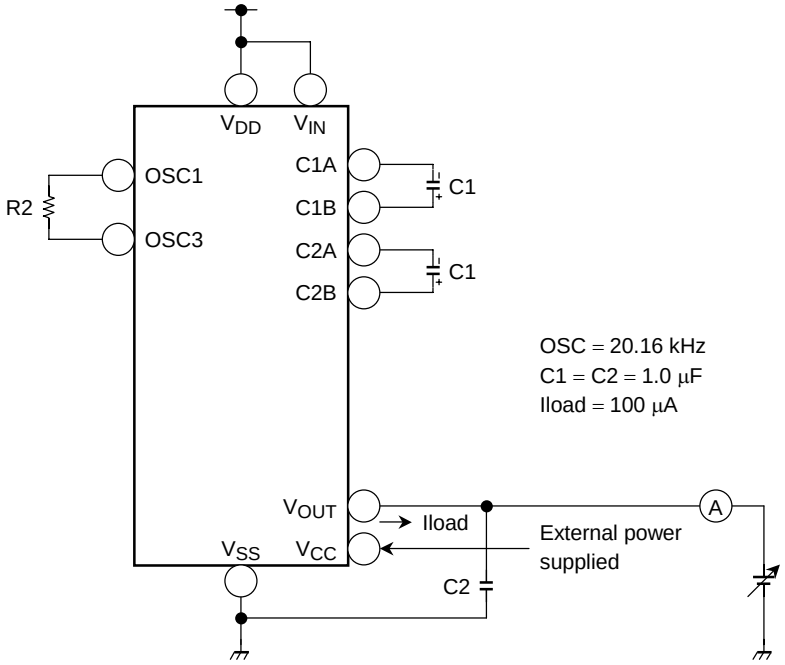
Note 26: V_{DD} = 2.7 to 3.3 V, V_{SS} = 0 V, 1/12 bias, 1/128 duty, V_{CC} = 16.0 V, op-amp on, no load
Vopoff1 = ((VLC1 − VLC2) − (VLC0 − VLC1)) + ((VLC3 − VLC4) − (VLC4 − VLC5))
Vopoff2 = ((VLC1 − VLC2) − (VLC0 − VLC1)) + ((VLC3 − VLC4) − (VLC4 − VLC5))

Test Circuit

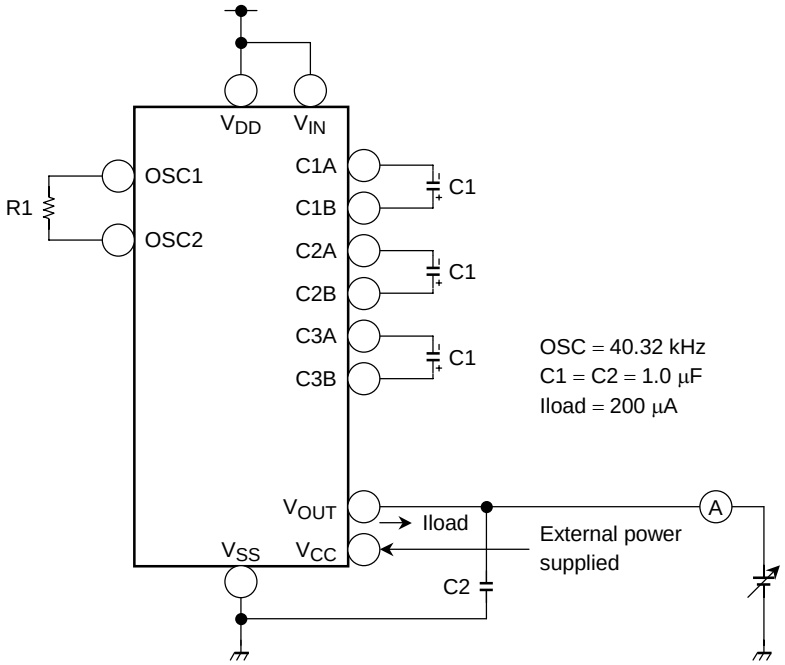
(1) With doubler



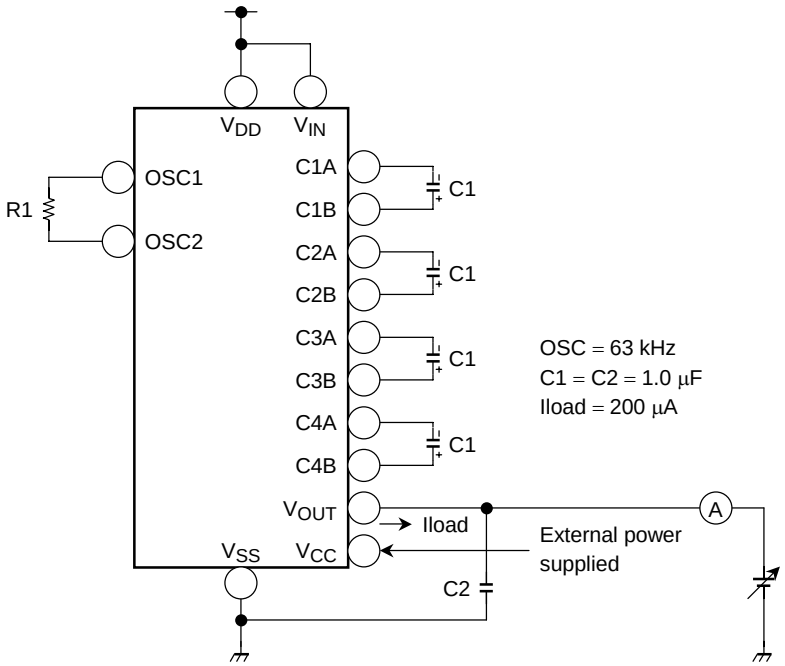
(2) With ×3 booster



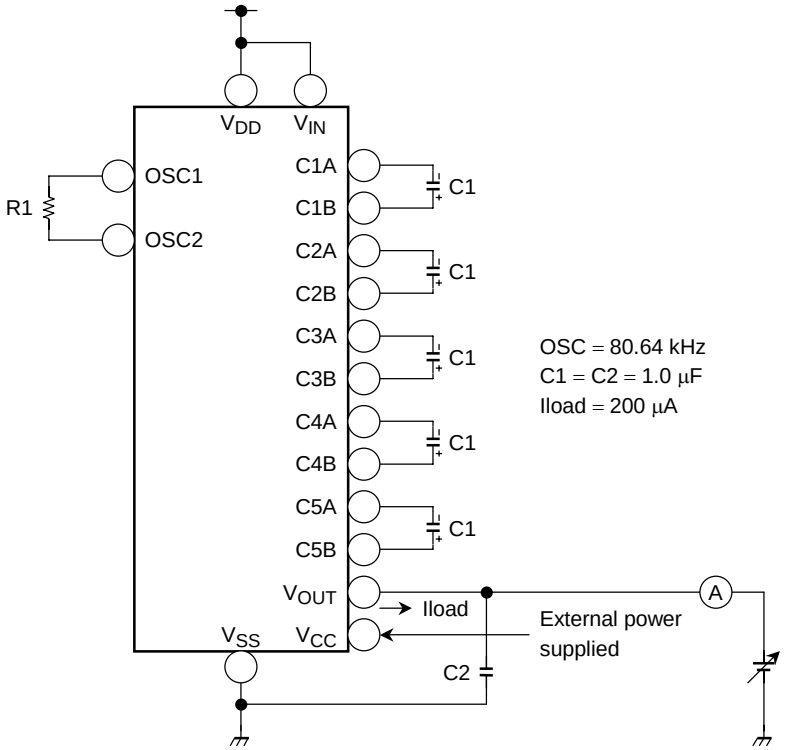
(3) With ×4 booster



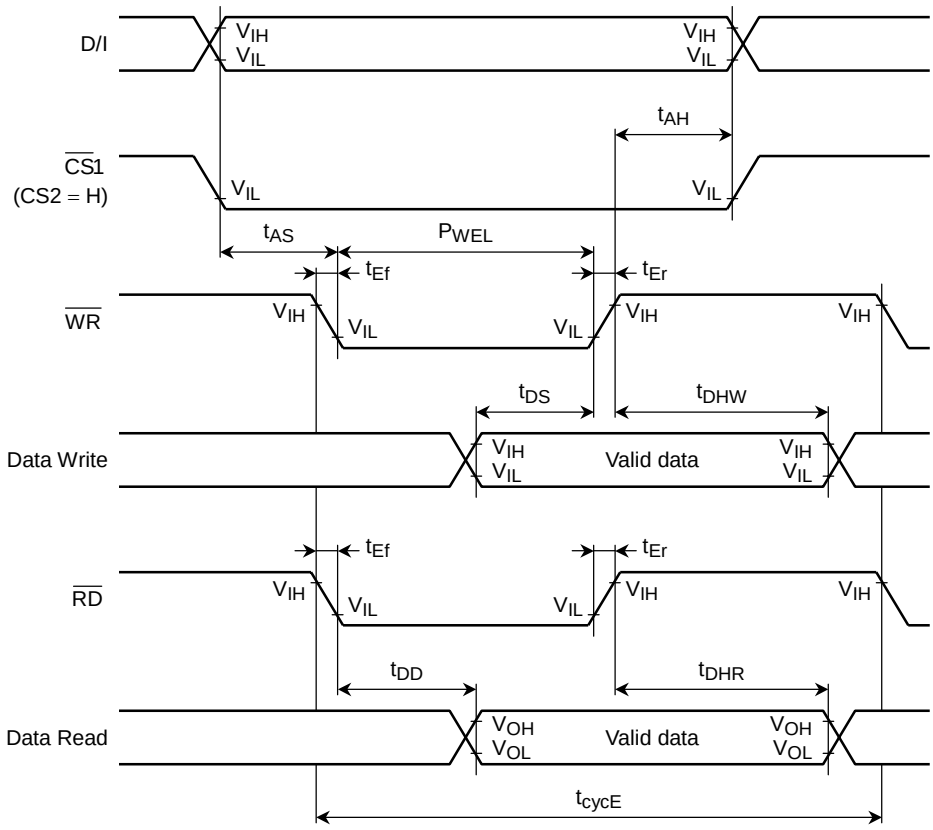
(4) With ×5 booster



(5) With ×6 booster



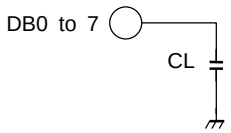
Switching Characteristics (1) (8-bit 80 series MPU interface)



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	500	—	ns
Enable pulse width	P_{WEL}	410	—	
Enable rise/fall time	t_{Er}, t_{Ef}	—	25	
Address setup time	t_{AS}	20	—	
Address hold time	t_{AH}	0	—	
Data setup time	t_{DS}	100	—	
Write data hold time	t_{DHW}	20	—	
Data delay time	t_{DD} (Note 27)	—	300	
Read data hold time	t_{DHR} (Note 27)	20	—	

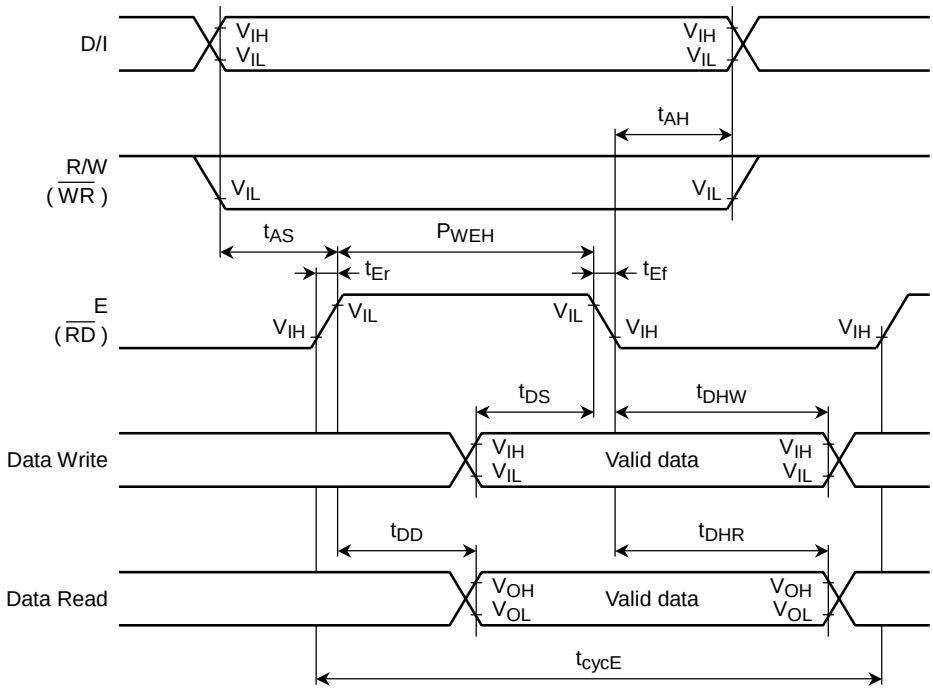
Load Circuit



CL = 100 pF
(including wiring capacitance)

Note 27: When the load circuit shown is added

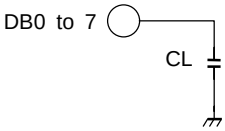
Switching Characteristics (2) (8-bit 68 series MPU interface)



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycE}	500	—	ns
Enable pulse width	P_{WEH}	410	—	
Enable rise/fall time	t_{Er}, t_{Ef}	—	25	
Address setup time	t_{AS}	20	—	
Address hold time	t_{AH}	0	—	
Data setup time	t_{DS}	100	—	
Write data hold time	t_{DHW}	20	—	
Data delay time	t_{DD} (Note 28)	—	300	
Read data hold time	t_{DHR} (Note 28)	20	—	

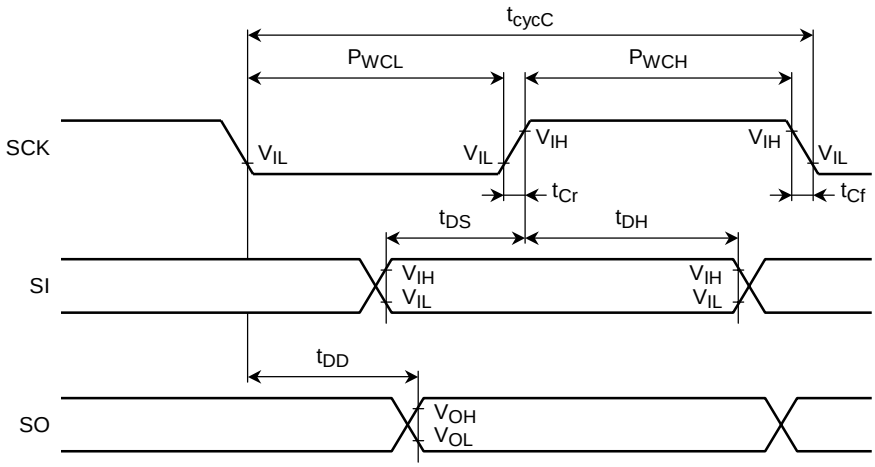
Load Circuit



CL = 100 pF
(including wiring capacitance)

Note 28: When the load circuit shown is added

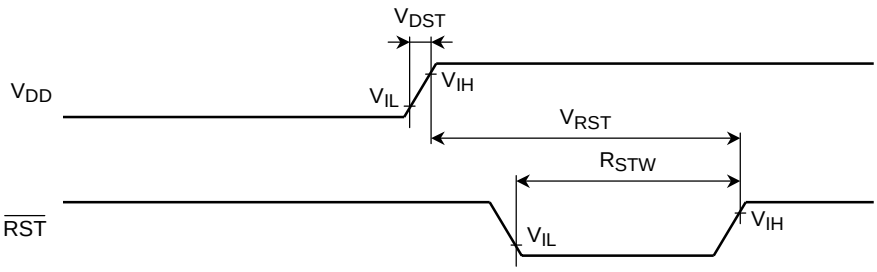
Switching Characteristics (3) (serial interface)



Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics	Symbol	Min	Max	Unit
Enable cycle time	t_{cycC}	2000	—	ns
Enable pulse width	P_{WCL}, P_{WCH}	900	—	
Enable rise/fall time	t_{Cr}, t_{Cf}	—	25	
Data setup time	t_{DS}	250	—	
Data hold time	t_{DH}	100	—	
Data delay time	t_{DD}	—	200	

Switching Characteristics (4)

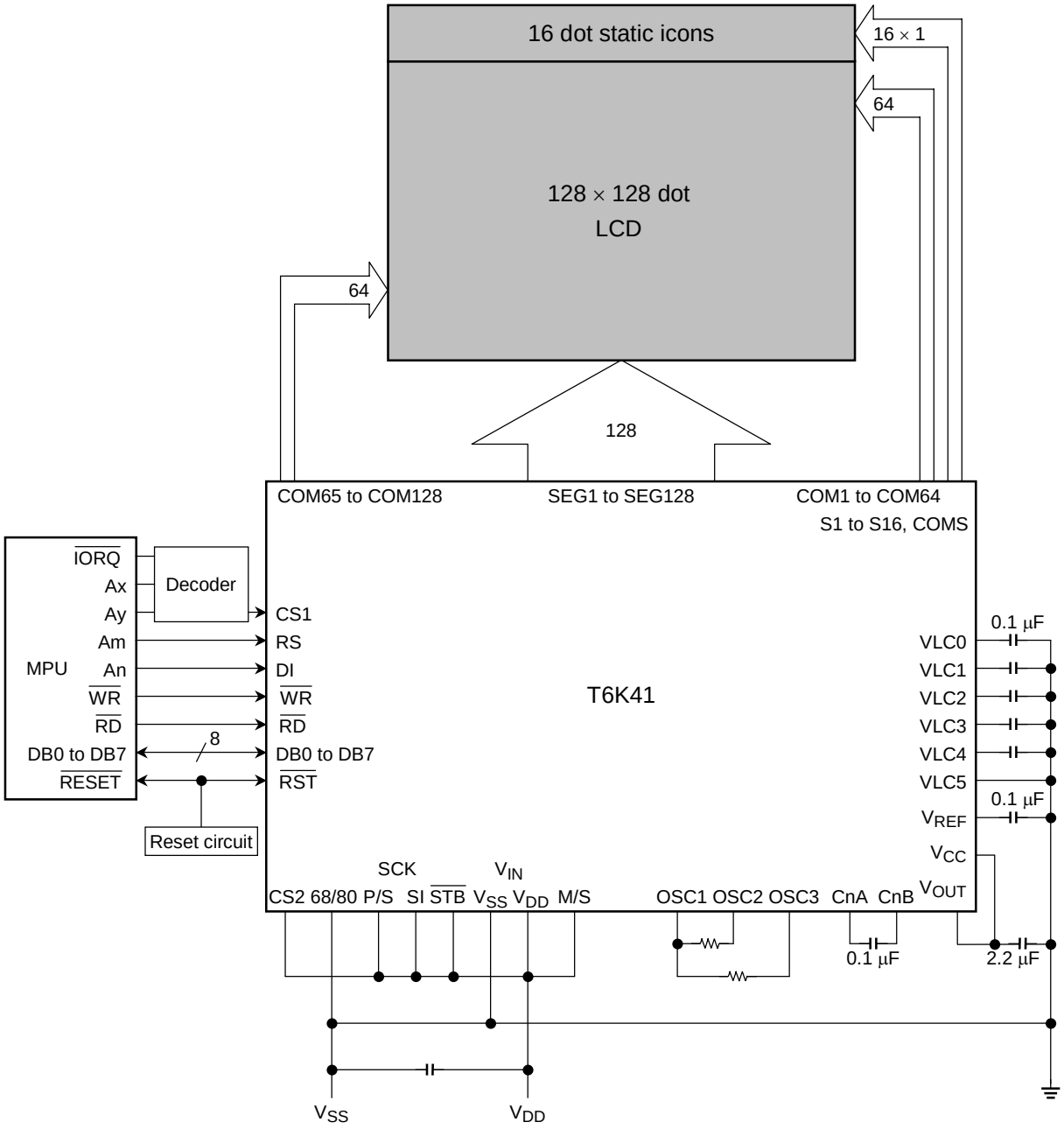


Test Conditions (Unless Otherwise Noted, V_{SS} = 0 V, V_{DD} = 2.7 to 3.3 V, V_{CC} = 15.5 V, Ta = 25°C)

Characteristics	Symbol	Min	Max	Unit
V_{DD} rise time	V_{DST}	—	1	ms
Reset hold	V_{RST}	1	—	μs
Reset pulse width	R_{STW}	1	—	μs

Application Circuit

T6K41 one chip (Master) mode



- V_{DD} = 3.0 V
- Using DC-DC converter (×6)
- Using internal CR oscillator
- Using Op-amp
- 80-series parallel interface

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- Light striking a semiconductor device generates electromotive force due to photoelectric effects. In some cases this can cause the device to malfunction.
  This is especially true for devices in which the surface (back), or side of the chip is exposed. When designing circuits, make sure that devices are protected against incident light from external sources. Exposure to light both during regular operation and during inspection must be taken into account.
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