PM7018 RPFEC

ERROR CORRECTION CIRCUIT

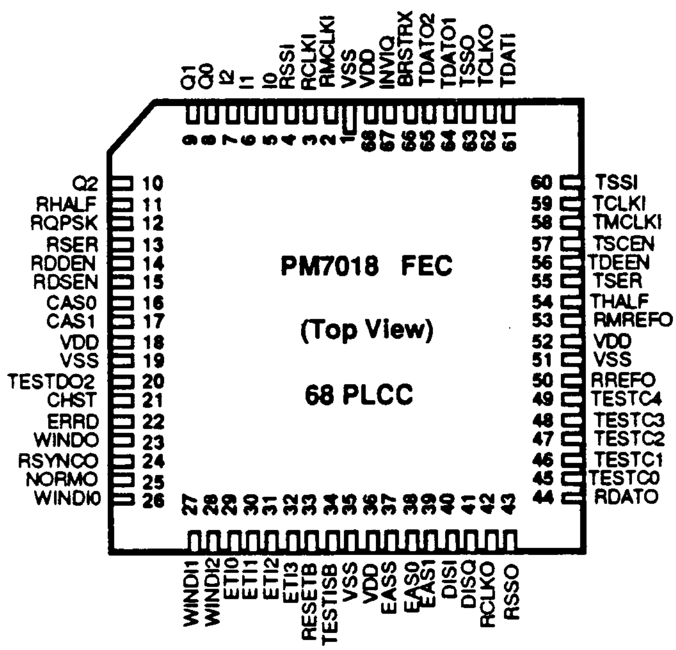
DATA SHEET

FEATURES

- Constraint length 7 convolutional encoder (polynomials 133,171)
- Viterbi decoder with up to 3 bit soft decision inputs and an 80 stage trellis
- Two versions for operation at the following information data rates:

  Up to 256 Kbit/sec PM7018-256
  Up to 2.5 Mbit/sec PM7018-2500
- Independent encoder and decoder operation
- Operation at code rates 1/2 and 3/4 with no additional components required
- Optional external dummy bit insertion for operation at other code rates
- Code rate 1/2 and 3/4 coding gain within 0.2 dB of theory (3 bit soft decision decoding with an infinite trellis length)
- Excellent performance for code rates up to 7/8
- Encoder and decoder valid data synchronization inputs and outputs for burst mode operation
- Automatic phase, symbol and rate 3/4 puncturing ambiguity resolution for BPSK, QPSK,and OQPSK modems with programmable parameters
- Optional external selection of ambiguity state
- Intelsat Earth Station Standards IESS-308, IESS-309 compatible
- Optional selection of CCITT V.35 scrambling/descrambling
- Optional selection of differential encoding/decoding
- Operating Status outputs
- System test and fault isolation inputs with loopback and tristate output control
- LSTTL compatible inputs and outputs
- Power supply: +5 volt
- Standard package: 68 pin PLCC

PIN DIAGRAM



DESCRIPTION

The PM7018 is a single chip forward error correction circuit that can provide more than 5 dB of coding gain for information rates up to 2.5 Mbit/s. It is suitable for modem or digital error correction systems where data bandwidth expansion is possible.

APPLICATIONS

- Satellite Communications
- Mobile Communications
- ISDN and other Digital Network applications

FUNCTIONAL DESCRIPTION

The FEC device contains a constraint length 7 convolutional encoder and a corresponding Viterbi decoder. The two sections are independent and separately configurable in a number of different operating modes.

The encoder accepts an input data stream in either continuous or burst data mode at data rates of up to 2.5 Mbit/s.

The encoder offers optional CCITT V.35 scrambling and differential encoding to be applied to the incoming data prior to the convolutional encoding. The generated code symbol pairs may output sequentially for input to a BPSK modulator or simultaneously for input to a QPSK modulator.

Code puncturing to rate 3/4 may be selected with BPSK or QPSK output.

The decoder accepts 3 bit soft decision code symbols from a BPSK demodulator or two 3 bit soft decision inputs from a QPSK or OQPSK demodulator in continuous or burst data mode.at either rate 1/2 or rate 3/4. The decoder offers optional differential decoder and CCITT V.35 descrambling to be applied after Viterbi decoding.

The options for scrambling and differential encoding are dynamically selectable and can be enabled and disabled during data transmission without introducing data errors. The encoding and decoding delays are not changed by any of the optional configuration selections.

The device was designed for ease of use with burst data modems by allowing multiple bursts to be resident in the trellis and by providing internal or external ambiguity state selection.

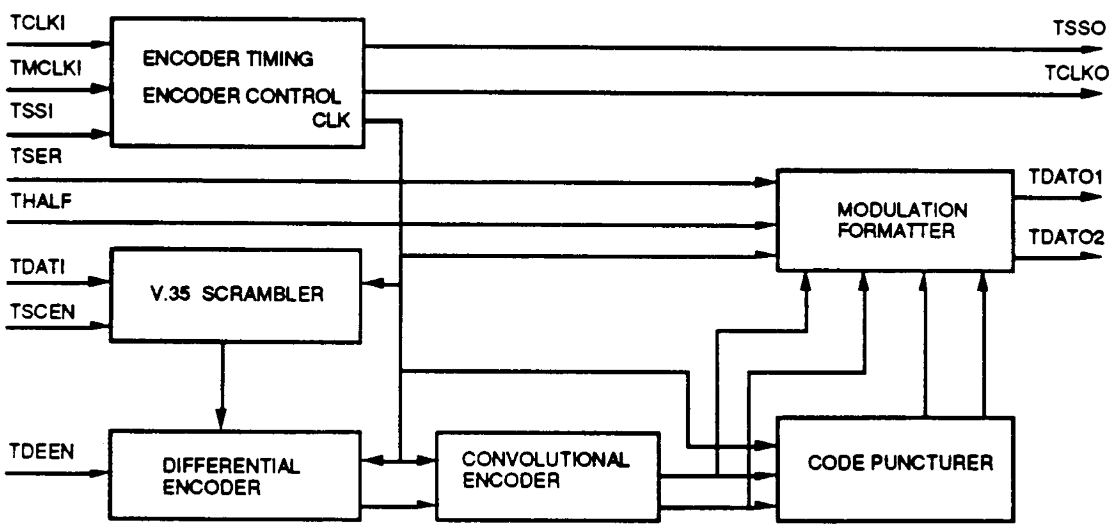
Continuous clock outputs and synchronized valid data outputs are provided for the encoded and decoded data.

A wide range of options for error threshold and integration window size allows tailoring the internal ambiguity state resolver to the application.

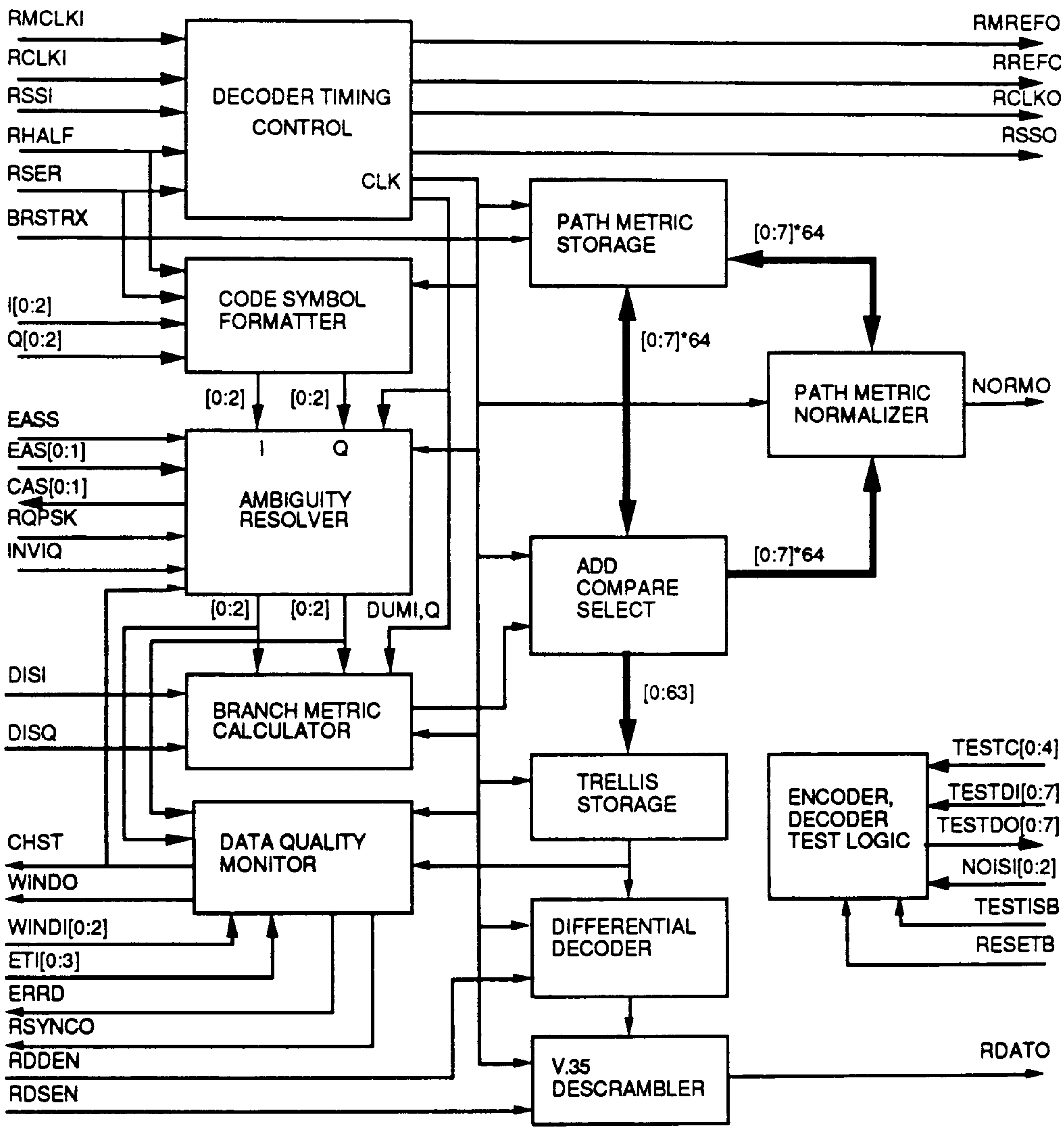
Status outputs are provided for channel error detection, current ambiguity state, change of ambiguity state, encoder/decoder ambiguity state synchronization and path metric normalization.

The device provides user test control options including loopback from encoder to decoder and decoder to encoder for system testing. A self test option allows an internally generated pseudo-random data pattern to be input to the encoder, looped back to the decoder and the resulting decoded data pattern validated. Another test option tristates all of the outputs.

ENCODER BLOCK DIAGRAM



DECODER BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The PM 7018 RPFEC circuit consists of a constraint length 7 Convolutional Encoder with a corresponding Viterbi decoder within a single integrated circuit. The encoder and decoder are separate blocks and are capable of running completely independent of each other. The circuit does allow internal loopback tests from encoder to decoder and contains internal test functions.

Encoder Description

The encoder takes the input data and clock, scrambles and differentially encodes the data (selected by the setting of TSCEN and TDEEN) and passes it to the convolutional encoder. The outputs from the convolutional encoder are processed in the code puncturer and modulation formatter to produce rate 1/2 or rate 3/4 signals in either parallel or serial format.

Timing and Control

The encoder timing and control takes TMCLKI and divides it down for the appropriate mode of transmission. TMCLKI is 8 times the encoder input data clock. The divide ratios are 4, 6, 8 and 12 which correspond to transmission modes of rate 1/2 BPSK, rate 3/4 BPSK, rate 1/2 QPSK and rate 3/4 QPSK. The transmit stop/start (TSSO) is also controlled from this block.

V.35 Scrambler and Differential Encoder

The V.35 scrambler scrambles the data to the V.35 standard. It involves a tapped 20 stage shift register and an adverse state detector which counts to 32 before affecting the output data. The differential encoder causes the output data to stay the same as its current value if the next bit is 0 and to change if the next bit is 1. Both operations can be selectively enabled.

Convolutional Encoder

The convolutional encoder is is constraint length 7 with generator polynomials of 133 and 171. The output is a rate 1/2 parallel bit stream which could be used directly for QPSK/OQPSK modulation.

Code Puncturer and Modulation Formatter

The code puncturer and modulation formatter take the two outputs of the convolutional encoder and convert them into the four possible outputs; rate 1/2 QPSK or BPSK and rate 3/4 QPSK or BPSK.

Decoder Description

The decoder takes any format of output from the encoder plus some errors and decodes it back to the original encoder input data. To do this the decoder undoes each of the coding functions applied in the encoder.

Timing and Control

The decoder timing and control takes RMCLKI and divides it down for the appropriate mode of transmission. RMCLKI is 8 times the decoder output clock. The ratio between RMCLKI and RCLKI depends on the mode of transmission. The relationships are:

Rate 1/2 parallel:

RCLKI=RMCLKI/8=RCLKO

Rate 1/2 serial:

RCLKI=RMCLKI/4=RCLKO

Rate 3/4 parallel:

RCLKI=RMCLKI/12=2/3 times RCLKO

Rate 1/2 parallel:

RCLKI=RMCLKI/6=4/3 times RCLKO

The receive stop/start (RSSO) is also controlled from this block. Reference outputs RMREFO and RREFO provide a comparison input to the PLL which generates RMCLKI.

Code Symbol Fomatter

The code symbol formatter takes in the 3 bit wide code symbols and reformats them as required. If the symbols are parallel, they are simply delayed by one clock period. If the symbols are serial, they are reformatted to parallel form.

Ambiguity Resolver

The ambiguity resolver corrects for ambiguity in the orientation and relative position of the code symbol pairs caused by BPSK, QPSK or OQPSK demodulation and puncturing. The corrections can be selected by external inputs or the ambiguity can be allowed to resolve automatically.

Branch Metric Calculator

The branch metric calculator generates noiseless three bit versions of the four possible combinations of the code symbol pairs and compares them to the three bit code symbol pairs. From this comparison, the four bit branch metrics are generated. Internal puncturing for rate 3/4 codes is provided for along with provision for insertion of bits for code rates other than 1/2 or 3/4.

Path Metric Storage

The path metric storage is a two stage, 8 x 8 bit register array. There are 3 independent data paths that permit writing to one memory location while reading from two independent sources. Each storage element forms a master/slave configuration, allowing the write operations to occur simultaneously with the read operations performed on the old data.

Add Compare Select

The add compare select combines two branch metrics with two path metrics from the path metric storage via the path metric normalizer. It outputs a new path metric for each trellis state. The constraint length 7 Viterbi decoder requires 64 path metrics be processed for each incoming data bit.

Path Metric Normalizer

The path metric normalizer examines the most significant bit of each of the 64 metrics for one bit time period. If the most significant bits are all logic one (ie. greater than 127), the path metric normalizer will subtract 128 from all, by forcing the most significant bit of all 64 path metrics to logic low during the next bit time.

Trellis Storage

The trellis storage is 64 bit by 80 stage array. Constraint length 7 Viterbi decoding requires 64 path metrics and 80 stages are required to accomplish decoding up to rate 7/8.

Data Quality Monitor

The data quality monitor is used for internal resolution of demodulation ambiguities. It takes the most significant bits of the 3 bit I and Q code symbols input to the Viterbi decoder and compares them to a re-encoded output of the Viterbi decoder with the proper delay inserted. The window to count errors in the data is selectable from 256 to 32786 RCLKO periods. Once a fraction of this window is counted to be errors (fractions selectable from 1/8 to 19/32 in 1/32 steps), the window is cleared, the ambiguity state is changed and a high is output on the CHST pin. Each error that occurs causes a pulse to be output on the ERRD pin.

Differential Decoder and V.35 Descrambler

The differential decoder undoes the function performed by a differential encoder. Similarly the V.35 Descrambler undoes the scrambling performed by a V.35 Scrambler. Both operations can be selectively inhibited.

Encoder and Decoder Test Logic

The encoder and decoder test logic contains the following internal test functions: encoder to decoder loopback, decoder to encoder loopback, selftest, output high impedance, scrambling and differential encoding tests and a boundary scan.

PIN DESCRIPTION

The following tables describe the function of each pin on the PM7018. Some input pins have internal pull-up resistors programming the device to default to continuous, RATE 1/2, and QPSK operation with differential encoding/decoding and scrambling/descrambling enabled.

Connector Name	Type	Pin Number	Pull UP/Down	Function

Encoder Clock, Data and Configuration Inputs

TMCLKI	Input	58		Transmit Master Clock Input: This clock runs at eight times the information (uncoded) data rate.
TCLKI	Input	59		Transmit Clock Input: This clock runs at the information (uncoded) data rate. Transitions of this clock should occur on the rising edge of TMCLKI.
TSSI	Input	60	PU	Transmit Start/Stop Input: A high on this input indicates the input of the valid data to the FEC encoder. A low forces the input of zeros into the convolutional encoder input and initializes the differential encoder and scrambler circuits. Transitions should occur on rising TCLKI edges.
TDATI	Input	61		Transmit Data Input: Data to be encoded is input on this line. The input data is valid whenever TSSI is high. Transitions should occur on rising TCLKI edges.
TSCEN	Input	57	PU	Transmit Scrambler Enable: The V.35 scrambler is enabled whenever this input is high. The scrambler remains initialized whenever TSSI is low. Transitions should occur on rising TCLKI edges and will affect the data bit input on the next rising edge. In self test and loopback #1 test modes, the input becomes noise test input NOISI2, and RDSEN determines scrambler enable status.
TDEEN	Input	56	PU	Transmit Differential Encoder Enable: The differential encoder is enabled whenever this input is high. The differential encoder remains initialized whenever TSSI is low. Transitions should occur on rising TCLKI edges and will affect the data bit input on the next rising edge. In self test and loopback #1 test modes, the input becomes noise test input NOISI1, and RDDEN determines encoder enable status.

TSER	Input	55	PD	Transmit Serial Format Enable: The encoder output format will be serial whenever this input is high. The output format will be parallel whenever the input is low. In self test and loopback #1 test modes, the input becomes noise test input NOISI0, and RSER determines the format.
THALF	Input	54	PU	Transmit Code Rate 1/2: The rate 1/2 convolutional code will be selected whenever this is high. The rate 3/4 code will be selected whenever this input is low. In self test and loopback #1 test modes, RHALF determines thecode rate.

Encoder Clock and Data Outputs

TCLKO	Output	62		Transmit Clock Output: This clock runs at the transmission clock rate determined by inputs TSER and THALF. Transitions occur on the falling edge of TMCLKI.
TSSO	Output	63		Transmit Start/Stop Output: This output goes high when the first valid code bits are available from the FEC encoder after TSSI goes high and remains high until all valid data has been output. Transitions occur on rising TCLKO edges.
TDATO1	Output	64		Transmit Data Output Bit 1: The code symbols g1 and g2 are alternately output on this line in serial mode and g1 is output on this line in parallel mode. Transitions occur on rising TCLKO edges.
TDATO2	Output	65		Transmit Data Output Bit 2: The code symbol g2 is output on this line in parallel mode. Transitions occur on rising TCLKO edges.

Decoder Clock and Data Inputs

RMCLKI	Input	2		Receive Master Clock Input: This clock runs at eight times the information data rate.
RCLKI	Input	3		Receive Clock Input: This clock runs at the received I channel symbol rate. In parallel (QPSK-OQPSK) format and rate 1/2 coding, the clock runs at the information (uncoded) data rate. When the code symbols are received in serial (BPSK) format and rate 1/2 coding the clock runs at twice the information data rate. For parallel format and rate 3/4 coding, the clock runs at 2/3 the information rate. For serial format and rate 3/4 coding, the clock runs at 4/3 the information rate. Transitions on this clock should be concurrent with the rising edge of RMCLKI.

RSSI	Input	4	PU	Receive Start/Stop Input: A high on this input indicates the presence of valid code symbols at the Decoder input. A low on this input will stop the decoding process by initializing path metrics and forcing the received data bit to 0. Transitions should occur on rising RCLKI edges.
I0,I1,I2	Input	5,6,7		I Code Symbol Input Bus: When the code symbols are received in parallel (QPSK-OQPSK) format, the I code symbols are input on this bus. I2 is the most significant bit. When the code symbols are received in serial (BPSK) format, both the I and Q code symbols are alternately input on this bus. The input format is offset binary: 111 is the most reliable 1 100 is the least reliable 1 011 is the least reliable 0 000 is the most reliable 0 Transitions should occur on rising RCLKI edges. In certain test modes the inputs become test data inputs.
Q0,Q1,Q2	Input	8,9,10		Q Code Symbol Input Bus: When the code symbols are received in parallel (QPSK-OQPSK) format, the Q code symbols are input on this bus. Q2 is the most significant bit. When the code symbols are received in serial (BPSK) format, this bus is not used. Transitions should occur on rising RCLKI edges. In certain test modes the inputs become test data inputs.

Decoder Configuration Inputs

RSER	Input	13	PD	Receive Serial Format: The decoder input format is serial whenever this input is high. The input format is parallel whenever the input is low.
RHALF	Input	11	PU	Receive Code Rate 1/2: The rate 1/2 decoder is enabled whenever this input is high. The dummy bit insertion logic for decoding rate 3/4 code symbols is enabled whenever this input is low. In certain test modes the input becomes a test data input.

RQPSK	Input	12	PU	Receive QPSK Format: This input, in conjunction with RSER and RHALF, determines the valid ambiguity states for the ambiguity resolver. For QPSK modulation (ie. RSER low) this input should be high. For OQPSK modulation (ie. RSER low) or for BPSK modulation (ie. RSER In certain test modes this input becomes a test data input.
RDSEN	Input	15	PU	Receive Descrambler Enable: The V.35 descrambler is enabled whenever this input is high. The descrambler is initialized whenever RSSO is low. Transitions should occur on rising RCLKO edges.
RDDEN	Input	14	PU	Receive Differential Decoder Enable: The differential decoder is enabled whenever this input is high. The decoder is initialized whenever RSSO is low. Transitions should occur on rising RCLKO edges.

Decoder Ambiguity Resolution Performance Inputs

EASS	Input	37	PD	External Ambiguity State Select: A high on this line forces the ambiguity resolver to select the ambiguity state provided on the external ambiguity state inputs EAS0 and EAS1 and disables the internal ambiguity resolver.
EAS0,EAS1	Input	38,39	PD	External Ambiguity State Inputs: The external ambiguity state is selected on these two lines. EAS0 determines QPSK 0, 90 degree phase rotation symbol or BPSK pair framing. EAS1 determines rate 3/4 puncture framing.
INVIQ	Input	67	PD	Invert I and Q: This line is used for external ambiguity state selection when differential decoding is not enabled (RDDEN is low). The signal determines 0, 180 degree phase rotation.
WINDI0,1,2	Input	26,27,28	PD	Error Window Size Select: These three lines determine the number of information bits to be examined by the data quality monitor to detect unresolved modem ambiguities. The bits represent the power of two from 0 to 7 that 256 bits are multiplied by to determine window size. The window size range is from 256 to 32768 bits.
ETI0,1,2,3	Input	29,30,31,32	PU	Error Threshold Select: These four lines determine the error threshold used by the data quality monitor to detect unresolved modem ambiguities. The inputs select a fraction which is the ratio of detected errors in a window to the number of bits in the window. The ratio ranges from 1/8 to 19/32 in 1/32 increments. In certain test modes, the inputs are used to specify portions of a logic block to be tested.

Decoder Clock and Data Outputs

RCLKO	Output	42		Receive Clock Output: This clock signal runs at the information (uncoded) data rate. Transitions are concurrent with the falling edge of RMCLKI.
RSSO	Output	43		Receive Start/Stop Output: A high on this output indicates valid decoded data bits from the decoder. Transitions occur on rising RCLKO edges.
RDATO	Output	44		Received Data Output: The decoded data from the FEC decoder via the differential decoder and/or descrambler if selected is output on this line. Transitions occur on rising RCLKO edges.
RMREFO	Output	53		Receive Master Reference Output: This clock signal is RMCLKI divided by 24, and can be used to provide a phase reference for a VCO for generating RMCLKI.
RREFO	Output	50		Receive Reference Output: This clock signal will be RCLKI divided by 2,3,4 or 6 depending on the modulation format and coding rate specified by RSER and RHALF respectively. The output can be used as the other phase reference for a VCO for generating RMCLKI.

Decoder Status Outputs

CAS0,CAS1	Output	16,17		Current Ambiguity State: The current ambiguity state used by the ambiguity resolver is output on these two lines. If EASS is High: CAS0 reflects EAS0 and CAS1 reflects EAS1. In test modes the outputs will be test outputs.
CHST	Output	21		Change Ambiguity State: A high pulse on this output will indicate that the number of errors detected by the data quality monitor has exceeded the error threshold. In test modes, the output is a test output.
ERRD	Output	22		Channel Error Detected: A high pulse on this output indicates the detection of a transmission error. In test modes, the output is a test output.
WINDO	Output	23		End of Window: A pulse on this output indicates that the error monitoring window is being reset. The window size is determined by WINDI[0:2]. Transitions will occur on rising RCLKO edges. In test modes, the output is a test output.

RSYNCO	Output	24		Decoder Synchronized: A low on this output will indicate that the data quality monitor has detected errors in excess of the error threshold, and that a WINDO pulse has not subsequently occurred. A high indicates that the FEC decoder is synchronized and RSSI is high. In some test modes a high pulse on this output indicates a decoding error, otherwise it is a test output.
NORMO	Output	25		Path Metric Normalization: A one information bit wide pulse is output on this pin every time the path metrics are normalized in normal operation. Transitions occur on rising RCLKO edges. In self test mode, an internally generated pseudo-random data sequence is output on this line with transitions occurring on rising TCLK edges.
TESTDO2	Output	20		Test Data Output: This pin is a test data output.

Decoder Special Functions

DISI	Input	40	PD	Disregard I Code Symbol: This input allows the Viterbi decoder to be used at code rates other than 1/2 or 3/4 or to be concatenated with another FEC device. A high on DISI instructs the decoder to disregard the I code symbol currently being processed. Transition should occur on rising RCLKO edges. The code rate should be 1/2 when using this input.
DISQ	Input	41	PD	Disregard Q Code Symbol: This input allows the Viterbi decoder to be used at code rates other than 1/2 or 3/4 or to be concatenated with another FEC. A high on DISQ instructs the decoder to disregard the Q code symbol currently being processed. Transition should occur on rising RCLKO edges. The code rate should be 1/2 when using this input.
BRSTRX	Input	66	PD	Burst Reception Biased Path Metrics: This input is used in conjunction with a burst demodulator using unique word detection. When this input is low, the path metrics of all states in the trellis are initialized to zero when RSSI goes low. When the input is high, the path metrics of all states but 000000 and 111111 are initialized to a high value and states 000000 and 111111 are initialized to zero. This improves the reliability of the first data bits received in a burst, assuming the first valid data bit is known.

Test Inputs

TESTC[0:4]	Input	45,46,47,48,49	PU	Test Control Inputs: These test inputs control the test modes of the device.
TESTISB	Input	34	PU	Test Input Select Bar: This input is used to control device test.
RESETB	Input	33	PU	Reset Bar: A low on this asynchronous input forces critical registers in the device to a known state for testing purposes.

Power

V_{DD}		18,36,52,68		+5 V
V_{SS}		1,19,35,51		Ground

INTERNAL TEST DESCRIPTION

The test table describes internal test functions of the PM7018 available to the user. Other test functions are available, but are generally used for production testing. Consult the factory for further information. To facilitate testing, the following pins have different functions when the circuit is being tested internally:

Test Pin Description

Pin	Operational Designation	Test Designation	Test Function
12	RQPSK	TESTDI[7]	Part of parallel test input bus
11	RHALF	TESTDI[6]	Part of parallel test input bus
10	Q[2]	TESTDI[5]	Part of parallel test input bus
9	Q[1]	TESTDI[4]	Part of parallel test input bus
8	Q[0]	TESTDI[3]	Part of parallel test input bus
7	I[2]	TESTDI[2]	Part of parallel test input bus
6	I[1]	TESTDI[1]	Part of parallel test input bus
5	I[0]	TESTDI[0]	Part of parallel test input bus
25	NORMO	TESTDO[7]	Part of parallel test output bus
24	RSYNCO	TESTDO[6]	Part of parallel test output bus
23	WINDO	TESTDO[5]	Part of parallel test output bus
22	ERRD	TESTDO[4]	Part of parallel test output bus
21	CHST	TESTDO[3]	Part of parallel test output bus

20	TESTDO2	TESTDO[2]	Part of parallel test output bus
17	CAS[1]	TESTDO[1]	Part of parallel test output bus
16	CAS[0]	TESTDO[0]	Part of parallel test output bus
57	TSCEN	NOISI[2]	Part of digital noise input bus
56	TDEEN	NOISI[1]	Part of digital noise input bus
55	TSER	NOISI[0]	Part of digital noise input bus

Test Table

Test C Inputs 43210	Description
11111	NORMAL OPERATION: No test modes are in effect.
11110	LOOPBACK #1: Complete loopback from encoder to decoder. The code symbol formatter will replace its normal inputs RSSI, I, Q and RCLKI with the encoder outputs TSSO, TDATO1, TDATO2 and TCLKO respectively. A digital noise sequence may be input on the NOISI[0-2] inputs. A decoding error will be indicated by a pulse on TESTDO6. Options selected for scrambling, differential coding, modulation format and coding rate for both the encoder and decoder will be determined using the decoder select inputs.
11101	SELF TEST MODE: The encoder maintenance control unit will instruct the encoder to disregard the data input on TDATI and encode the internally generated pseudo-random data sequence. This data will be available on test output TESTDO7. The code symbol formatter will replace its normal inputs RSSI, I, Q and RCLKI with the encoder outputs TSSO, TDATO2 and TCLKO respectively. A digital noise sequence may be input on the NOISI[0-2] inputs. Options selected for scrambling, differential coding, modulation format and coding rate for both the encoder and decoder will be determined using the decoder select inputs.
11011	LOOPBACK #2: Complete loopback from decoder to encoder. The encoder will replace its normal inputs TSSI, TDATI and TCLKI with the decoder outputs RSSO, RDATO and RCLKO respectively. Options selected for scrambling, differential coding, modulation format and coding rate for both the encoder and decoder will be determined using the decoder select inputs.
10111	HIGH IMPEDANCE OUTPUTS: The maintenance control unit will place the following outputs in a high impedance state: TCLKO, TSSO, TDATO1, TDATO2, RMREFO, RREF, RCLKO, RSSO, RDATO, and TESTDO[0-7].
10110	SCRAMBLING, DIFFERENTIAL ENCODING TEST#1: The encoder scrambler and differential encoder logic will be directly connected to the decoder differential decoder and descrambler. The by-pass logic will function normally. In this test mode, the adverse state logic from the scrambler and descrambler will be disconnected and the input to the scrambler shift register will be TDATI directly. The scrambler output, the differential decoder output and the scrambler and descrambler adverse state counter outputs will appear on the TESTDO bus.

10101	SCRAMBLING, DIFFERENTIAL ENCODING TEST#2: The encoder scrambler and differential encoder logic will be directly connected to the decoder differential decoder and descrambler. In this test mode, the by-pass logic and the scrambler and descrambler will operate normally. The scrambler output, the differential decoder output and the scrambler and descrambler adverse state counter outputs will appear on the TESTDO bus.
01111	BOUNDARY SCAN: The maintenance control unit will connect the following outputs directly to the following inputs as stated below: RCLKI to RCLKO TCLKI to TCLKO TDATI to TDATO1 and TDATO2 RSSI to RSSO RMCLKI to RMREFO TMCLKI to RREFO TSSI to TSSO RQPSK to NORMO RHALF to RSYNCO Q[2] to WINDO Q[1] to ERRD Q[0] to CHST I[2] to TESTDO[2] I[1] to CAS[1] I[0] to CAS[2] Parity of DISI and DISQ to RDATO

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +125°C
Supply Voltage to Ground Potential	-0.5 V to +6.0 V
Applied Input Voltage	-0.5 V to V_{DD} + 0.5V

Stresses above those listed may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS T_A = 0°C to +70°C, V_{DD} = 5 V ±5%

Note: *Inputs = V_{SS} or V_{DD}, outputs are unloaded*

Symbol	Parameter	Min	Max	Units	Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	Volts	
V_{IH}	Input High Voltage	2.0	V_{DD}	Volts	
I_I	Input Current	-10	10	µA	V_I = V_{DD} or GND without PU/PD
I_I	Input Current	25	120	µA	V_I = GND with PU
I_I	Input Current	35	145	µA	V_I = V_{DD} with PD
I_{DD}	Power Supply Current		130	mA	TMCLKI, RMCLKI @ 20 MHz
I_{DD}	Power Supply Current		12	mA	TMCLKI, RMCLKI @ 24 kHz
V_{OL}	Output Low Voltage		0.05	Volts	I_{OL} = 1 µA
V_{OH}	Output High Voltage	V_{DD} - 0.05		Volts	I_{OH} = -1 µA
I_{OL}	Output Low Current	2.0		mA	V_{OL} = 0.4 V
I_{OH}	Output High Current	-2.0		mA	V_{OH} = 2.4 V
I_{OZ}	High Impedance Output Leakage Current	-10.0	10.0	µA	V_O = V_{DD} or GND
C_{in}	Input Capacitance		10	pF	V_O = V_{DD}
C_{out}	Output Capacitance		20	pF	V_O = V_{DD}

AC CHARACTERISTICS T_A = 0°C to +70°C, V_{DD} = 5 V ±5%

Parameter	PM7018-256		PM7018-2500		Units	Conditions
	Min	Max	Min	Max		
Information Data Rate Range	3 k	256 k	3 k	2.5 M	bit/s	Uncoded data (See also Note 1)
TMCLKI Frequency Range	24 k	2048 k	24 k	20 M	Hz	8 times Information Data Rate
TCLKI Frequency Range	3 k	256 k	3 k	2.5 M	Hz	
BPSK RCLKI Frequency Range	4 k	512k	4 k	5 M	Hz	Min. Rate 3/4 and Max. Rate 1/2
QPSK-OQPSK Frequency Range	2 k	256 k	2 k	2.5 M	Hz	Min. Rate 3/4 and Max. Rate 1/2
RMCLKI Frequency Range	24 k	2048 k	24 k	20 M	Hz	8 times Information Data Rate
Worst case input clock duty cycle RCLKI/TCLKI	25	75	25	75	%	BPSK @ Rate 1/2
Worst case input clock duty cycle RMCLKI/TMCLKI	40	60	40	60	%	@ 20 MHz
Output 10%-90% rise/fall times		60		60	ns	50 pF load
Peak clock jitter on RCLKI, with respect to RMCLKI						
QPSK, Rate 3/4	-4	+4	-4	+4	%	Percentage of period subject to meeting set-up time requirements (See also Note 2)
QPSK, Rate 1/2	-6	+6	-6	+6		
BPSK, Rate 3/4	-8	+8	-8	+8		
BPSK, Rate 1/2	-12	+12	-12	+12		

Notes: 1. The minimum information rate is determined by the capacitive storage time on some dynamic memory cells.
2. RCLKI is sampled on the falling edge of RMCLKI

TIMING DIAGRAMS

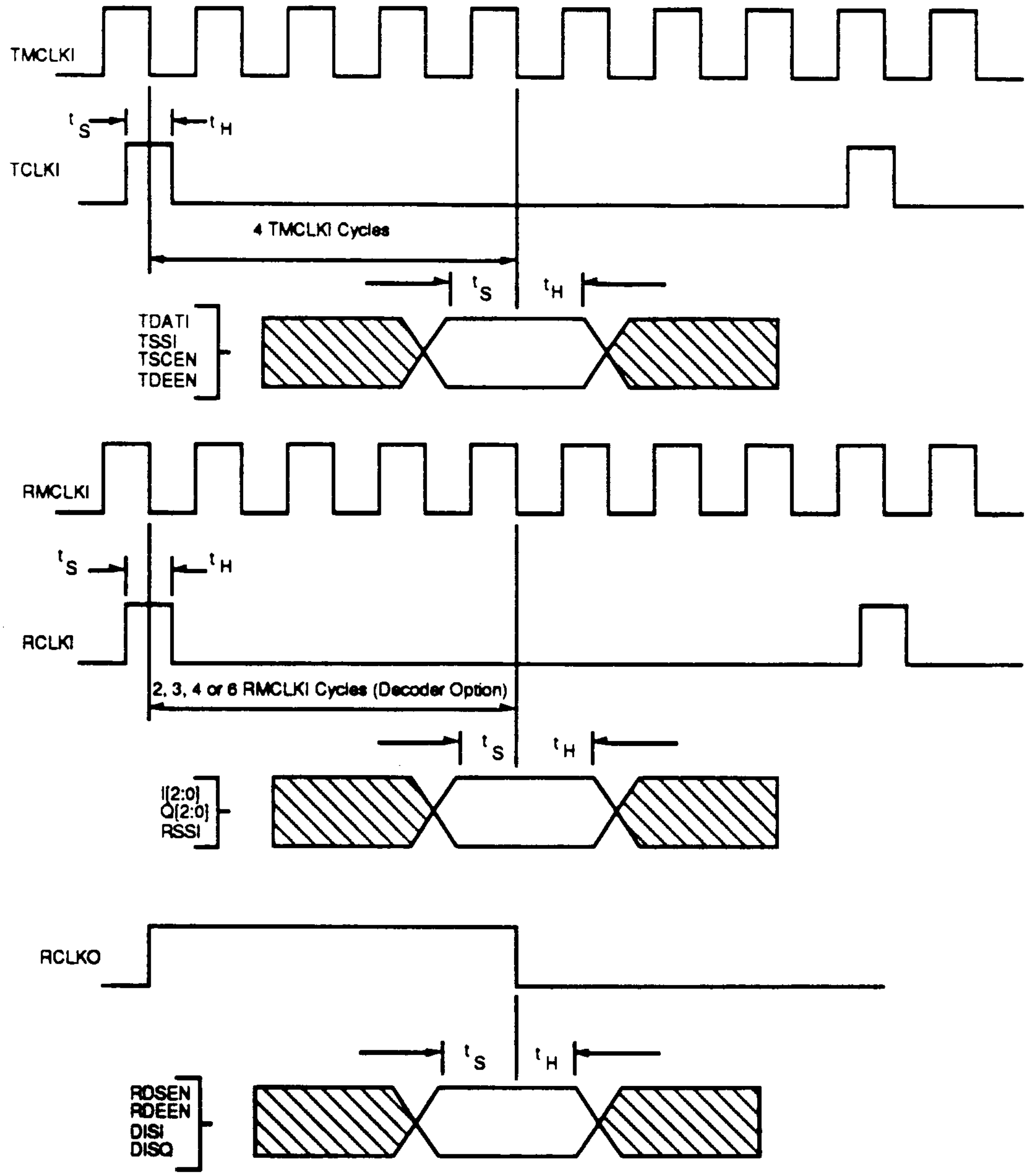


Fig. 1 Set-up and Hold Times

Notes:

1. Decoder inputs are sampled on falling edge of RMCLKI, including RCLKI.
2. Decoder outputs are sampled on falling edge of RMCLKI, including RCLKO.
3. Encoder inputs are sampled on falling edge of TMCLKI.
4. Encoder outputs are sampled on falling edge of TMCLKI.
5. TCLKI and RCLKI are expected to be a nominal 50% duty cycle
6. Inputs are sampled on the falling edge of TMCLKI (RMCLKI) which is in the middle of a bit period.

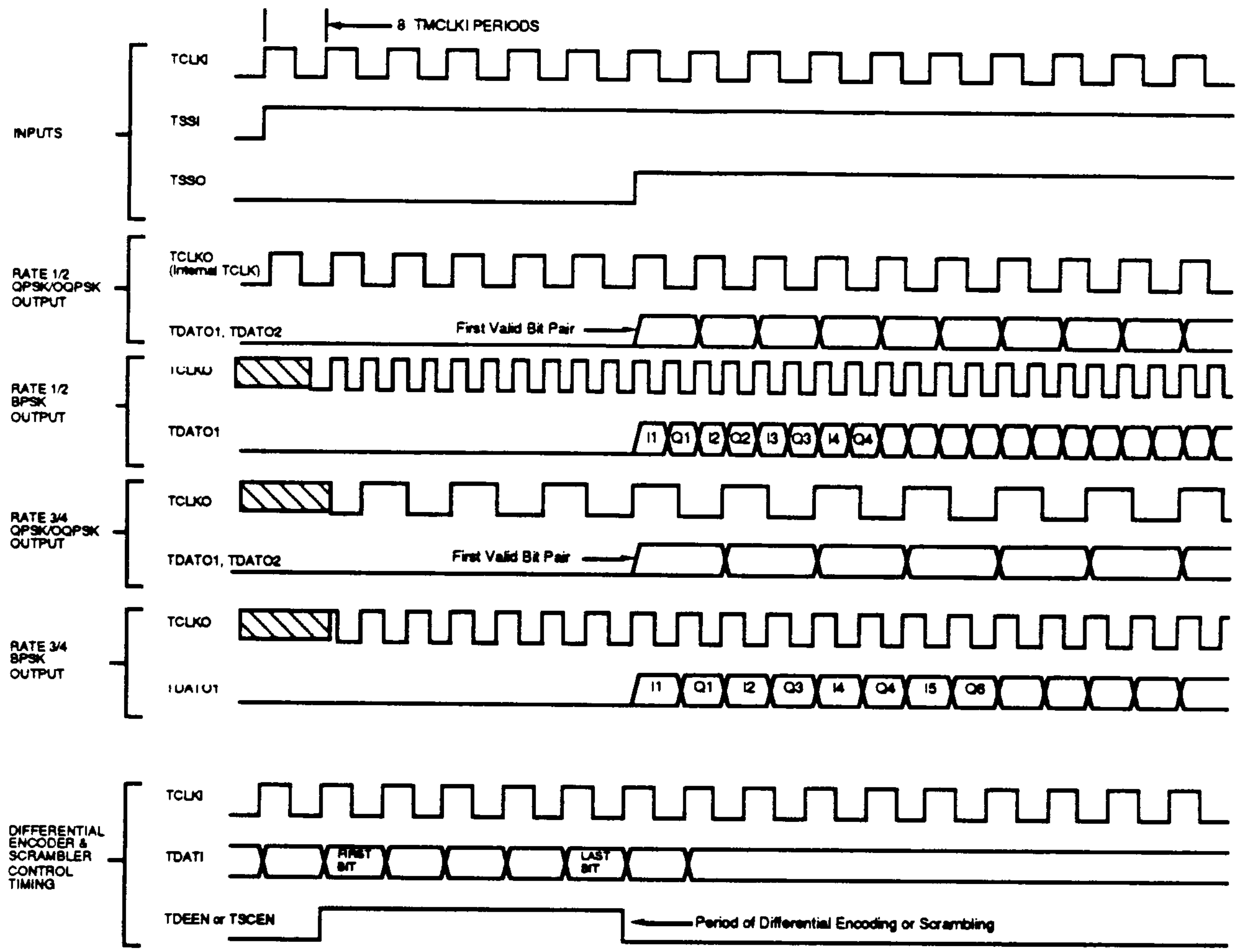
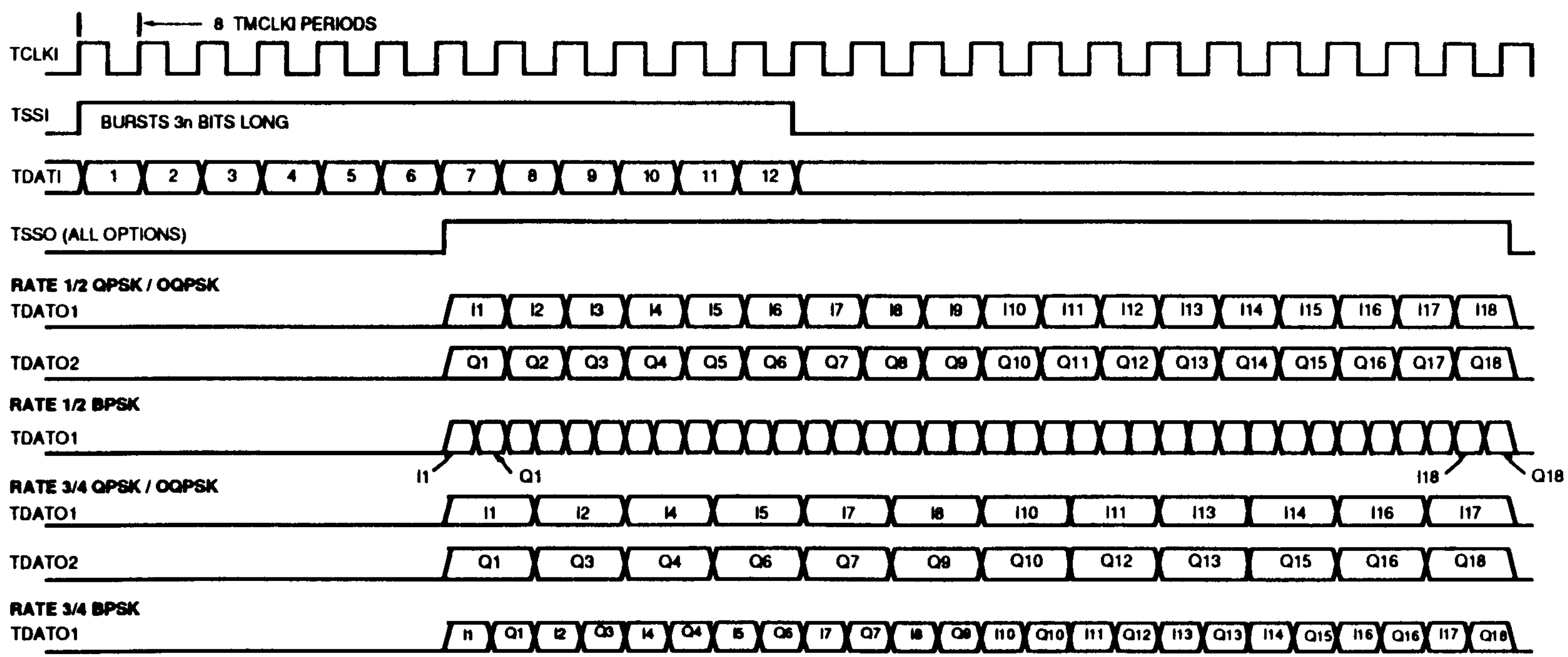
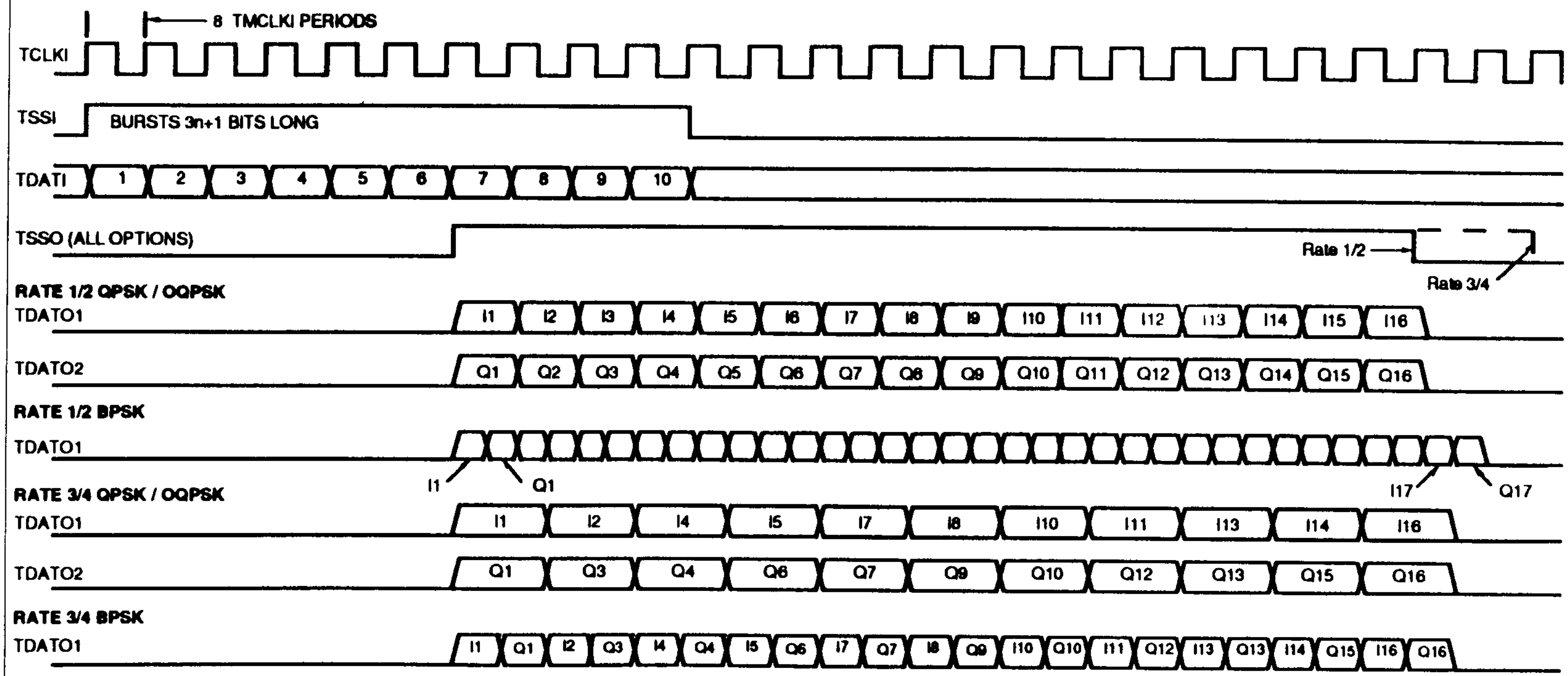


Fig. 2 Encoder Continuous Operation Timing Diagram



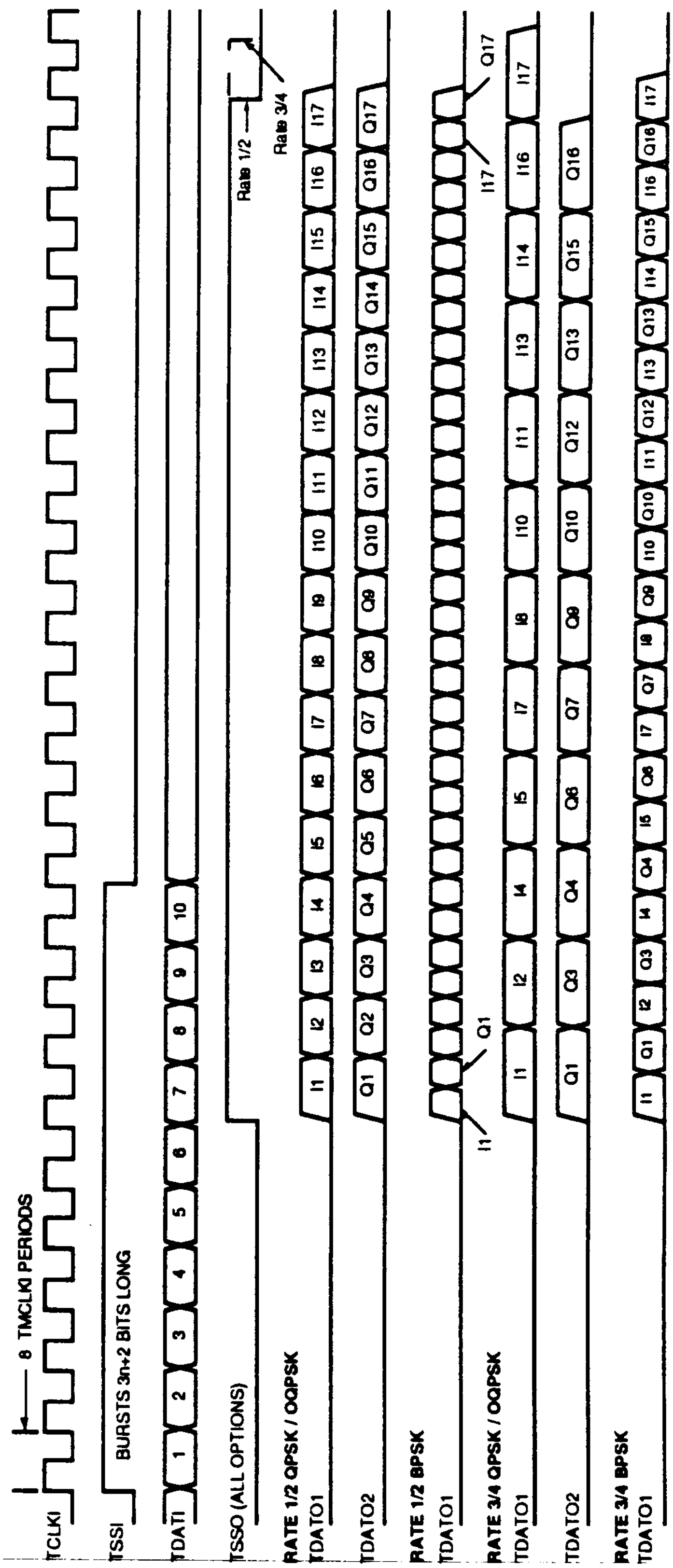
Bursts which are input to the encoder in lengths of 3n bits always result in output bursts which are of determinable length in all options.

Fig. 3 Encoder Timing Diagram for Operation with Bursts of Length 3n



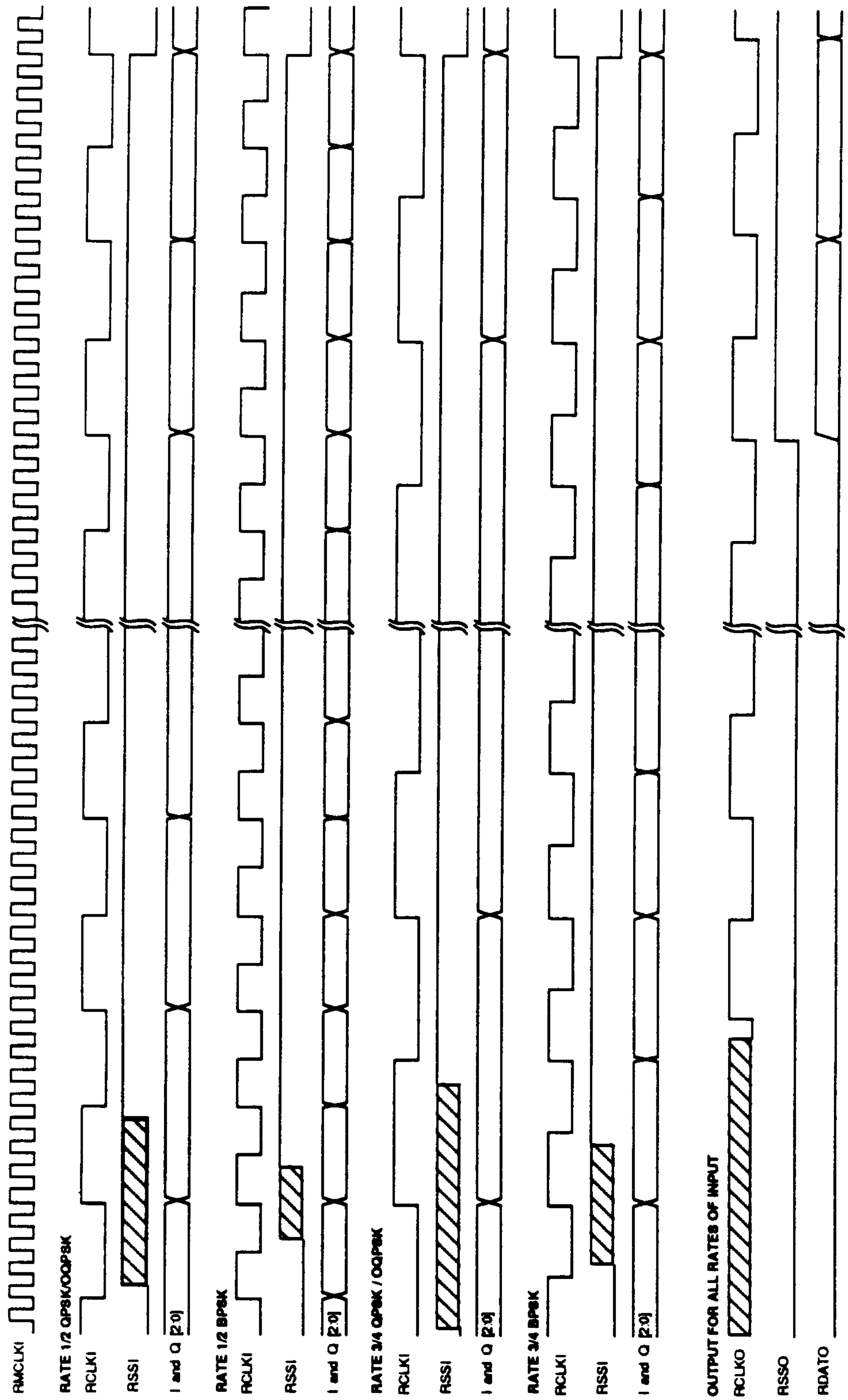
Bursts which are input to the encoder in lengths of 3n+1bits result in longer output bursts in Rate 3/4

Fig. 4 Encoder Timing Diagram for Operation with Bursts of Length 3n+1



Bursts which are input to the encoder in lengths of 3n+2 bits result in longer output bursts in Rate 3/4

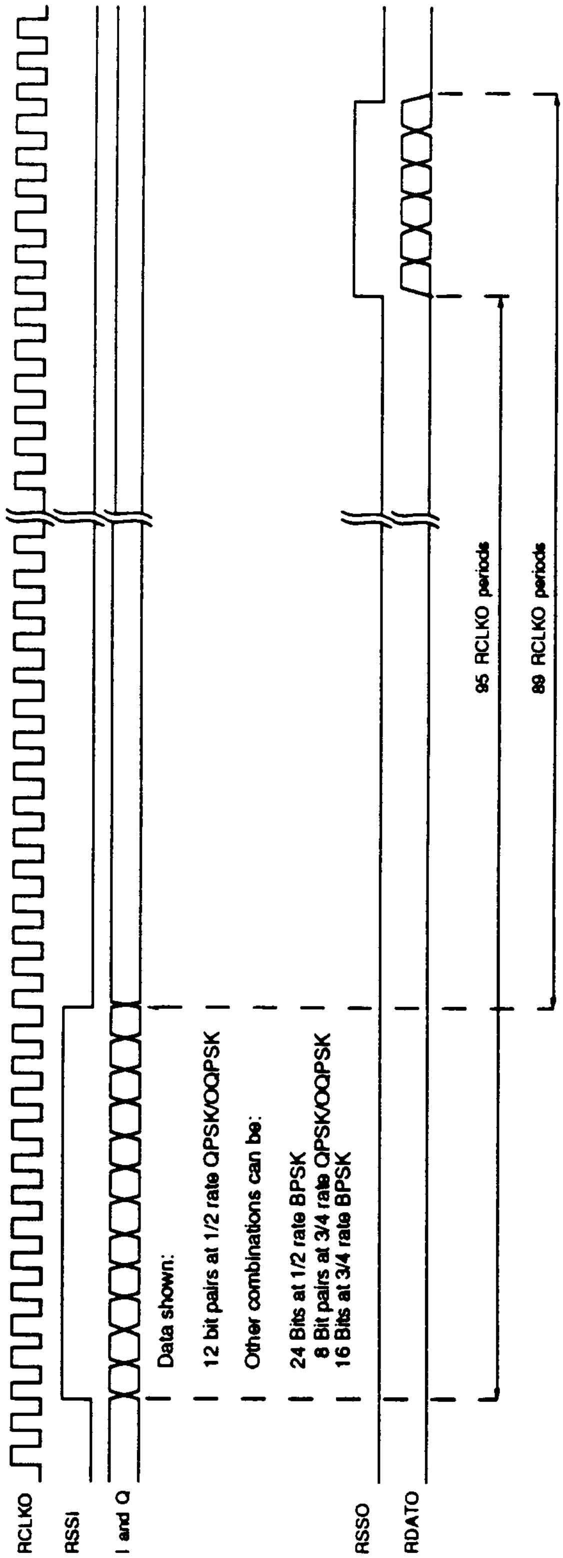
Fig. 5 Encoder Timing Diagram for Operation with Bursts of Length 3n+2



NOTE: 1) Incoming data (I and Q) is initially sampled by its accompanying RCLKI clock signal on a falling cock edge.

2) RCLKO phase is adjusted at the start of a burst relative to the LOW to HIGH transition of RSSI.

Fig. 6 Decoder Timing Diagram for Continuous Operation



Note:

1. Bursts can be streamed through the decoder with a minimum spacing of 6 RCLKO periods. The rising RSSI edges of the bursts must be a multiple of 3 RCLKO periods apart.

2 RSSI marks the length of the incoming burst which will always be a multiple of 3 RCLKO periods long if received from an identical device encoder.

Fig. 7 Decoder Timing Diagram for Burst Operation

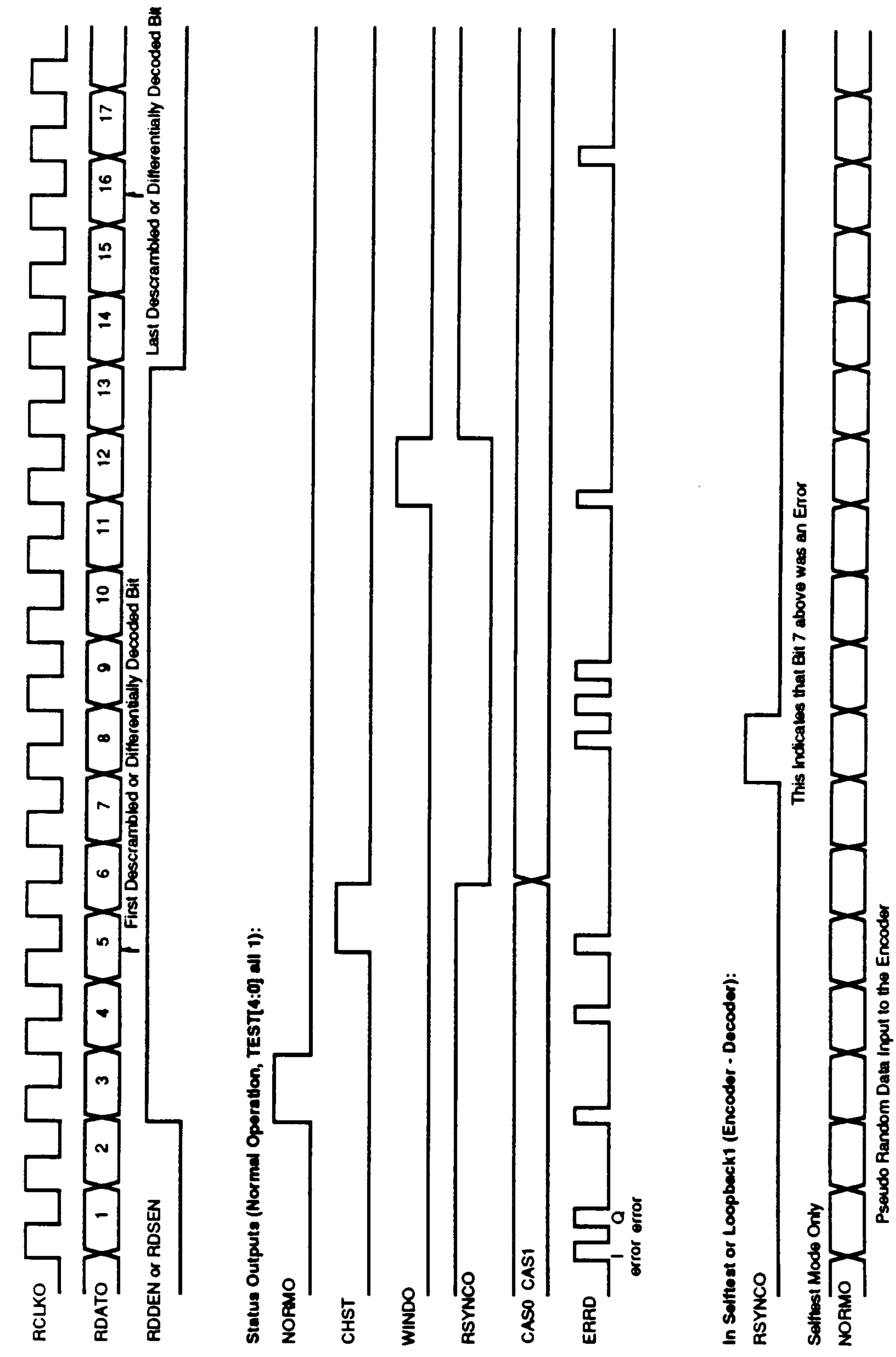


Fig. 8 Descrambler and Differential Decoder Timing Diagram

APPLICATION INFORMATION

Modulator Interface

Figure 9 illustrates the interface requirements to either a BPSK modulator and a QPSK modulator.

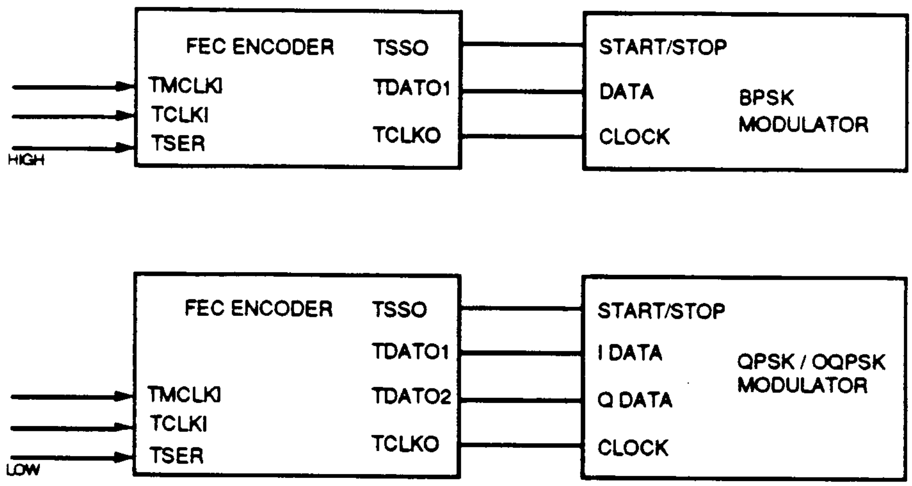


Fig. 9 Encoder-Modulator Interface

Soft Decision Options

Either hard decision or 2 bit or 3 bit soft decision can be implemented with this circuit. Figure 10 shows the connections for each option:

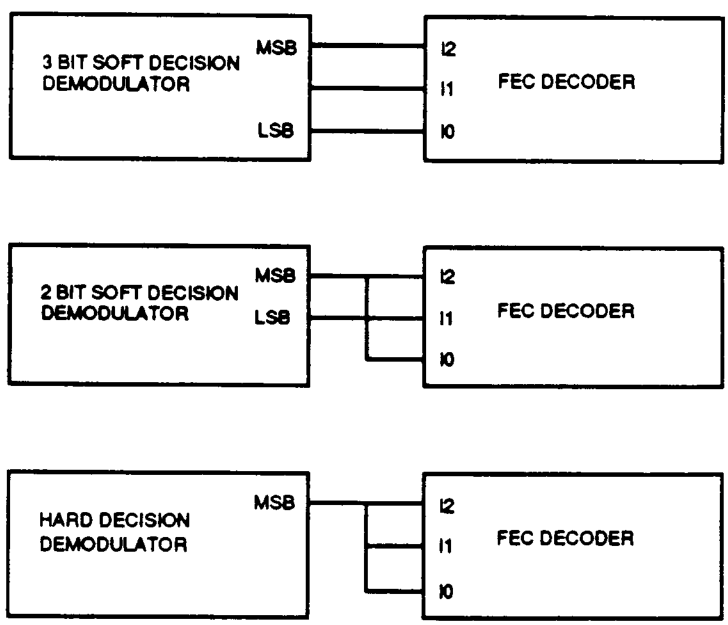


Fig. 10 Bit Slicer - Decoder Interface

Decoder-Demodulator Interface

Figure 11 illustrates the interface requirements to either a BPSK demodulator or a QPSK demodulator.

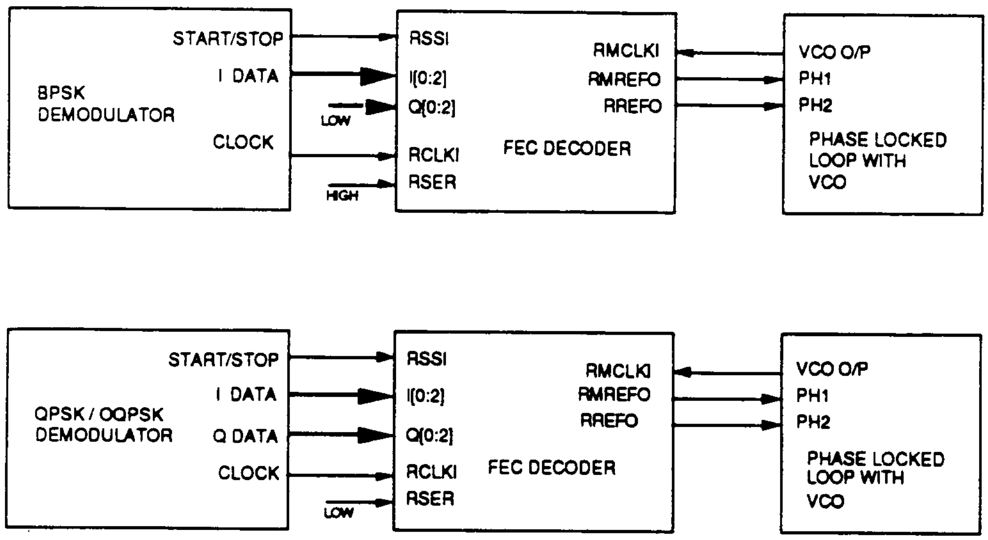


Fig. 11 Demodulator-Decoder Interface

Operation With A Jittery Clock

In the event that the receive clock contains too much jitter, it can be cleaned up by reconstructing it with a PLL. Figure 12 illustrates an example of this reconstruction:

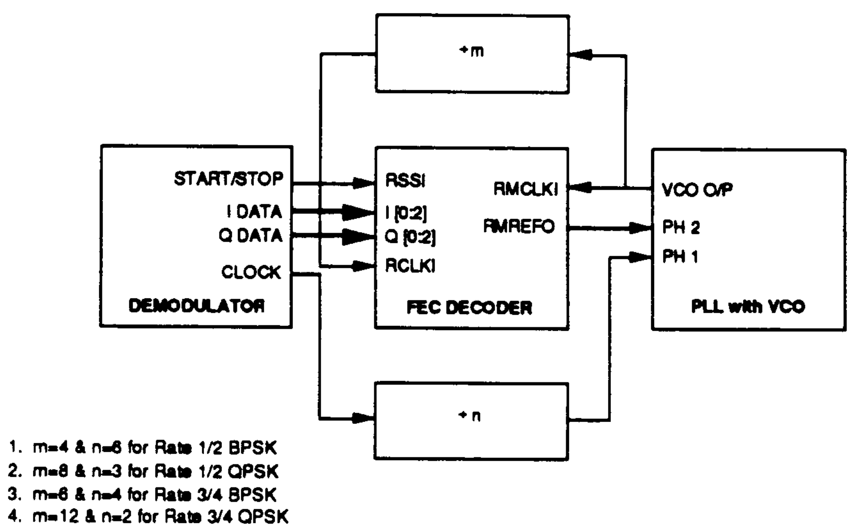


Fig. 12 Demodulator-Decoder Interface with a Jittery Demodulator Clock

Error Threshold Selection

The following tables contain the available options for error threshold selection. The window size is selectable in 8 different sizes from 256 bits to 32768 bits. The error threshold is selectable in fractions of the window size. Once the number of errors exceeds the selected fraction of bits in the given window size, a CHST pulse is sent to the ambiguity resolver.

Data Quality Monitor Error Threshold Selection

Ratio of channel errors to window size	ETI3	ETI2	ETI1	ETI0
1/8	0	0	0	0
5/32	0	0	0	1
3/16	0	0	1	0
7/32	0	0	1	1
1/4	0	1	0	0
9/32	0	1	0	1
5/16	0	1	1	0
11/32	0	1	1	1
3/8	1	0	0	0
13/32	1	0	0	1
7/16	1	0	1	0
15/32	1	0	1	1
1/2	1	1	0	0
17/32	1	1	0	1
9/16	1	1	1	0
19/32	1	1	1	1

Data Quality Monitor Error Threshold Selection

Window Size (decoded data bit)	WINDI2	WINDI1	WINDI0
256	0	0	0
512	0	0	1
1024	0	1	0
2048	0	1	1
4096	1	0	0
8192	1	0	1
16384	1	1	0
32768	1	1	1

It should be noted that the nominal setting for Rate 1/2 operation is a window size of 256 data bits with the threshold set to 7/16's of that window size. The nominal setting for Rate 3/4 is a window size of 2048 data bits with the threshold set to 3/16's of that window size.

Performance Curve

Figure 13 shows the performance improvement using 3 bit soft decision Viterbi decoding. As can be seen, performance improves approximately 5 dB at a bit error rate of 10^{-5}. It should be noted that this curve shows data with the optional differential coding and V.35 scrambling disabled. With these options enabled, a 0.3 dB margin should be added.

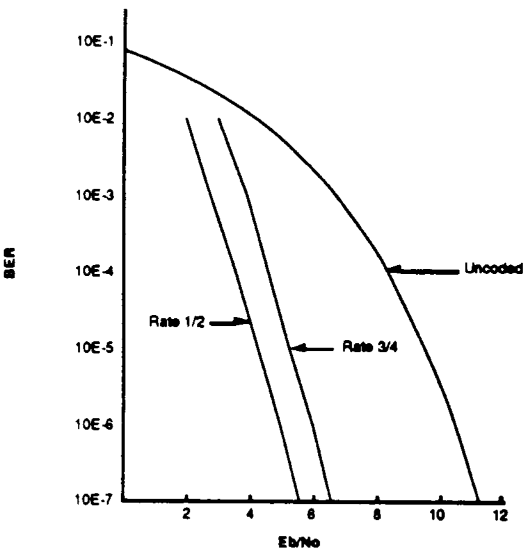


Fig. 13 PM7018 BER Performance Curve

ORDER INFORMATION:

Information Rate	Part Number	Package
4k to 256 kbit/sec	PM7018-256QC	68PLCC
4k to 2.5 Mbit/sec	PM7018-2500QC	68PLCC

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