# HA13559FP

**Voice Coil Motor Driver IC**

## Description

The HA13559FP IC that was developed for use as a voice coil motor driver in 12 V HDD applications. It provides the following functions and features.

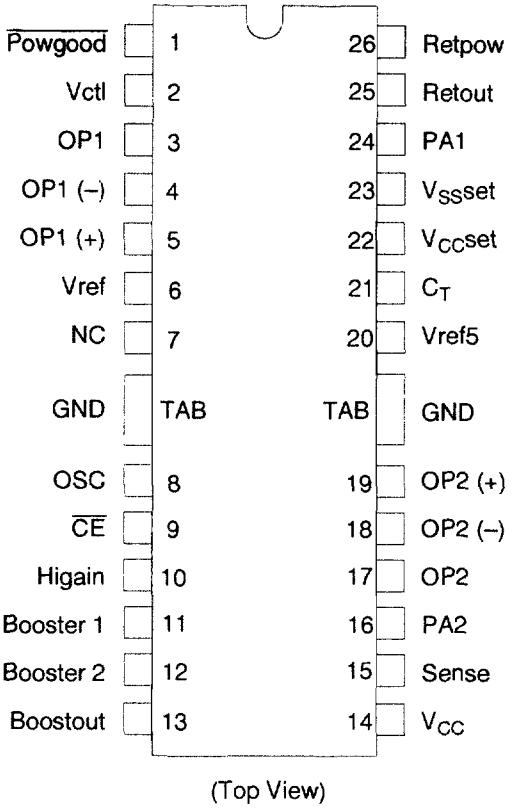
## Features

- Low saturation voltage
- Low crossover distortion
- Less external components

## Function

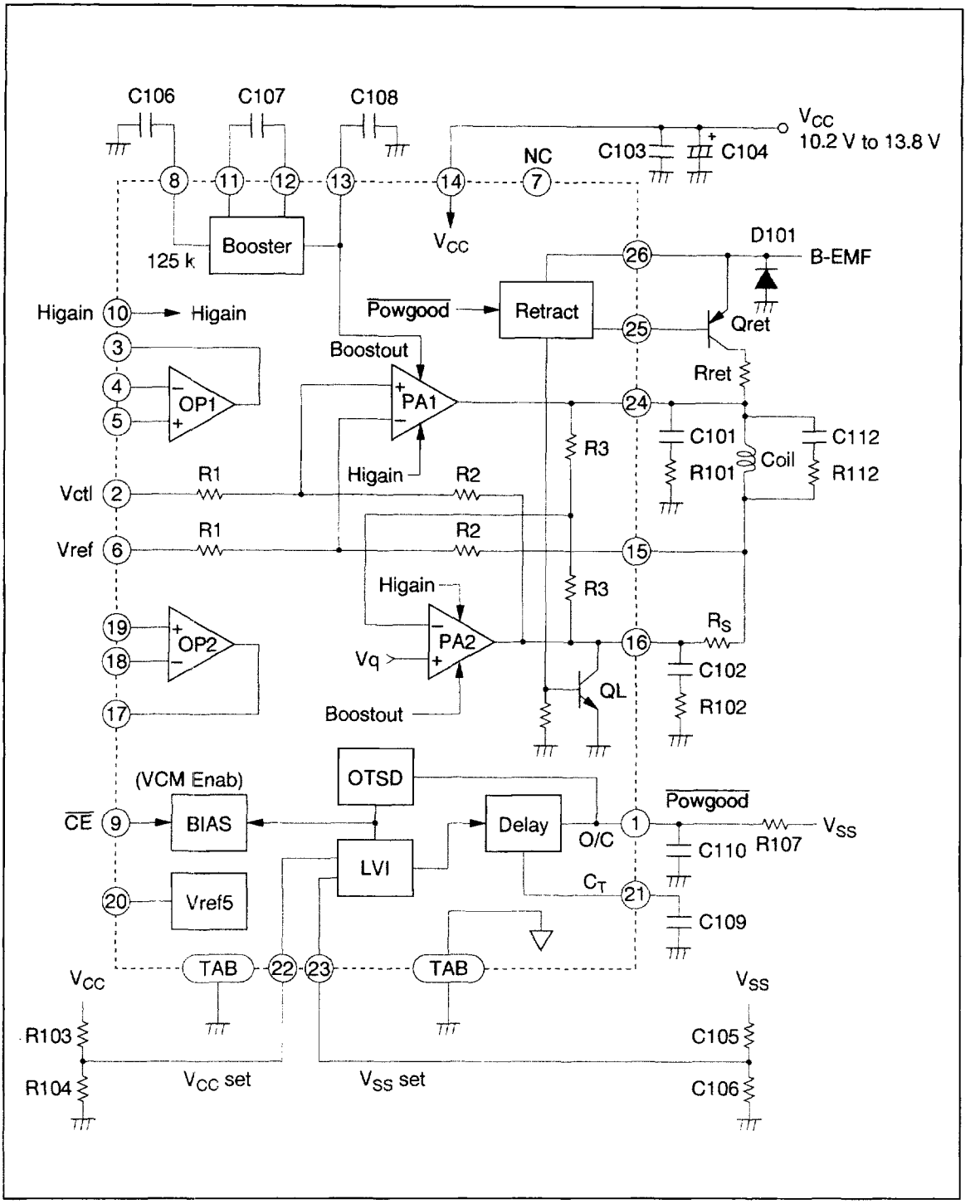
- 1.5 A BTL output amplifier (Dual gain)
- Auto-retraction circuit
- Two independent operational amplifiers
- 5 V reference voltage
- Thermal protection circuit OTSD
- Two under-voltage protection circuits LVI

## Pin Arrangement




(Top View)

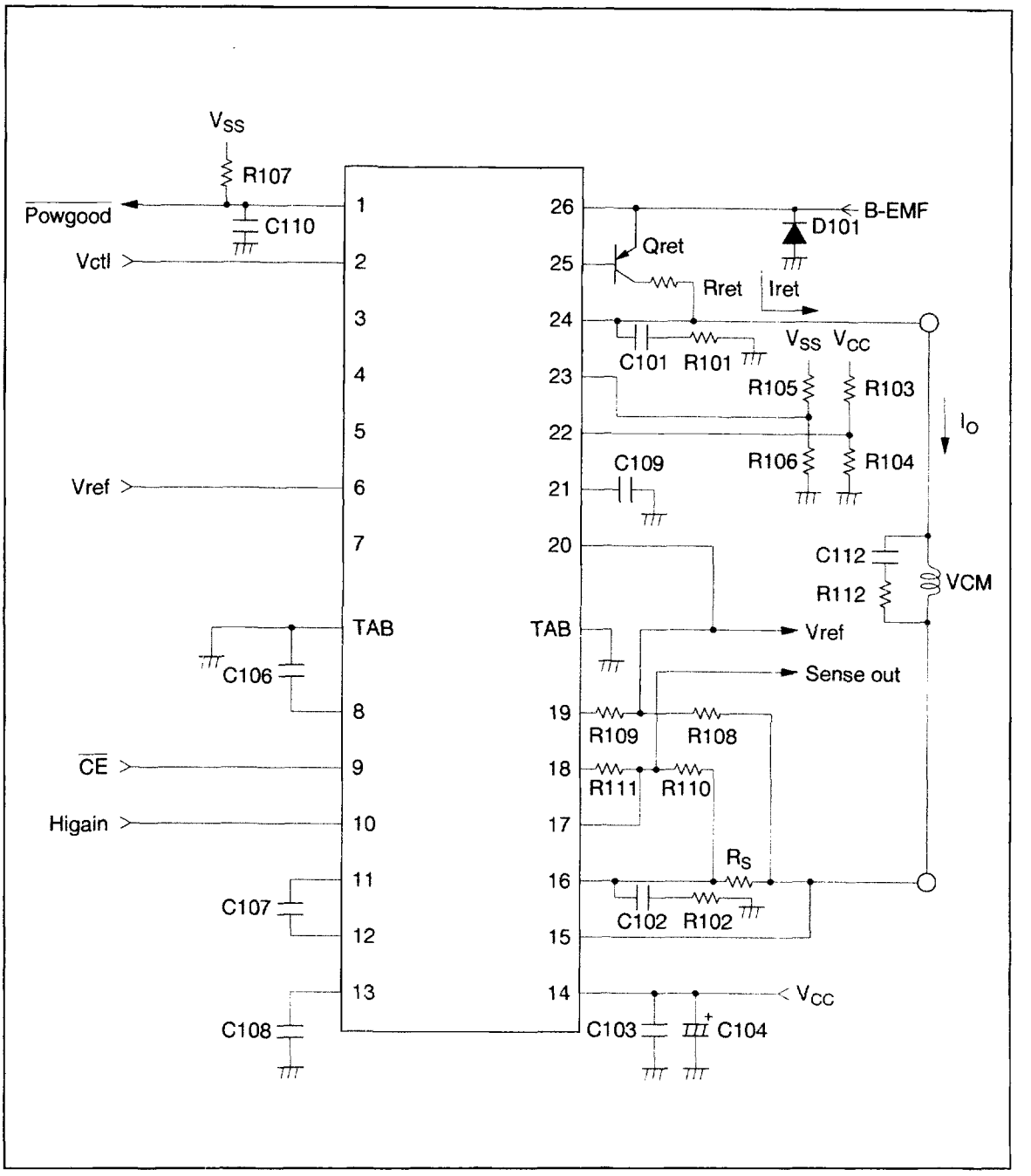
## Block Diagram



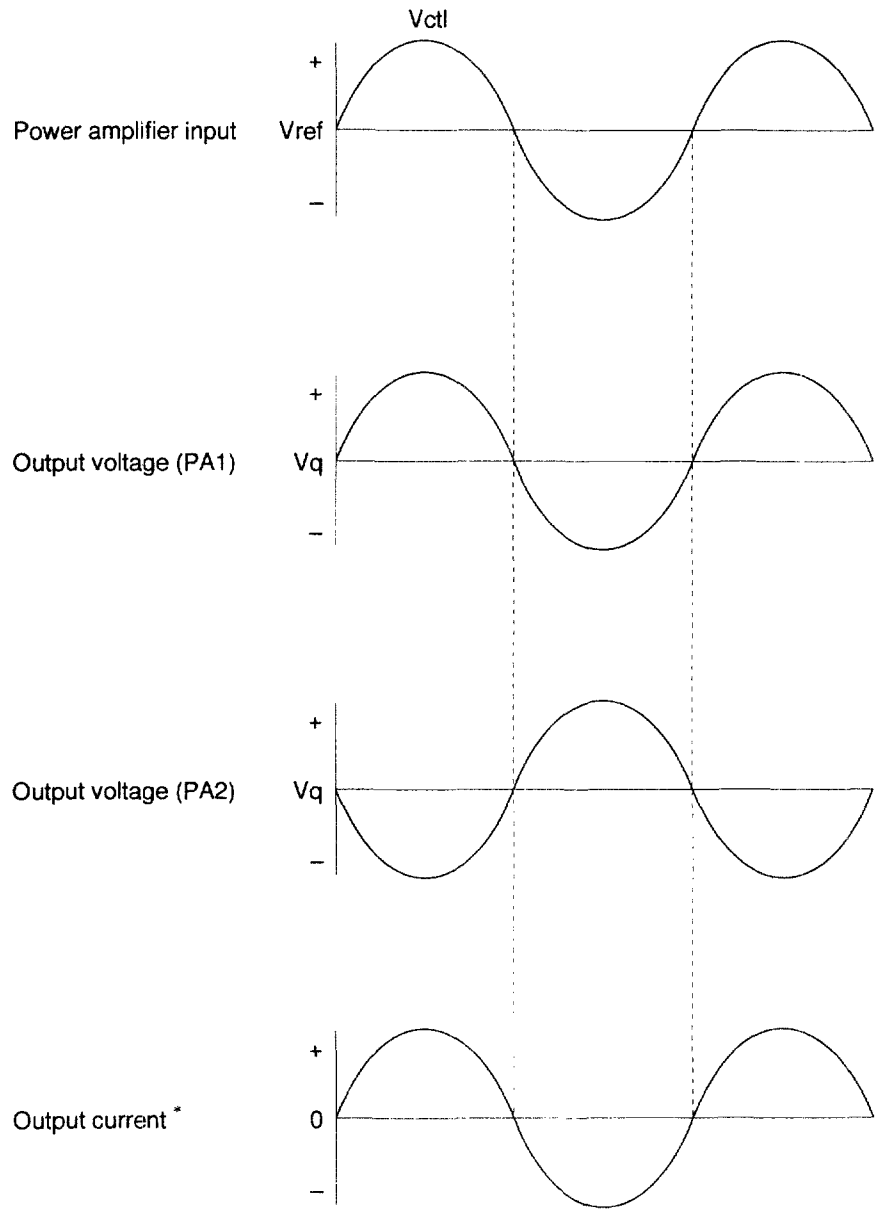
## Pin Assignment

| Pin No. | Symbol | Function |
|---|---|---|
| 1 | $\overline{\text{Powgood}}$ | Abnormal state monitor. Low: Normal state, High impedance: Abnormal state. Open collector output |
| 2 | Vctl | Power amplifier (+) input. PA1 output reference. |
| 3 | OP1 | Operational amplifier that operates when $V_{CC}$ > 10 V independent of the $\overline{\text{CE}}$ pin. Can be used for input filter. |
| 4 | OP1 (–) | OP1 (–) input Must be shorted to ground when unused. |
| 5 | OP1 (+) | OP1 (+) input |
| 6 | Vref | Power amplifier (–) input. PA1 output reference. |
| 8 | OSC | Used with the booster (charge pump) and as an oscillator frequency adjustment. |
| 9 | $\overline{\text{CE}}$ | Chip enable. Low: Enable, High: Disable |
| 10 | Higain | Power amplifier gain switch. Low: Low gain, High: High gain |
| 11 | Booster 1 | Booster (charge pump) pulse input |
| 12 | Booster 2 | Booster (charge pump) pulse output |
| 13 | Boostout | Booster output. Power amplifier pre-driver power supply |
| 14 | $V_{CC}$ | Power supply |
| 15 | Sense | Power amplifier current sense |
| 16 | PA2 | PA2 output |
| 17 | OP2 | Operational amplifier that operates when $V_{CC}$ > 10 V independent of the $\overline{\text{CE}}$ pin. Can be used as a sensor amplifier. |
| 18 | OP2 (–) | OP2 (–) input Must be shorted to ground when unused. |
| 19 | OP2 (+) | OP2 (+) input |
| 20 | Vref5 | 5 V Reference voltage. Use power amplifier reference voltage. |
| 21 | $C_T$ | $\overline{\text{Powgood}}$ falling edge delay time setting |
| 22 | $V_{CC}$set | $V_{CC}$ side LVI operating voltage (Vsd1) setting. Must be shorted to $V_{CC}$ if unused. |
| 23 | $V_{SS}$set | $V_{SS}$ side LVI operating voltage (Vsd2) setting. Must be shorted to $V_{CC}$ or $V_{SS}$ if unused. |
| 24 | PA1 | PA1 output |
| 25 | Retout | Retractor external PNP base current supply |
| 26 | Retpow | Retractor power supply. Can be used the spindle motor output. |

## Application



## Timing Chart




Notes: These waveforms are for input frequencies less than 1 kHz.
* Current flowing from PA1 to PA2 is indicated as positive (+), and current flowing from PA2 to PA1 is indicated as negative (–).

## Truth Table 1

| Inputs | | | | Outputs | | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_{SS}$ | $\overline{CE}$*2 | Higain*2 | PA1 | PA2 | Retout | $\overline{Powgood}$ |
| ≤Vsd1*1 | ≤Vsd2*1 | X | X | Disable | VsatL*3 | Iret*3 | Iret*3 |
| ≤Vsd1 | >Vsd2 | | | | | | |
| >Vsd1 | ≤Vsd2 | | | | | | |
| >Vsd1 | >Vsd2 | H | X | Disable | Disable | Z | L |
| | | L | H | High gain*1 | High gain*1 | Z | L |
| | | | L | Low gain*1 | Low gain*1 | Z | L |
| >Vsd1 | >Vsd2 | X | (Tj > Tsd) | Disable | VsatL*3 | Iret*3 | Z |

## Truth Table 2

| Inputs | Outputs | |
|---|---|---|
| $V_{CC}$ | OP1,OP2 | Vref5 |
| <7V | Disable | Disable |
| 8 V to 12 V | Enable | Enable |

Notes:
1. See the external components table.
2. Z = High impedance
   H = High voltage level
   L = Low voltage level
   X = Irrelevant
3. See the electrical characteristics table.

## External Components

| Part No. | Recommended Value | Purpose | Note |
|---|---|---|---|
| R101, R102 | 2.2 Ω | Power amplifier output stabilization | 1 |
| R103, R104 | — | LVI voltage setting ($V_{CC}$) | 2 |
| R105, R106 | — | LVI voltage setting ($V_{SS}$) | 3 |
| R107 | — | $\overline{\text{Powgood}}$ pull-up | |
| R108 to R111 | — | Output sense amplifier gain setting | |
| R112 | 130 Ω | Reduction for gain peaking | |
| $R_S$ | 1.0 Ω | Power amplifier output current detection | 4 |
| Rret | — | Retractor current limiter | 5 |
| Qret | — | Retractor | 5 |
| C101, C102 | 0.1 µF | Power amplifier output stabilization | 1 |
| C103, C104 | 0.1 µF, 4.7 µF | Power supply stabilization | |
| C106 | 820 pF | Booster (oscillation) | |
| C107, C108 | 0.1 µF, 2.2 µF | Booster | |
| C109 | 0.01 µF | $\overline{\text{Powgood}}$ delay setting | 6 |
| C110 | 0.0022 µF | $\overline{\text{Powgood}}$ filter | |
| C112 | 0.47 µF | Reduction for gain peaking | |
| D101 | $V_F$ < 0.75 V ($I_F$ = 0.5 A) | B-EMF clamp | |

Notes: 1. Can be omitted depending on the used coil.

2. The LVI1 ($V_{CC}$) operating voltage (Vsd1) and hysteresis (Vhys1) are determined by the following formulas.

$$Vsd1 = \left(1 + \frac{R103}{R104}\right) \cdot Vref1\ (V)$$ (Set Vsd1 to be 9.0 V or higher.)

$$Vhys1 = \left(1 + \frac{R103}{R104}\right) \cdot Vhys1\ (V)$$ Vref1, Vhys1 : See the electrical characteristics table.

3. The LVI2 ($V_{SS}$) operating voltage (Vsd2) and hysteresis (Vhys2) are determined by the following formulas.

$$Vsd2 = \left(1 + \frac{R105}{R106}\right) \cdot Vref2\ (V)$$ (Set Vsd2 to be 3.0 V or higher.)

$$Vhys2 = \left(1 + \frac{R105}{R106}\right) \cdot Vhys2\ (V)$$ Vref2, Vhys2 : See the electrical characteristics table.

4. The relationship between the PA output current ($I_O$) and input voltage (Vctl) is determined by the following formula.

$$I_O = \frac{(Vctl - Vref)\ Gctl}{R_S} = \frac{(Vctl - Vref) \cdot gm \cdot R'_S}{R_S}$$

Where: Gctl : $gm \cdot R'_S$ (See the electrical characteristics table.)
Vref : PA1 reference voltage

5. The retract current (Iret) is determined by the following formula.

$$Iret = \frac{Vretpow - Vretsat - VsatL}{R_L + R_S + Rret}$$

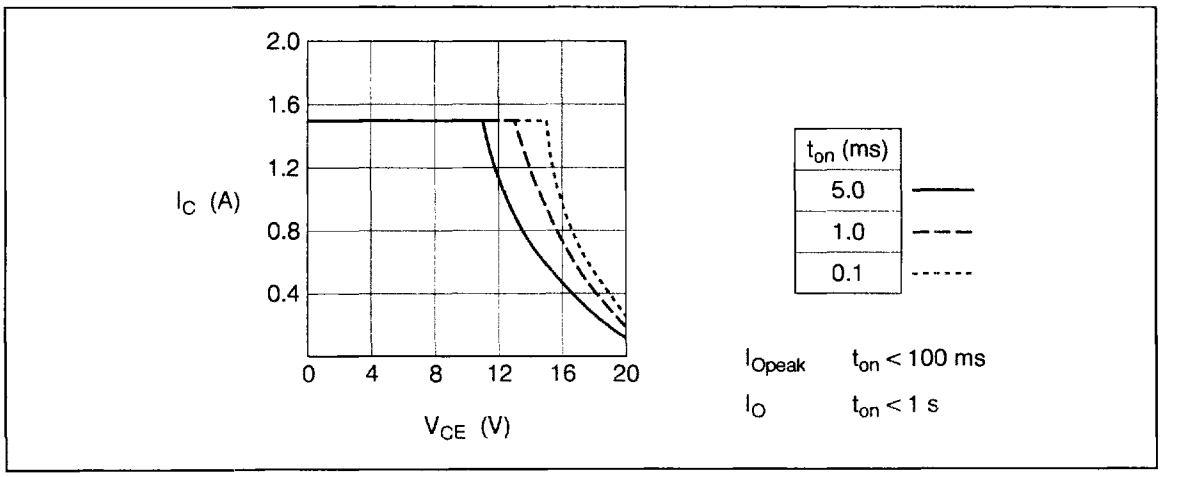
Where: Vretpow : Retpow voltage
Vretsat : Qret saturation voltage
$R_L$ : Load resistance
VsatL : PA2 lower side saturation voltage (See the electrical characteristics table.)

6. The $\overline{\text{Powgood}}$ delay time (Tpor) is determined by the following formulas.
Tporhl = $C_T \cdot Vth$ / Icha
Tporlh ≤ $C_T\ (V_{CC} - Vth)$ / Idis

## Absolute Maximum Ratings

| Item | Symbol | Rating | Unit | Note |
|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 15 | V | 1 |
| Peak output current | $I_{Opeak}$ | 1.5 | A | 2 |
| Steady-state output current | $I_O$ | 1.0 | A | 2 |
| Retract current | Iret | 0.2 | A | 3 |
| Input voltage | Vin | $V_{CC}$ | V | |
| Allowable power dissipation | $P_T$ | 6.0 ($T_C$ = 100°C) | W | 4 |
| Junction temperature | Tj | +150 | °C | 5 |
| Storage temperature | Tstg | –55 to +125 | °C | |

Notes: 1. The operating voltage range is as follows:
$V_{CC}$ = 10.2 V to 13.8 V
2. ASO of each output transistor is shown below. Operating locus must be within the ASO.




3. Applies to the PA2 lower side transistor. (Qret)
4. Permitted value at $T_C$ = 100°C. Thermal resistance is shown below.
θj-c ≤ 8 °C/W
θj-a ≤ 35 °C/W (when a 6-layer printed circuit board is used)
θj-a ≤ 62 °C/W (when a glass epoxy printed circuit board is used with a wiring density of 20%)
5. The junction operating temperature range is as follows.
Tjopr = 0 °C to 125 °C

## Electrical Characteristics (Ta = 25°C, $V_{CC}$ = 12 V, $V_{SS}$ = 5 V)

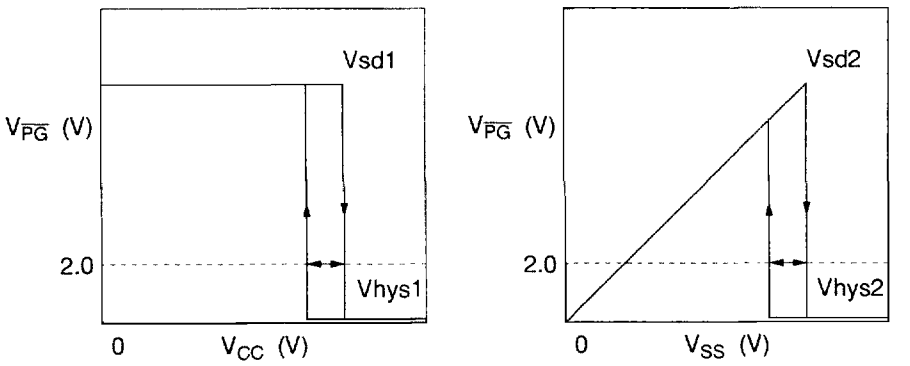
| Item | | Symbol | Min | Typ | Max | Unit | Test Condition | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| Quiescent current | | $I_{CC0}$ | — | 3.5 | 5.0 | mA | $\overline{CE}$ = H | 14 | |
| | | $I_{CC1}$ | — | 15 | 20 | mA | $\overline{CE}$ = L, $V_{SS}$ = 5V | | |
| | | Iretpow | — | 50 | 70 | mA | $\overline{CE}$ = L, $V_{SS}$ = 0V Vretpow = 5 V | 26 | |
| $\overline{CE}$, Higain | Input current | Iin1 | — | — | ±10 | µA | | 9, 10 | |
| | Input high voltage | Vih1 | 2.0 | — | — | V | | | |
| | Input low voltage | Vil1 | — | — | 0.8 | V | | | |
| PA1, PA2 | Input resistance | Rin (H) | 18.75 | 25 | 31.25 | kΩ | Higain = H | 2, 6 | |
| | | Rin (L) | 30 | 40 | 50 | kΩ | Higain = L | | |
| | Common mode input voltage range | Vcm (H) | 0 | — | $V_{CC}$ − 2.0 | V | Higain = H | | |
| | | Vcm (L) | 0 | — | $V_{CC}$ − 2.0 | V | Higain = L | | |
| | Output quiescent-voltage | Vq | 5.6 | 6.0 | 6.4 | V | $R_L$ = 10 Ω, $R_S$ = 1.0 Ω | 16, 24 | |
| | Output offset voltage (PA2-sense) | Vofs (H) | — | — | ±6 | mV | Higain = H, $R_S$ = 1.0 Ω, $R_L$ = 10 Ω Vctl = Vref = 6.0 V | | |
| | | Vofs (L) | — | — | ±5 | mV | Higain = L, $R_S$ = 1.0 Ω, $R_L$ = 10 Ω Vctl = Vref = 6.0 V | | |
| | Output saturation voltage | Vsat1 | — | 0.8 | 1.1 | V | $I_O$ = 0.8 A | | 1 |
| | | Vsat2 | — | 0.4 | 0.55 | V | $I_O$ = 0.4 A | | |
| | Output leak current | $I_{CER}$ | — | — | ±100 | µA | $V_{CE}$ = 15 V | | 2 |
| | Transfer gain | gm (H) | 0.86 | 0.93 | 1.00 | A/V | Higain = H, $R_L$ = 10 Ω $R'_S$ = 1.0 Ω | 2, 6, 16, 24 | |
| | | gm (L) | 0.22 | 0.24 | 0.26 | A/V | Higain = L, $R_L$ = 10 Ω $R'_S$ = 1.0 Ω | | |
| | Gain bandwidth (resistive load) | B (H) | — | 70 | — | kHz | Higain = H $R_L$ = 10 Ω, $R_S$ = 1.0 Ω | | 3 |
| | | B (L) | — | 120 | — | kHz | Higain = L $R_L$ = 10 Ω, $R_S$ = 1.0 Ω | | |
| Retract | Retpow voltage | Vretpow | 0.8 | — | — | V | Iretout = 0.1 mA | 26 | |
| | Retout output current | Iretout | 5.0 | 9.0 | — | mA | Vretpow = 3 V | 25 | |
| | QL saturation voltage | VsatL | — | 0.1 | 0.25 | V | Iret = 0.1 A Vretpow = 3 V | 16 | |

## Electrical Characteristics (Ta = 25°C, $V_{CC}$ = 12 V, $V_{SS}$ = 5 V) (cont)

| Item | | Symbol | Min | Typ | Max | Unit | Test Condition | Applicable Pins | Note |
|---|---|---|---|---|---|---|---|---|---|
| OP1, OP2 | Input current | Iinop | — | — | ±500 | nA | | 4, 5 18, 19 | |
| | Input offset voltage | Vosop | — | — | ±7 | mV | | | |
| | Common mode input voltage range | Vcmop | 0 | — | $V_{CC}$ −1.8 | V | | | |
| | Output high voltage | Vohop | $V_{CC}$ −1.3 | — | — | V | Iout = 1.0 mA | 3, 17 | |
| | Output low voltage | Volop | — | — | 1.1 | V | | | |
| | Open loop gain | Gop | — | 41 | — | dB | f = 10 kHz | | 3 |
| | Gain bandwidth | Bop | — | 1.5 | — | MHz | Gop = 0 dB | | |
| $\overline{\text{Powgood}}$ | Output leak current | Ileak | — | — | ±10 | μA | Voh = 15 V | 1 | |
| | Output low voltage | Vol | — | 0.1 | 0.4 | V | Iol = 1 mA | | |
| Vref5 | Output voltage | Vref5 | 4.75 | 4.9 | 5.05 | V | $I_O$ = 20 mA | 20 | |
| | Output resistance | Rout | — | — | 5 | Ω | $I_O$ = 20 mA | | |
| LVI | Reference voltage | Vref1 | 1.32 | 1.36 | 1.40 | V | R103 = 62 kΩ | 22, 23 | |
| | | Vref2 | 1.28 | 1.32 | 1.36 | V | R104 = 10 kΩ | | |
| | Hysteresis | Vhys1 | 40 | 80 | 100 | mV | R105 = 18 kΩ | | |
| | | Vhys2 | 60 | 105 | 130 | mV | R106 = 10 kΩ | | |
| Delay | Threshold voltage | Vth | — | 2.5 | — | V | | 21 | |
| | $C_T$ charge current | Icha | — | 10 | — | μA | | | |
| | $C_T$ discharge current | Idis | 1.0 | 1.8 | — | mA | | | |
| OTSD | Operating temperature | Tsd | 125 | 150 | — | °C | | | 3 |
| | Hysteresis | Thys | — | 25 | — | °C | | | |

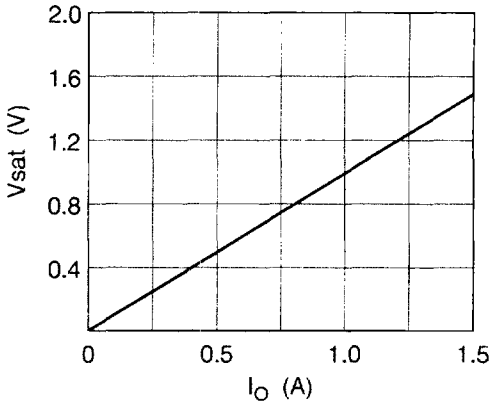
Notes: 1. The output saturation voltage is the sum of the upper and lower saturation voltages.
2. The value is output transistor only, not include Feed back resistance etc.
3. These are design center values and are not (and cannot be) tested in the mass production products.

The LVI circuit has the hysteresis, and it is shown below.

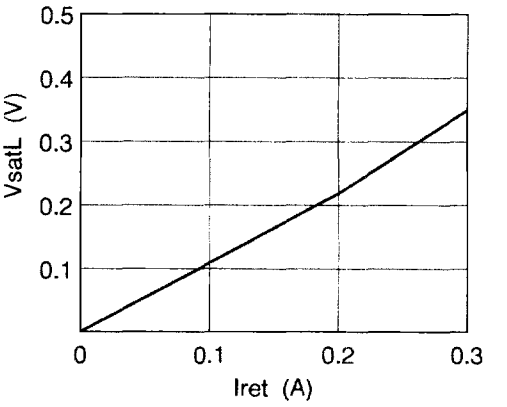


## Main Characteristics

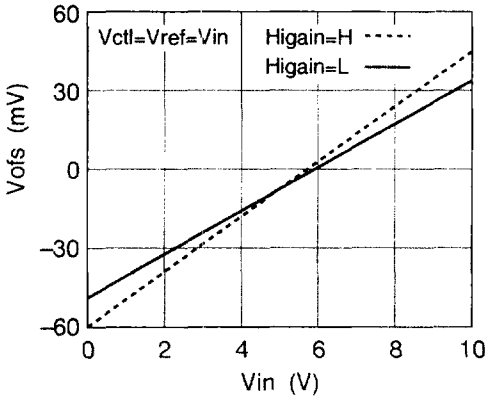
Output Saturation Voltage vs. Output Current




Lower Side Saturation Voltage vs. Retractor Current




Input Voltage vs. Output Offset Voltage




Output Current Frequency Characteristics