120W - 28V - 175MHz

GOLD METALIZED MULTI-PURPOSE SILICON DMOS RF FET

FEATURES

- METAL GATE
- EXTRA LOW Crss
- BROAD BAND
- SIMPLE BIAS CIRCUITS
- LOW NOISE
- HIGH GAIN

APPLICATIONS

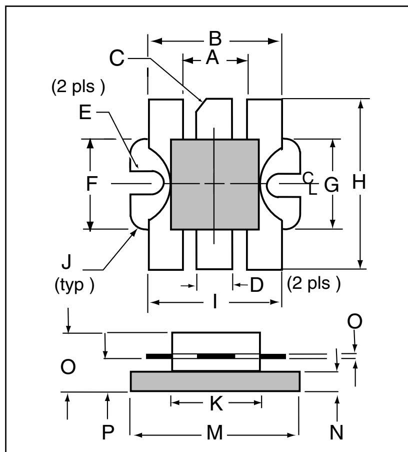
- HF/VHF/UHF COMMUNICATIONS

ABSOLUTE MAXIMUM RATINGS (T_{CASE} = 25°C unless otherwise stated)		
P_D	Power Dissipation	220W
BV_{DSS}	Drain-source breakdown voltage	70V
V_{GSS}	Gate-source voltage	±20V
I_D	Drain Current	30A
T_{stg}	Storage temperature	-65 to 150°C
T_j	Maximum operating junction temperature	200°C
$R_{THj-case}$	Thermal resistance junction-case	Max..8°C/W

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25°C unless otherwise stated)

Parameter		Test Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Breakdown voltage, drain source	V_{GS}=0 I_D=100mA	70			Vdc
I_{DSS}	Drain leakage current	V_{DS}=28V V_{GS}=0			6	mAdc
I_{GSS}	Gate leakage current	V_{GS}=20V V_{DS}=0			1	µAdc
$V_{GS(th)}$	Gate threshold voltage	I_D=10mA V_{DS}=V_{GS}	1		7	Vdc
gfs	Transconductance (300µs pulse)	V_{DS}=10V I_D=6A	4.8			mhos
G_{PS}	Common source power gain	P_O=120W	16			dB
η	Drain efficiency	V_{DS}=28V I_{DQ}=1.2A	50			%
VSWR	Load mismatch tolerance	f=175MHz	20:1			
C_{iss}	Input capacitance	V_{DS}=0V V_{GS}=-5V f=1MHz			360	pF
C_{oss}	Output capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			180	pF
C_{rss}	Reverse transfer capacitance	V_{DS}=28V V_{GS}=0 f=1MHz			15	pF

DIMENSIONS



DM	Millimeter	TOL	Inches	TOL
A	9.09	.13	.358	.005
B	19.30	.13	.760	.005
C	45°	5°	45°	5°
D	5.71	.13	.225	.005
E	1.65R	.13	.065R	.005
F	9.78	.13	.385	.005
G	10.16	.13	.400	.005
H	20.32	.25	.800	.010
I	19.30	.13	.760	.005
J	1.52R	.13	.060R	.005
K	10.77	.13	.424	.005
M	22.86	.13	.900	.005
N	3.17	.13	.125	.005
O	0.13	.02	.005	.001
P	4.19	.13	.165	.005
Q	6.35	REF	.250	REF

HAZARDOUS MATERIAL WARNING

The ceramic portion of the device between leads and metal flange is beryllium oxide. Beryllium oxide dust is highly toxic and care must be taken during handling and mounting to avoid damage to this area. THESE DEVICES MUST NEVER BE THROWN AWAY WITH GENERAL INDUSTRIAL OR DOMESTIC WASTE.

U.S. PATENTS 5,121,176 & 5,179,032
GLOBAL PATENTS PENDING

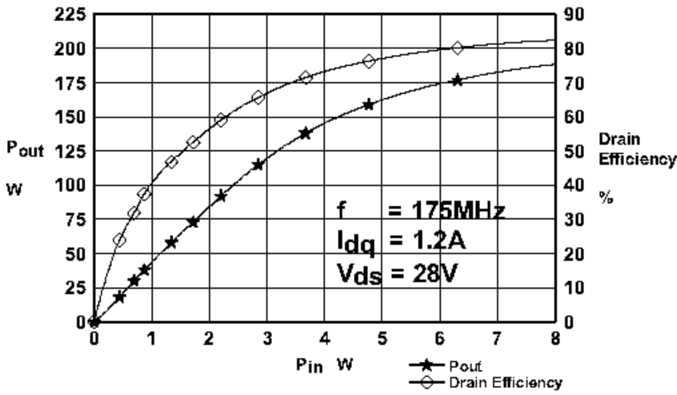


Figure 1.
Power Output and Efficiency vs.Input Power

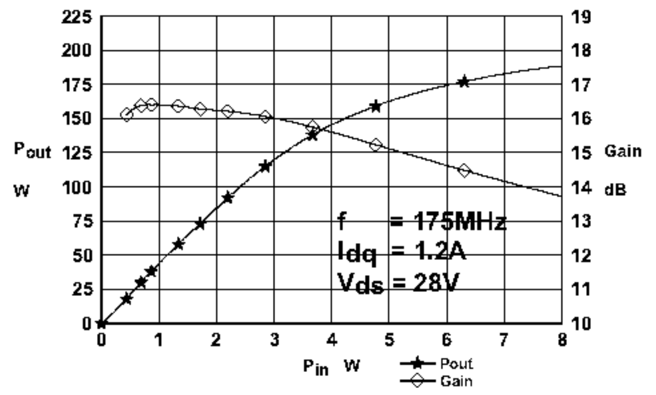


Figure 2.
Power Output and Gain vs. Input Power

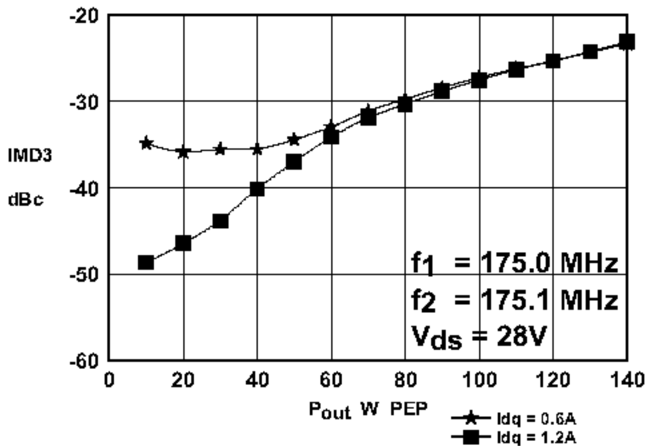
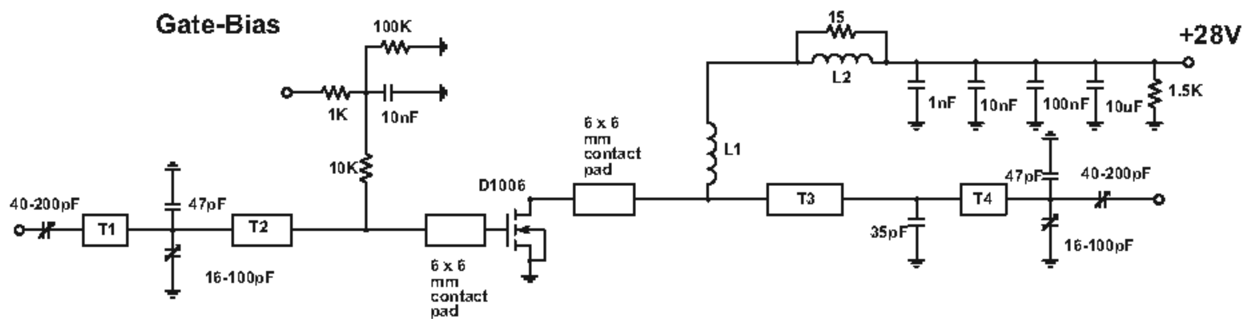


Figure 3.
IMD vs Output Power

D1006

OPTIMUM SOURCE AND LOAD IMPEDANCE

Frequency MHz	Z_S Ω	Z_L Ω
175	0.5 - j0.6	1.7 - j0.1



175 MHz Test Fixture

Substrate 1.6mm PTFE/glass, Er = 2.5
All microstrip lines W = 5mm

T1	10mm
T2	23.5mm
T3	25mm
T4	6mm
L1	9 turns 20swg encamelled copper wire, 6mm i.d.
L2	11 turns 19swg enamelled copper wire on Fair-Rite FT82 ferrite core

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*D1006

*PSPICE MODEL FOR POINT NINE RF N-CHANNEL VERTICAL DMOS POWER FET
*May 2004


*                  ____GATE
*                  I   ____DRAIN
*                  I   I   ____SOURCE
*                  I   I   I
.SUBCKT D1006  10  20  30
*Cin1,Cin2 & Lin model the input side of the package
Cin1   10    30    0.44p
Lin    10    11    0.2n
Cin2   11    30    0.44p
LG     11    12    0.6n      ;Gate bond wire inductance
CGS    12    13    276p      ;Gate-source capacitance
MOS    14    12    13    13  D1006 L=0.9U W=0.336    ;D G S B LEVEL1
JFET   16    13    14        D1006                   ;D G S
DBODY  13    16              D1006                   ;P N
LS     13    30    0.3n      ;Source bond wire inductance
CGD    12    16    6p        ;Gate-drain feedback capacitance

*Cout1,Cout2 & Lout model the output side of the package
Cout1  16    30    1.45p
Lout   16    20    0.67n
Cout2  20    30    1.2p

.MODEL D1006 NMOS (VTO=4.76 KP=2.811E-5 LAMBDA=0.032 RD=0.013 RS=0.051)

.MODEL D1006  NJF  (VTO=-4.3 BETA=1.5 LAMBDA=0.54)
.MODEL D1006  D    (CJO=493.2P RS=0.25 VJ=0.7 M=0.35 BV=75)

.ENDS
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