

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

D2661, DECEMBER 1983—MAY 1986

- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Choice of True or Inverting Data Paths
- Choice of 3-State or Open-Collector Outputs
- Package Options Include Plastic "Small Outline" Packages, Both Plastic and Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

DEVICE	OUTPUT	LOGIC
'ALS646, 'AS646	3-State	True
'ALS647	Open-Collector	True
'ALS648, 'AS648	3-State	Inverting
'ALS649	Open-Collector	Inverting

description

These devices consist of bus transceiver circuits, with 3-state or open-collector outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal bus transceivers and registers.

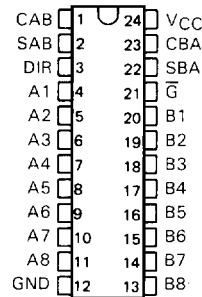
Enable (\bar{G}) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The circuitry used for select control will eliminate the typical decoding glitch which occurs in a multiplexer during the transition between stored and real-time data. The direction control determines which bus will receive data when enable \bar{G} is active (low). In the isolation mode (control \bar{G} high), A data may be stored in one register and/or B data may be stored in the other register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

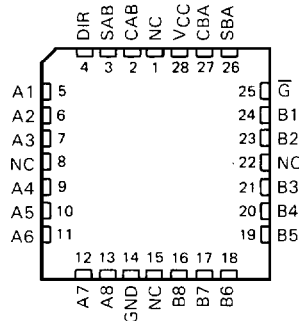
The -1 versions of the SN74ALS' parts are identical to the standard versions except that the recommended maximum I_{OL} is increased to 48 milliamperes. There are no -1 versions of the SN54ALS' parts.

The SN54' family is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74' family is characterized for operation from 0°C to 70°C .

SN54ALS', SN54AS' . . . JT PACKAGE
SN74ALS', SN74AS' . . . DW OR NT PACKAGE
(TOP VIEW)

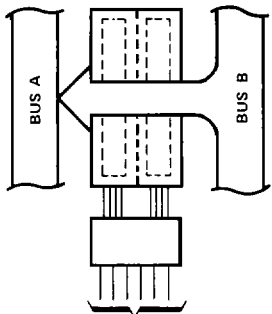


SN54ALS', SN54AS' . . . FK PACKAGE
SN74ALS', SN74AS' . . . FN PACKAGE
(TOP VIEW)



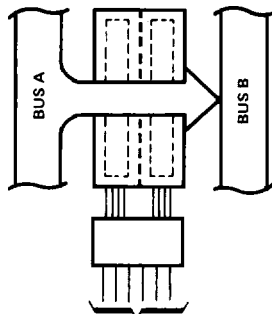
NC—No internal connection

**SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648
SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS**



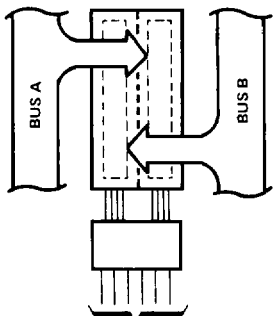
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS B TO BUS A**



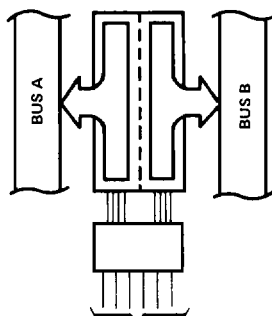
(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	H	X	X	L	X

**REAL-TIME TRANSFER
BUS A TO BUS B**



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

**STORAGE FROM
A, B, OR A AND B**



(21)	(3)	(1)	(23)	(2)	(22)
G	DIR	CAB	CBA	SAB	SBA
L	L	X	HorL	X	H
L	H	HorL	X	H	X

**TRANSFER
STORED DATA
TO A OR B**

SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648 SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648 OCTAL BUS TRANSCEIVERS AND REGISTERS

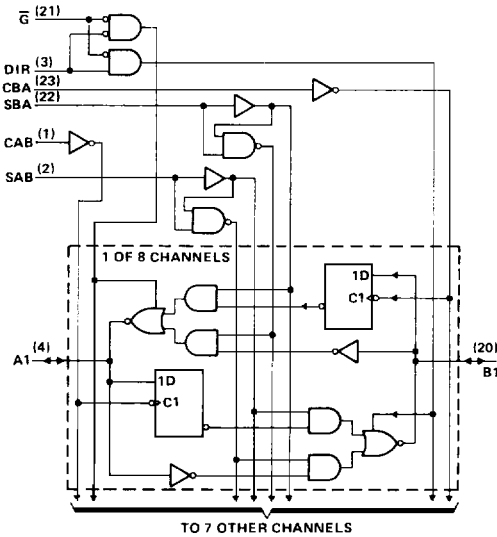
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION	
G	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†	Store B, A unspecified†
H	X	↑	↑	X	X	input	Input	Store A and B Data Isolation, hold storage	Store A and B Data Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time \bar{B} Data to A Bus Stored \bar{B} Data to A Bus
L	L	X	H or L	X	H	Output	Input	Real-Time A Data to B Bus Stored A Data to B Bus	Real-Time \bar{A} Data to B Bus Stored \bar{A} Data to B Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus	Real-Time \bar{A} Data to B Bus Stored \bar{A} Data to B Bus
L	H	H or L	X	H	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus	Real-Time \bar{A} Data to B Bus Stored \bar{A} Data to B Bus

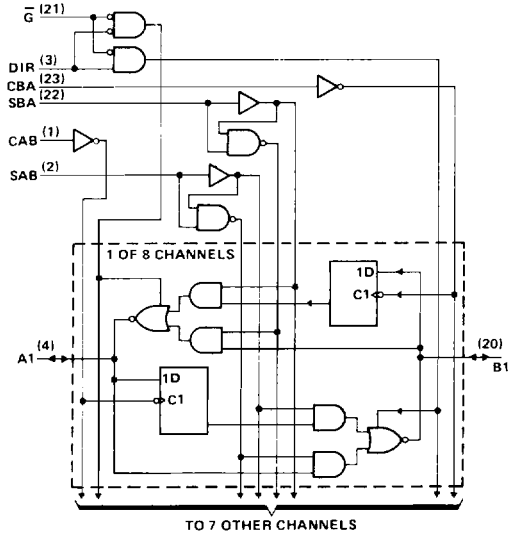
†The data output functions may be enabled or disabled by various signals at the \bar{G} and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

functional block diagrams (positive logic)

'ALS646, 'AS646, 'ALS647



'ALS648, 'AS648, 'ALS649

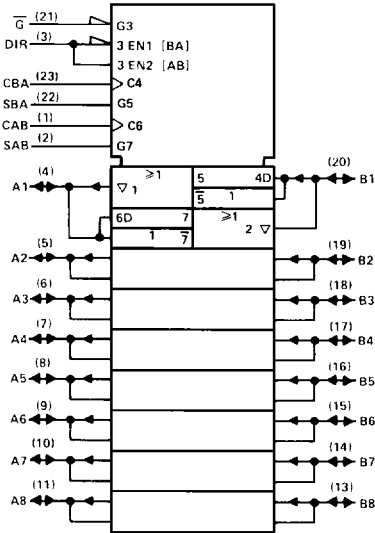


Pin numbers shown are for DW, JT, and NT packages.

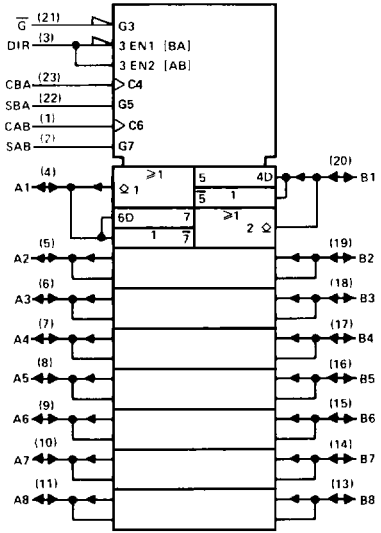
**SN54ALS646 THRU SN54ALS649, SN54AS646, SN54AS648
SN74ALS646 THRU SN74ALS649, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS**

logic symbols†

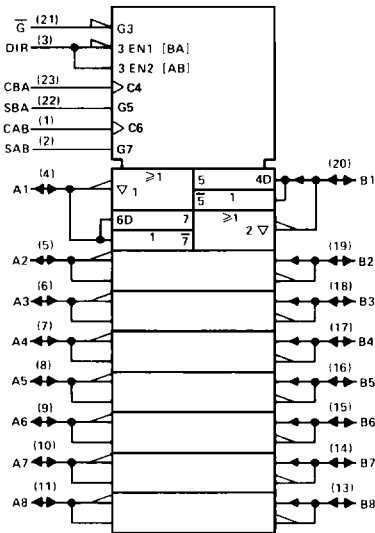
'ALS646, 'AS646



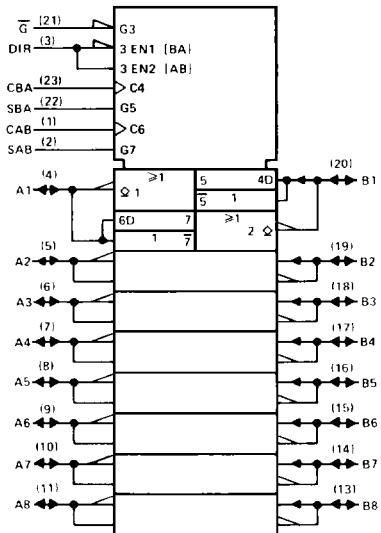
'ALS647



'ALS648, 'AS648



'ALS649



†These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

2 ALS and AS Circuits

SN54ALS646, SN74ALS646

OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage: Control inputs	7 V
I/O ports	5.5 V
Operating free-air temperature range: SN54ALS646	-55°C to 125°C
SN74ALS646	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS646			SN74ALS646			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
I_{OH}	High-level output current	-12			-15			mA
I_{OL}	Low-level output current	12			24			mA
					48 [†]			
f_{clock}	Clock frequency	0 to 35			0 to 40			MHz
t_w	Pulse duration, clocks high or low	14.5			12.5			ns
t_{su}	Setup time, A before CAB [†] or B before CBA [†]	15			10			ns
t_h	Hold time, A after CAB [†] or B after CBA [†]	0			0			ns
T_A	Operating free-air temperature	-55 to 125			0 to 70			°C

[†]The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS646-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS646			SN74ALS646			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5\text{ V}$, $I_I = -18\text{ mA}$	-1.2			-1.2			V
V_{OH}	$V_{CC} = 4.5\text{ V to }5.5\text{ V}$, $I_{OH} = -0.4\text{ mA}$	$V_{CC} \cdot 2$			$V_{CC} \cdot 2$			V
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -3\text{ mA}$	2.4 3.2			2.4 3.2			
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -12\text{ mA}$	2						
	$V_{CC} = 4.5\text{ V}$, $I_{OH} = -15\text{ mA}$				2			
V_{OL}	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 12\text{ mA}$	0.25 0.4			0.25 0.4			V
	$V_{CC} = 4.5\text{ V}$, $I_{OL} = 24\text{ mA}$				0.35 0.5			
	$I_{OL} = 48\text{ mA}$ for -1 version)							
I_I	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 7\text{ V}$			0.1			mA
	A or B ports	$V_{CC} = 5.5\text{ V}$, $V_I = 5.5\text{ V}$			0.1			
I_{IH}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 2.7\text{ V}$			20			μA
	A or B ports [§]				20			
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$, $V_I = 0.4\text{ V}$			-0.2			mA
	A or B ports [§]				-0.2			
I_O^*	$V_{CC} = 5.5\text{ V}$, $V_O = 2.25\text{ V}$	-30 to -112			-30 to -112			mA
I_{CC}	$V_{CC} = 5.5\text{ V}$	Outputs high	47 76		47 76		mA	
		Outputs low	55 88		55 88			
		Outputs disabled	55 88		55 88			

[‡]All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

*The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

SN54ALS646, SN74ALS646
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

†ALS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T _A = MIN to MAX			UNIT	
			ALS646			SN54ALS646		SN74ALS646		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}			50		35		40	MHz		
t _{PLH}	CBA or CAB	A or B	20	25	10	35	10	30	ns	
t _{PHL}			11	15	5	20	5	17		
t _{PLH}	A or B	B or A	11	17	5	22	5	20	ns	
t _{PHL}			7.5	10	3	15	3	12		
t _{PLH}	SBA or SAB† (with A or B low)	A or B	24	32	15	40	15	35	ns	
t _{PHL}			13	17	5	23	5	20		
t _{PLH}	SBA or SAB† (with A or B high)	A or B	17	22	8	30	8	25	ns	
t _{PHL}			13	17	5	24	5	20		
t _{PZH}	\bar{G}	A or B	10	15	3	20	3	17	ns	
t _{PZL}			10	15	5	22	5	20		
t _{PHZ}	\bar{G}	A or B	6	8	1	12	1	10	ns	
t _{PLZ}			10	13	2	20	2	16		
t _{PZH}	DIR	A or B	22	28	10	38	10	30	ns	
t _{PZL}			14.5	20	5	30	5	25		
t _{PHZ}	DIR	A or B	6	8	1	12	1	10	ns	
t _{PLZ}			10	13	2	21	2	16		

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

SN54ALS647, SN74ALS647 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS647	-55°C to 125°C
SN74ALS647	0°C to 70°C
Storage temperature range	-65°C to 150°C

recommended operating conditions

		SN54ALS647			SN74ALS647			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.7			V
V_{OH}	High-level output voltage				5.5			V
I_{OL}	Low-level output current				12			mA
					48†			
f_{clock}	Clock frequency	0			25			MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB† or B before CBA†	15			10			ns
t_h	Hold time, A after CAB† or B after CBA†	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

†The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS647-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54ALS647			SN74ALS647			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}		$V_{CC} = 4.5\text{ V}$,	$I_I = -18\text{ mA}$	-1.2			-1.2			V
I_{OH}		$V_{CC} = 4.5\text{ V}$,	$V_{OH} = 5.5\text{ V}$	0.1			0.1			mA
V_{OL}		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 12\text{ mA}$	0.25			0.4			V
		$V_{CC} = 4.5\text{ V}$,	$I_{OL} = 24\text{ mA}$ ($I_{OL} = 48\text{ mA}$ for -1 versions)				0.35 0.5			
I_I	A or B ports	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			mA
	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 7\text{ V}$	0.1			0.1			
I_{IH}	A or ports [§]	$V_{CC} = 5.5\text{ V}$,	$V_I = 2.7\text{ V}$	20			20			μA
	Control inputs			20			20			
I_{IL}	Control inputs	$V_{CC} = 5.5\text{ V}$,	$V_I = 0.4\text{ V}$	-0.2			-0.2			mA
	A or B ports [§]			-0.2			-0.2			
I_{CC}		$V_{CC} = 5.5\text{ V}$	Outputs high	35 60		35 60		mA		
			Outputs low	40 65		40 65				

‡All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

§For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

2
ALS and AS Circuits

SN54ALS647, SN74ALS647
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

'ALS647 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25°C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX			UNIT			
			'ALS647			SN54ALS647		SN74ALS647				
			MIN	TYP	MAX	MIN	MAX	MIN		MAX		
t _{max}			40			25		30		MHz		
t _{PLH}	CBA or CAB	A or B	38			50		19		72		ns
t _{PHL}			12			20		6		24		
t _{PLH}	A or B	B or A	35			39		17		70		ns
t _{PHL}			10			13		4		19		
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	40			51		20		72		ns
t _{PHL}			12			17		6		26		
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	40			51		20		72		ns
t _{PHL}			12			17		6		26		
t _{PLH}	\bar{G}	A or B	20			27		10		37		ns
t _{PHL}			10			15		2		20		
t _{PLH}	DIR	A or B	20			25		9		34		ns
t _{PHL}			13			17		2		22		

[†]These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

SN54ALS648, SN74ALS648 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

ALS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R ₁ = 500 Ω, R ₂ = 500 Ω, T _A = MIN to MAX			UNIT	
			'ALS648			SN54ALS648		SN74ALS648		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
f _{max}			50			35		40		MHz
t _{PLH}	CBA or CAB	A or B	21			8		39		ns
t _{PHL}			13			5		23		
t _{PLH}	A or B	B or A	10			3		20		ns
t _{PHL}			6			2		12		
t _{PLH}	SBA or SAB [†] (with A or B low)	A or B	24			5		44		ns
t _{PHL}			15			4		26		
t _{PLH}	SBA or SAB [†] (with A or B high)	A or B	16			6		30		ns
t _{PHL}			14			6		25		
t _{PZH}	\bar{G}	A or B	12			4		25		ns
t _{PZL}			12			4		25		
t _{PHZ}	\bar{G}	A or B	5			1		12		ns
t _{PLZ}			7			2		21		
t _{PZH}	DIR	A or B	14			4		35		ns
t _{PZL}			10			3		25		
t _{PHZ}	DIR	A or B	7			1		17		ns
t _{PLZ}			7			2		22		

[†] These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

SN54ALS649, SN74ALS649 OCTAL BUS TRANSCEIVERS AND REGISTERS WITH OPEN-COLLECTOR OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC}	7 V
Input voltage	7 V
Operating free-air temperature range: SN54ALS649	-55 °C to 125 °C
SN74ALS649	0 °C to 70 °C
Storage temperature range	-65 °C to 150 °C

recommended operating conditions

		SN54ALS649			SN74ALS649			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage				0.8			V
V_{OH}	High-level output voltage				5.5			V
I_{OL}	Low-level output current				24			mA
					48 [†]			
f_{clock}	Clock frequency	0			30			MHz
t_w	Pulse duration, clocks high or low	20			16.5			ns
t_{su}	Setup time, A before CAB [†] or B before CBA [†]	15			10			ns
t_h	Hold time, A after CAB [†] or B after CBA [†]	0			0			ns
T_A	Operating free-air temperature	-55			125			°C

[†]The extended condition applies if V_{CC} is maintained between 4.75 V and 5.25 V.
The 48-mA limit applies for the SN74ALS649-1 only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS649			SN74ALS649			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IK}	$V_{CC} = 4.5$ V, $I_I = -18$ mA	-1.2			-1.2			V
I_{OH}	$V_{CC} = 4.5$ V, $V_{OH} = 5.5$ V	0.1			0.1			mA
V_{OL}	$V_{CC} = 4.5$ V, $I_{OL} = 12$ mA	0.25			0.4			V
	$V_{CC} = 4.5$ V, $I_{OL} = 24$ mA ($I_{OL} = 48$ mA for -1 versions)				0.35			
I_I	A or B ports	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			mA
	Control inputs	$V_{CC} = 5.5$ V, $V_I = 7$ V			0.1			
I_{IH}	A or ports [§]	$V_{CC} = 5.5$ V, $V_I = 2.7$ V			20			μ A
	Control inputs				20			
I_{IL}	Control inputs	$V_{CC} = 5.5$ V, $V_I = 0.4$ V			-0.2			mA
	A or B ports [§]				-0.2			
I_{CC}	$V_{CC} = 5.5$ V	Outputs high	40	60	40	60	mA	
		Outputs low	45	70	45	70		

[‡]All typical values are at $V_{CC} = 5$ V, $T_A = 25$ °C

[§]For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

2
ALS and AS Circuits

SN54ALS649, SN74ALS649
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH OPEN-COLLECTOR OUTPUTS

ALS649 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 5 V, C _L = 50 pF, R _L = 680 Ω, T _A = 25 °C			V _{CC} = 4.5 V to 5.5 V, C _L = 50 pF, R _L = 680 Ω, T _A = MIN to MAX			UNIT							
			ALS649			SN54ALS649		SN74ALS649								
			MIN	TYP	MAX	MIN	MAX	MIN		MAX						
f _{max}			40			25		30		MHz						
t _{PLH}	CBA or CAB	A or B	40			19		77		19		62		ns		
t _{PHL}			12			18		6		22		6			20	
t _{PLH}	A or B	B or A	30			41		13		65		13		50		ns
t _{PHL}			6			9		2		11		2		10		
t _{PLH}	SBA or SAB† (with A or B low)	A or B	35			46		20		72		20		55		ns
t _{PHL}			15			21		6		26		6		22		
t _{PLH}	SBA or SAB† (with A or B high)	A or B	35			46		20		72		20		55		ns
t _{PHL}			15			21		6		26		6		22		
t _{PLH}	Z	A or B	16			22		8		28		8		25		ns
t _{PHL}			13			18		2		23		2		20		
t _{PLH}	DIR	A or B	16			22		8		28		8		25		ns
t _{PHL}			13			17		2		23		2		20		

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.

2 ALS and AS Circuits

SN54AS646, SN54AS648, SN74AS646, SN74AS648
OCTAL BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS

AS646 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS646		SN74AS646		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	11	2	9	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	\bar{G}	A or B	2	10	2	9	ns
t_{PZL}			3	15	3	14	
t_{PHZ}	\bar{G}	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

AS648 switching characteristics (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V,}$ $C_L = 50 \text{ pF,}$ $R_1 = 500 \Omega,$ $R_2 = 500 \Omega,$ $T_A = \text{MIN to MAX}$				UNIT
			SN54AS648		SN74AS648		
			MIN	MAX	MIN	MAX	
f_{max}			75		90		MHz
t_{PLH}	CBA or CAB	A or B	2	9.5	2	8.5	ns
t_{PHL}			2	10	2	9	
t_{PLH}	A or B	B or A	2	9	2	8	ns
t_{PHL}			1	8	1	7	
t_{PLH}	SBA or SAB†	A or B	2	12	2	11	ns
t_{PHL}			2	10	2	9	
t_{PZH}	\bar{G}	A or B	2	10	2	9	ns
t_{PZL}			3	18	3	15	
t_{PHZ}	\bar{G}	A or B	2	11	2	9	ns
t_{PLZ}			2	11	2	9	
t_{PZH}	DIR	A or B	3	19	3	16	ns
t_{PZL}			3	21	3	18	
t_{PHZ}	DIR	A or B	2	12	2	10	ns
t_{PLZ}			2	12	2	10	

† These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

NOTE 1: Load circuit and voltage waveforms are shown in Section 1.