GENERAL DESCRIPTION

The XRT72L71 DS3 ATM User Network Interface (UNI)/Clear-Channel Framer device is designed to function as either a DS3 ATM UNI or Clear channel framer IC. For ATM UNI applications, this device provides the ATM Physical Layer (Physical Medium Dependent and Transmission Convergence sub-layers) interface for the public and private networks at DS3 rates. For Clear-Channel framer applications, this device supports the transmission and reception of "user data" via the DS3 payload.

The XRT72L71 DS3 UNI for ATM incorporates Receive, Transmit, Microprocessor Interface, Performance Monitor, Test and Diagnostic and Line Interface Unit Scan Drive functional sections.

FEATURES

- Compliant with UTOPIA Level 1and 2 with 8 or 16 Bit Interface Specification and supports UTOPIA Bus operating at 25, 33 or 50 MHz
- Contains on-chip 16 cell FIFO (configurable in depths of 4, 8, 12 or 16 cells), in both the Transmit (TxFIFO) and Receive Directions (RxFIFO)
- Contains on-chip 54 byte transmit and Receive OAM Cell Buffers for transmission, reception, and processing of OAM Cells
- Supports PLCP or ATM Direct Mapping modes
- Supports M13 and C-Bit Parity Framing Formats
- Supports DS3 Clear Channel Framing Applications
- Includes PRBS Generator and Receiver
- Supports Line, Cell, and PLCP Loop-backs
- Interfaces to 8 or 16 Bit wide Motorola and Intel µPs and µCs
- Low power 3.3V, 5V tolerant, CMOS
- Available in 160 pin PQFP Package

APPLICATIONS

- Private User Network Interfaces
- ATM Switches
- ATM Routers and Bridges
- ATM Concentrators
- DS3 Frame Relay Equipment

FIGURE 1. BLOCK DIAGRAM OF THE XRT72L71 DS3 UNI IC

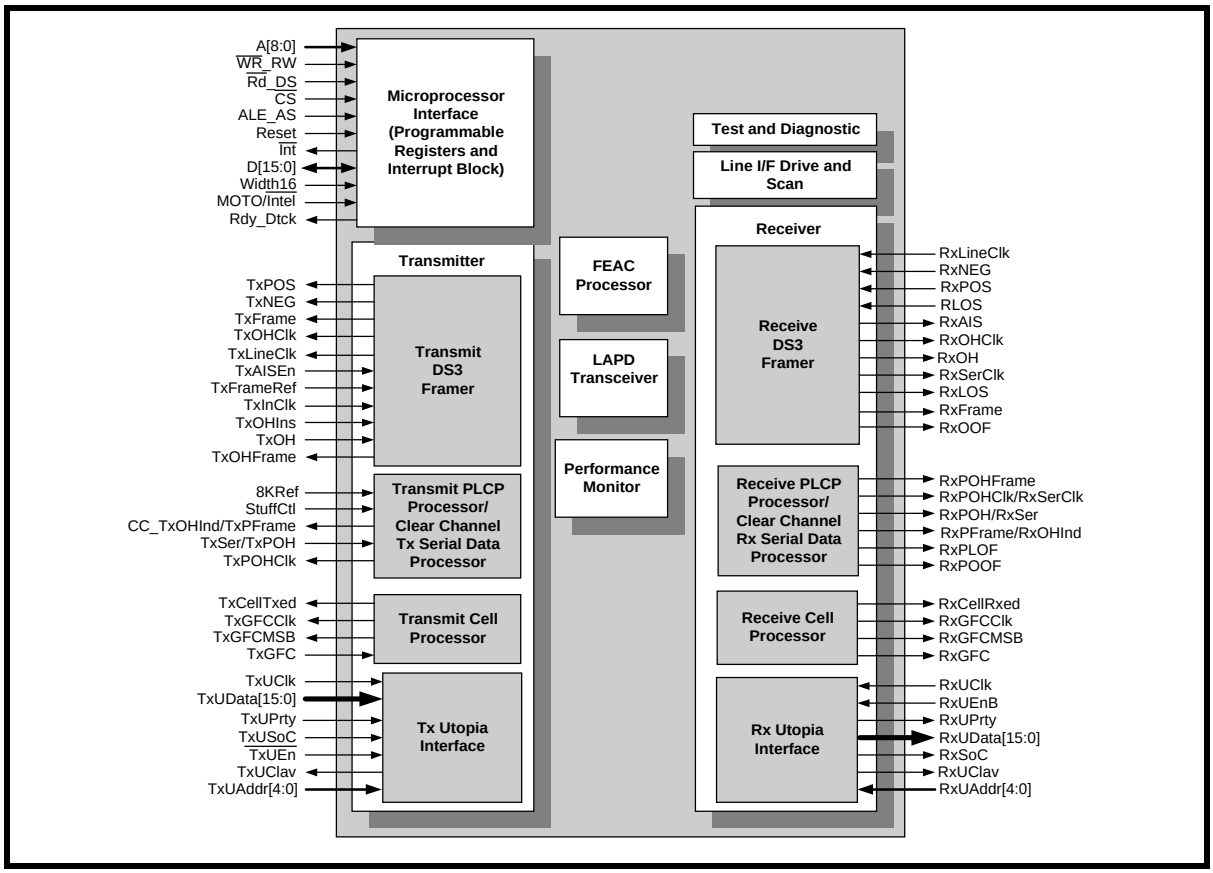
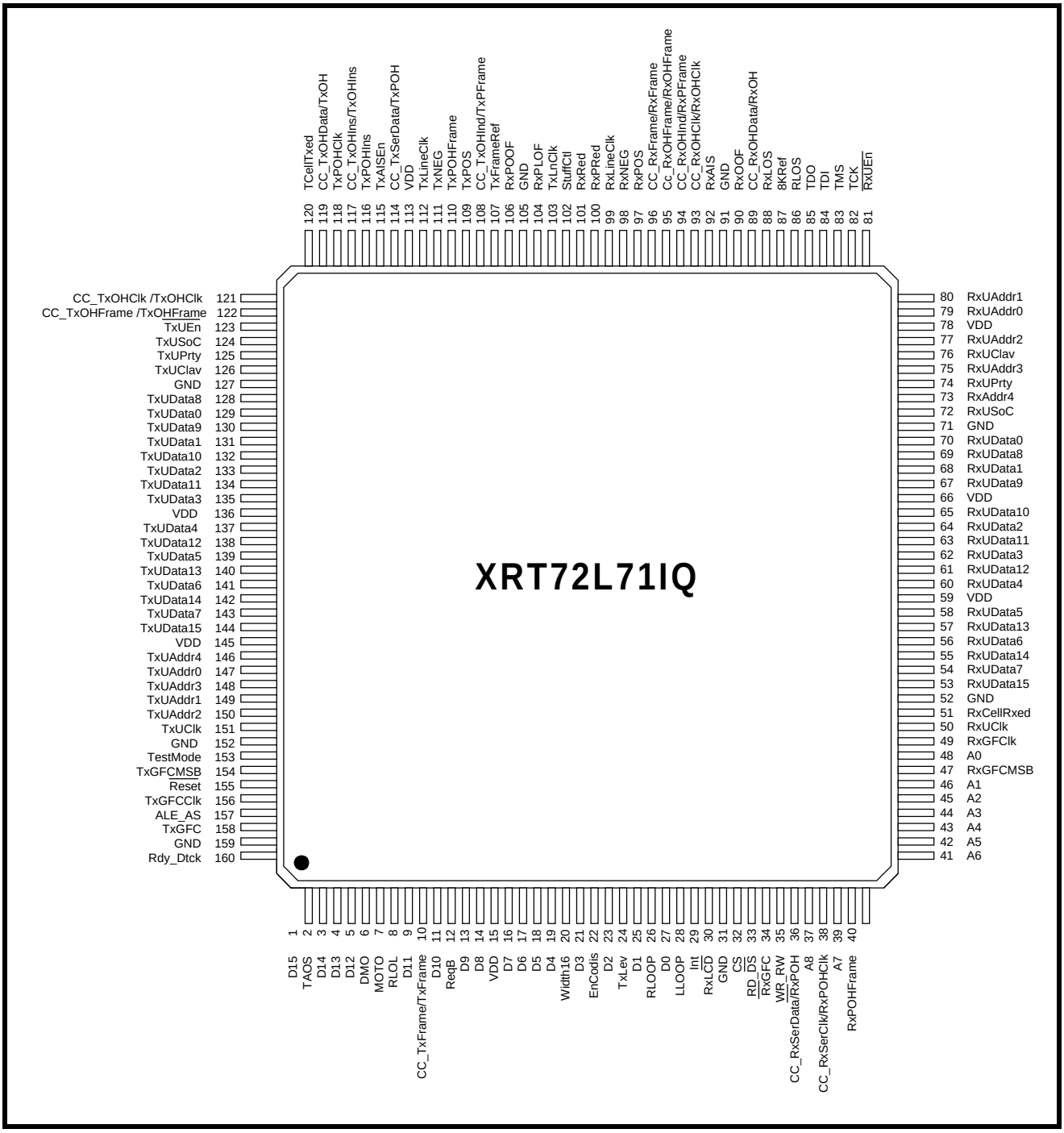


FIGURE 2. PIN OUT OF THE XRT72L71 DS3 ATM UNI



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L71IQ	160 PQFP	-40°C to +85°C

Pin Descriptions (see Figure 2)

PIN DESCRIPTION

PIN NO.	SYMBOL	TYPE	DESCRIPTION
1	D15	I/O	**MSB of Bi-Directional Data Bus (Microprocessor Interface Section):** This pin, along with pins D0 - D14, function as the Microprocessor Interface bi-directional data bus, and is intended to be interfaced to the “local” microprocessor. This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus.
2	TAOS	O	**“Transmit All Ones Signal” (TAOS) Command (for the XRT7300 LIU IC).** This output pin is intended to be connected to the TAOS input pin of the XRT7300 LIU IC. The user can control the state of this output pin by writing a ‘0’ or ‘1’ to Bit 4 (TAOS) of the Line Interface Drive Register (Address = 72h). If the user commands this signal to toggle "high" then it will force the XRT7300 DS3 Line Transmitter IC to transmit an "All Ones" pattern onto the line. Conversely, if the user commands this output signal to toggle "low" then the XRT7300 DS3 Line Transmitter IC will proceed to transmit data based upon the pattern that it receives via the TxPOS and TxNEG output pins. Writing a "1" to Bit 4 of the Line Interface Drive Register (Address = 72h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***NOTE:*** *If the customer is not using the XR-T7300 LIU IC, then he/she can use this output pin for a variety of other purposes.*
3	D14	I/O	**Bi-directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin1)
4	D13	I/O	**Bi-directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin 1)
5	D12	**I/O**	**Bi-directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin1)
6	DMO	I	**“Drive Monitor Output” Input (from the XRT7300 LIU IC):** This input pin is intended to be tied to the DMO output pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can determine the state of this input pin by reading Bit 2 (DMO) within the Line Interface Scan Register (Address = 73h). If this input signal is “high”, then it means that the drive monitor circuitry (within the XRT7300 LIU IC) has not detected any bipolar signals at the MTIP and MRING inputs within the last 128 ± 32 bit-periods. If this input signal is “low”, then it means that bipolar signals are being detected at the MTIP and MRING input pins of the XRT7300 device. ***NOTE:*** *If this customer is not using the XRT7300 E3/DS3/STS-1 LIU IC, then he/she can use this input pin for a variety of other purposes.*
7	MOTO/$\overline{\text{Intel}}$	I	**Motorola/Intel Processor Interface Select Mode:** This input pin allows the user to configure the Microprocessor Interface to interface with either a “Motorola-type” or “Intel-type” microprocessor/microcontroller. Tying this input pin to VCC, configures the microprocessor interface to operate in the Motorola mode (e.g., the UNI device can be readily interfaced to a “Motorola type” local microprocessor). Tying this input pin to GND configures the microprocessor interface to operate in the Intel Mode (e.g., the UNI device can be readily interfaced to an “Intel type” local microprocessor).

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
8	RLOL	I	**Receive Loss of Lock Indicator—from the XRT7300 E3/DS3/STS-1 LIU IC:** This input pin is intended to be connected to the RLOL (Receive Loss of Lock) output pin of the XRT7300 LIU IC. The user can monitor the state of this pin by reading the state of Bit 1 (RLOL) within the Line Interface Scan Register (Address = 73h). If this input pin is "low", then it means that the phase-locked-loop circuitry, within the XRT7300 device is properly locked onto the incoming DS3 data-stream; and is properly recovering clock and data from this DS3 data-stream. However, if this input pin is "high", then it means that the phase-locked-loop circuitry, within the XRT7300 device has lost lock with the incoming DS3 data-stream, and is not properly recovering clock and data. For more information on the operation of the XRT7300 E3/DS3/STS-1 LIU IC, please consult the "XRT7300 E3/DS3/STS-1 LIU IC" data sheet. ***NOTE:*** *If the customer is not using the XRT7300 LIU IC, he/she can use this input pin for other purposes.*
9	D11	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):**
10	TxFrame	O	**Transmit End of DS3 Frame Indicator:** The function of this pin is same in both Clear Channel and ATM UNI modes of the XRT72L71. This pin marks the end of each DS3 frame. **ATM UNI Mode** This pin is pulsed for one DS3 clock period when the transmit input interface is processing the last bit of the given DS3 frame. This just serves as an indication to terminal equpiment in the ATM UNI mode. **Clear Channel Mode** In Clear channel mode this pulse is to alert the terminal equipment to begin transmission of a new frame at the next clock. When the external interface samples this pin high, it should provide the 'X' bit on TxSer pin if XRT72L71 is configured to accept the OH data from TxSer input. Any paylod data provided at this time will be ignored.
11	D10	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin1)
12	$\overline{\text{Req}}$	O	**Receive Equalization Bypass Control Output Pin—(to be connected to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the REQB input pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a '0' or '1' to Bit 5 (REQB) of the Line Interface Driver Register (Address = 72h). If the user commands this signal to toggle "high" then it will cause the incoming DS3 line signal to "bypass" equalization circuitry, within the XRT7300 Device. Conversely, if the user commands this output signal to toggle "low", then the incoming DS3 line signal with be routed through the equalization circuitry. For information on the criteria that should be used when deciding whether to bypass the equalization circuitry or not, please consult the "XRT7300 E3/DS3/STS-1 LIU IC" data sheet. Writing a "1" to Bit 5 of the Line Interface Drive Register (Address = 72h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***NOTE:*** *If the customer is not using the XRT7300 E3/DS3/STS-1 LIU IC, then he/she can use this output pin for a variety of other purposes.*
13	D9	I/O	**Bi-Directional Data bus (Microprocessor Interface Section): T**his pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin1)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
14	D8	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** This pin is inactive if the Microprocessor Interface block is configured to operate over an 8 bit data bus. (Please see description for D15, pin1)
15	VDD	***	**Power Supply Pin**
16	D7	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
17	D6	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
18	D5	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
19	D4	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
20	Width16	I	**Microprocessor Interface Block Data Bus Width Selector:** This input pin allows the user to configure the microprocessor interface of the UNI, to operate over either an 8 or 16 bit wide data bus. Tying this pin to VCC configures the Microprocessor Interface Data Bus width to be 16 bits. Tying this pin to GND configures the Microprocessor Interface Data Bus width to be 8 bits.
21	D3	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
22	Encodis	O	**Encoder (B3ZS) Disable Output pin (intended to be connected to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the Encodis input pin of the XRT7300 LIU IC. The user can control the state of this output pin by writing a “0” or “1” to Bit 3 (Encodis) of the Line Interface Driver Register (Address = 72h). If the user commands this signal to toggle “high” then it will disable the B3ZS encoder circuitry within the XRT7300 IC. Conversely, if the user commands this output signal to toggle “low”, then the B3ZS Encoder circuitry, within the XRT7300 IC will be enabled. Writing a “1” to Bit 3 of the Line Interface Driver Register (Address = 72h) will cause this output pin to toggle “high”. Writing a “0” to this bit-field will cause this output pin to toggle “low”. ***NOTES:*** 1. *The user is advised to disable the B3ZS encoder (within the XRT7300 IC) if the Transmit and Receive DS3 Framers (within the UNI) are configured to operate in the B3ZS line code.* 2. *If the customer is not using the XRT7300 DS3 Line Transmitter IC, then he/she can use this output pin for a variety of other purposes.*
23	D2	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
24	TxLev	O	**Transmit Line Build Enable/Disable Select (to be connected to the TxLev input pin of the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the TxLev input pin of the XRT7300 E3/DS3/STS-1 LIU IC. The user can control the state of this output pin by writing a "0" or a "1" to Bit 2 (TxLev) within the Line Interface Driver Register (Address = 72h). If the user commands this signal to toggle "high" then it will disable the "Transmit Line Build-Out" circuitry within the XRT7300 device. In this case, the XRT7300 device will output unshaped (square-wave) pulses onto the "Transmit Line Signal". In order to insure that the XRT7300 device generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the Cross-Connect), the user is advised to set this output pin high, if the cable length (between the Transmit Output of the XRT7300 device and the Cross-Connect) is greater than 225 feet. Conversely, if the user commands this signal to toggle "high", then it will enable the "Transmit Line Build-Out" circuitry within the XRT7300 device. In this case, the XRT7300 device will output shaped pulses onto the "Transmit Line Signal". In order to ensure that the XRT7300 device generates a line signal that is compliant with the Bellcore GR-499-CORE Pulse Template requirements (at the Cross-Connect), the user is advised to set this output pin low, if the cable length (between the Transmit Output of the XRT7300 device and the Cross Connect) is less than 225 ft. of cable. Writing a "1" to Bit 2 of the Line Interface Drive Register (Address = 72h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause this output pin to toggle "low". ***NOTE:*** *If the customer is not using the XRT7300 E3/DS3/STS-1 LIU IC, then he/she can use this output pin for a variety of other purposes.*
25	D1	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)
26	RLOOP	O	**Remote Loop-back Output Pin (to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the RLOOP input pin of the XRT7300 LIU IC. The user can command this signal to toggle "high" and, in turn, force the XRT7300 into the "Remote Loop-back" mode. Conversely, the user can command this signal to toggle "low" and allow the XRT7300 device to operate in the normal mode. (For a detailed description of the XRT7300 LIU IC's operation during Remote Loop-back, please see the XRT7300 E3/DS3/STS-1 LIU IC Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register (Address = 72h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". ***NOTE:*** *If the customer is not using the XRT7300 E3/DS3/STS-1 IC, then he/she can use this output pin for a variety of other purposes.*
27	D0	I/O	**Bi-Directional Data bus (Microprocessor Interface Section):** (Please see description for D15, pin1)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
28	LLOOP	O	**Local Loop-back Output Pin (to the XRT7300 E3/DS3/STS-1 LIU IC):** This output pin is intended to be connected to the LLOOP input pin of the XRT7300 LIU IC. The user can command this signal to toggle "high" and, in turn, force the LIU into the "Local Loop-back" mode. (For a detailed description of the XRT7300 LIU IC's operation during Local Loop-back, please see the XRT7300 E3/DS3/STS-1 LIU IC Data Sheet). Writing a "1" to bit 1 of the "Line Interface Drive Register" (Address = 72h) will cause this output pin to toggle "high". Writing a "0" to this bit-field will cause the RLOOP output to toggle "low". ***NOTE:*** *If the user is not using the XRT7300 E3/DS3/STS-1 LIU IC, then he/she can use this output pin for a variety of other purposes.*
29	$\overline{\text{Int}}$	O	**Interrupt Request Output:** This open-drain, active-low output signal will be asserted when the UNI device is requesting interrupt service from the local microprocessor. This output pin should typically be connected to the "Interrupt Request" input of the local microprocessor.
30	RxLCD	O	**Loss of Cell Delineation Indicator:** This active-high output pin will be asserted whenever the Receive Cell Processor has experienced a "Loss of Cell Delineation". This pin will return "low" once the Receive Cell Processor has regained Cell Delineation.
31	GND	***	**Ground Pin Signal**
32	$\overline{\text{CS}}$	I	**Chip Select Input:** This active-low input signal selects the Microprocessor Interface Section of the UNI device and enables Read/Write operations between the "local" microprocessor and the UNI on-chip registers and RAM locations.
33	RDB_DS	I	**Read Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this input will function as the RD* (READ STROBE) input signal from the local µP. Once this active low signal is asserted, then the UNI will place the contents of the addressed registers (within the UNI) on the Microprocessor Data Bus (D[15:0]). When this signal is negated, the Data Bus will be tri-stated. **Data Strobe (Motorola Mode):** If the microprocessor interface is operating in the Motorola mode, then this pin will function as the active low Data Strobe signal.
34	RxGFC	O	**Receive GFC Nibble Field Serial Output pin:** This pin, along with the RxGFCClk and the RxGFCMSB pins form the "Receive GFC Nibble-Field" serial output port. This pin will serially output the contents of the GFC Nibble field of each cell that is processed through the Receive Cell Processor. This data is serially clocked out of this pin on the rising edge of the RxGFCClk signal. The Most Significant Bit (MSB) of each GFC value is designated by a pulse at the RxGFCMSB output pin.
35	$\overline{\text{WR}}$_RW	I	**Write Data Strobe (Intel Mode):** If the microprocessor interface is operating in the Intel Mode, then this active low input pin functions as the WR* (Write Strobe) input signal from the µP. Once this active-low signal is asserted, then the UNI will latch the contents of the µP Data Bus, into the addressed register (or RAM location) within the UNI IC. **R/W Input Pin (Motorola Mode):** When the Microprocessor Interface Section is operating in the "Motorola Mode", then this pin is functionally equivalent to the "R/W*" pin. In the Motorola Mode, a "READ" operation occurs if this pin is at a logic "1". Similarly, a WRITE operation occurs if this pin is at a logic "0".

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
36	RxSerData/ RxPOH	O	**Receive Serial Output/Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Pin:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, the DS3 frame received by XRT72L71 is sent out as serial data stream on this pin. This data can be sampled with the rising edge of RxClkOut. **ATM UNI Mode:** This output pin, along with RxPOHClk, RxPOHFrame, and RxPOHIns pins comprise the “Receive PLCP Frame POH Byte” serial output port. For each PLCP frame that is received by the Receive PLCP Processor, this serial output port will output the contents of all 12 POH (Path Overhead) bytes. The data that is output via this pin, is updated on the rising edge of the RxPOHClk output clock signal. The RxPOHFrame pin will pulse “high” when the first bit of the Z6 byte is being output on this output pin.
37	A8	I	**Address Bus Input (Microprocessor Interface)—MSB (Most Significant Bit):** This input pin, along with inputs A0 - A7 are used to select the on-chip UNI register and RAM space for READ/WRITE operations with the “local” microprocessor.
38	RxSerClk/ RxPOHClk	O	**Clear Channel Mode Receive Clock Output Signal for Serial Data Interface/ Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Output Clock Signal:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, this pin can be used by the external interface to sample the clear channel serial data stream on RxSer pin. The serial data should be sampled on the rising edge of this clock. **ATM UNI MODE:** In the ATM UNI mode of operation, this pin serves as RxPOHClk. This output clock pin, along with RxPOH, RxPOHframe pins comprise the 'Receive PLCP OH serial output' interface.
39	A7	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
40	RxPOHFrame	O	**Receive PLCP Frame Path Overhead (POH) Byte Serial Output Port—Beginning of Frame Signal Pin:** This output pin, along with RxPOH, RxPOHClk, and RxPOHIns pins comprise the “Receive PLCP Frame POH Byte” serial output port. This output pin provides framing information to external circuitry receiving and processing this POH (Path Overhead) data, by pulsing “high” when the first bit of the Z6 byte is output via the RxPOH output pin. This pin is “low” at all other times during this PLCP POH framing cycle.
41	A6	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
42	A5	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
43	A4	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
44	A3	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
45	A2	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
46	A1	I	**Address Bus Input (Microprocessor Interface):** (Please see description for A8)
47	RxGFCMSB	O	**Received GFC Nibble Field—MSB Indicator**: This output pin functions as a part of the "Receive GFC-Nibble Field" Serial Output port; which also consists of the RxGFC and RxGFCClk pins. This pin pulses "high" the instant that the MSB (Most Significant Bit) of a GFC Nibble is being output on the RxGFC pin.
48	A0	I	**Address Bus Input (Microprocessor Interface)—LSB (Least Significant Bit):** (Please see description for A8)
49	RxGFClk	O	**Received GFC Nibble Serial Output Port Clock Signal:** This output pin functions as a part of the "Receive GFC Nibble-Field" Serial Output Port; also consisting of the RxGFC and RxGFCMSB pins. This pin provides a clock pulse which allows external circuitry to latch in the GFC Nibble-Data via the RxGFC output pin.
50	RxUClk	I	**Receive UTOPIA Interface Clock Input:** The byte (or word) data, on the Receive UTOPIA Data bus is updated on the rising edge of this signal. The Receive UTOPIA Interface can be clocked at rates up to 50 MHz.
51	RxCellRxed	O	**Receive Cell Processor—Cell Received Indicator:** This output pin pulses "high" each time the Receive Cell Processor receives a new cell from the Receive PLCP Processor or the Receive DS3 Framer.
52	GND	***	**Ground Pin Signal**
53	RxUData15	O	**Receive UTOPIA Data Bus Output (MSB):** This output pin, along with RxUData14 through RxUData0 functions as the Receive UTOPIA Data Bus. ATM cell data that has been received from the "Far-End" UNI is output on the Receive UTOPIA Data Bus, where it can be read and processed by the ATM Layer Processor.
54	RxUData7	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
55	RxUData14	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
56	RxUData6	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
57	RxUData13	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
58	RxUData5	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
59	VDD	***	**Power Supply Pin**
60	RxUData4	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
61	RxUData12	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
62	RxUData3	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
63	RxUData11	O	**Receive UTOPIA Data Bus Output:See description of RxUData15 pin 53.**
64	RxUData2	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
65	RxUData10	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
66	VDD	***	**Power Supply Pin**
67	RxUData9	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
68	RxUData1	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
69	RxUData8	O	**Receive UTOPIA Data Bus Output:** See description of RxUData15 pin 53.
70	RxUData0	O	**Receive UTOPIA Data Bus Output—LSB:** See description of RxUData15 pin 53.
71	GND	***	**Ground Signal Pin**
72	RxUSoC	O	**Receive UTOPIA Interface—Start of Cell Indicator:** This output pin allows the ATM Layer Processor to determine the boundaries or the ATM cells that are output via the Receive UTOPIA Data bus. The Receive UTOPIA Interface block will assert this signal when the first byte (or word) of a new cell is present on the Receive UTOPIA Data Bus; RxUData[15:0].
73	RxUAddr4	I	**Receive UTOPIA Address Bus input (MSB):** This input pin, along with RxUAddr3 through RxUAddr0 functions as the Receive UTOPIA Address bus inputs. These input pins are only active when the UNI device is operating in the Multi-PHY Mode. The Receive UTOPIA Address Bus input is sampled on the rising edge of the RxUClk signal. The contents of this address bus are compared with the value stored in the "Rx UT Address Register (Address = 6Ch). If these two values match, then the UNI will inform the ATM Layer Processor on whether or not it has any new ATM cells to be read from the RxFIFO; by driving the RxUClav output to the appropriate level. If these two address values do not match, then the UNI will not respond to the ATM Layer Processor; and will keep its RxUClav output signal tri-stated.
74	RxUPrty	O	**Receive UTOPIA Interface—Parity Output pin:** The Receive UTOPIA interface block will compute the odd-parity of each byte (or word) that will place in the Receive UTOPIA Data Bus. This odd-parity value will be output on this pin, while the corresponding byte (or word) is present on the Receive UTOPIA Data Bus.
75	RxUAddr3	I	**Receive UTOPIA Address Bus input:** (See Description for RxUAddr4 pin 73)
76	RxUClav	O	**Receive UTOPIA—Cell Available:** The Receive UTOPIA Interface block will assert this output pin in order to indicate that the Rx FIFO has some ATM cell data that needs to be read by the ATM Layer Processor. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshake mode. **Octet Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "octet-level handshaking" mode; this signal is asserted (toggles "high") when at least one byte of cell data exists within the RxFIFO (within the Receive UTOPIA Interface block). This output pin will toggle "low" if the RxFIFO is depleted of ATM cell data. **Cell Level Handshaking Mode** When the Receive UTOPIA Interface block is operating in the "cell-level handshaking" mode; this signal is asserted if the RxFIFO contains at least one full cell of data. This signal will toggle "low" if the RxFIFO is depleted of data, or if it contains less than one full cell of data. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the RxUClk cycle following the assertion of a valid address on the Receive UTOPIA Address bus input pins (e.g., if the contents on the Receive UTOPIA Address bus pins match that with the Receive UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode.
77	RxUAddr2	I	**Receive UTOPIA Address Bus input:** (See Description for RxUAddr4 pin 73)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
78	VDD	****	**Power Supply Pin**
79	RxUAddr0	I	**Receive UTOPIA Address Bus input—LSB:** (See Description for RxUAddr4 pin 73)
80	RxUAddr1	I	**Receive UTOPIA Address Bus input:** (See Description for RxUAddr4 pin 73)
81	$\overline{\text{RxUEn}}$	I	**Receive UTOPIA Interface—Output Enable:** This active-low input signal is used to control the drivers of the Receive UTOPIA Data Bus. When this signal is “high” (negated) then the Receive UTOPIA Data Bus is tri-stated. When this signal is asserted, then the contents of the byte or word that is at the “front of the RxFIFO” will be “popped” and placed on the Receive UTOPIA Data bus on the very next rising edge of RxUClk.
82	TCK	I	**Test Clock:** Boundry Scan clock input.
83	TMS	I	**Test Mode Select:** Boundry Scan Mode Select input.
84	TDI	I	**Test Data In:** Boundry Scan Test data input.
85	TDO	O	**Test Data Out:** Boundry Scan test data output.
86	RLOS	I	**Receive LOS (Loss of Signal) Indicator Input (from XRT7300 E3/DS3/ STS-1 Line Interface Unit).** This input pin is intended to be connected to the RLOS (Receive Loss of Signal) output pin of the XRT7300 E3/DS3 /STS-1 Line Interface IC. The user can monitor the state of this pin by reading the state of Bit 0 (RLOS) within the Line Interface Scan Register (Address = 73h). If this input pin is “low”, then it means that the XRT7300 device is detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream. However, if this input pin is “high”, then it means that the XRT7300 device is not detecting a sufficient amount of signal energy on the line, due to the incoming DS3 data-stream, and may be experiencing a “Loss of Signal” condition. For more information on the operation of the XRT7300 E3/DS3/STS-1 Line Interface Unit IC, please consult the “XRT7300 ” data sheet. ***NOTE:*** *Asserting the RLOS input pin will cause the XRT72L71 DS3 UNI device to declare an “LOS” (Loss of Signal) condition. Therefore, this input pin should not be used as a general purpose input.*
87	8KRef	I	**8 kHz Reference Clock Input for the PLCP Processors:** The Transmit PLCP processor can be configured to synchronize its PLCP frame processing to this clock signal. The Transmit PLCP Processor will also use this signal to compute the trailer nibble stuff opportunities. ***NOTE:*** *This input signal is active only if the user has configured the PLCP Processors to use this signal as their “master clock” signal. The user can configure the UNI to use this signal by setting TimRefSel[1,0] (within the UNI Operating Mode Register) to 01.*
88	RxLOS	O	**Receive DS3 Framer—Loss of Signal Output Indicator:** This pin is asserted when the Receive DS3 Framer encounters 180 consecutive 0’s via the RxPOS and RxNEG pins. This pin will be negated once the Receive DS3 Framer has detected at least 60 “1s” out of 180 consecutive bits.
89	RxOH	O	**Receive Overhead Output Port** All overhead bits, which are received via the "Receive Section" of the Framer IC; will be output via this output pin, upon the rising edge of RxOHClk.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
90	RxOOF	O	**Receiver DS3 Framer—"Out of Frame" Indicator:** The UNI Receive DS3 Framer will assert this output signal whenever it has declared an "Out of Frame" (OOF) condition with the incoming DS3 frames. This signal is negated when the framer correctly locates the F- and M-bits and regains synchronization with the DS3 frame.
91	GND	***	**Ground Signal Pin**
92	RxAIS	O	**Receive "Alarm Indication Signal" Output pin:** The UNI will assert this pin to indicate that the Alarm Indication Signal (AIS) has been identified in the Receive DS3 data stream. An "AIS" is detected if the payload consists of the recurring pattern of 1010... and this pattern persists for 63 M-frames. An additional requirement for AIS indication is that the C-bits are set to 0, and the X-bits are set to 1. This pin will be negated when a sufficient number of frames, not exhibiting the "1010..." pattern in the payload has been detected. For more details, please see Section _.
93	RxOHClk	O	**Receive Overhead Output Clock Signal:** This pin serves as the clock signal for external device to sample the Overhead data on the RxOH pin. The external interface should use the rising edge of this clock to sample the OH data on RxOH pin.
94	RxOHInd/ RxPFrame	O	**Receive Overhead Bit Indicator/PLCP Frame Boundary Indicator Output—Receive PLCP Processor.** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, this pin is pulsed high for one bit period whenever an OH bit is being output on the RxSer pin. In other words, RxSer will contain OH if this pin is sampled high. **ATM UnI Mode:** This output pin pulses "high" when the Receive PLCP Processor is receiving the last bit of a PLCP frame.
95	RxOHFrame	O	**Receive Overhead Frame Boundary Indicator:** This pin is pulsed high for one RxOHClk period whenever the first 'X' bit is output on RxOH pin. If external device samples this pin high on the rising edge of RxOHClk, the data on RxOH is 'X' bit (first OH bit in the received DS3 frame).
96	RxFrame	O	**Receive Boundary of DS3 Frame Output Indicator:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode this pin is pulsed high for one DS3 clock period whenever the 'X' bit (first OH bit in the DS3 frame) of the frame is being output on the RxSer pin. RxSer will contain 'X' bit (first OH bit of DS3 frame) if this pin is sampled high. **ATM UNI Mode:** In the ATM UNI mode, this signal indicates the start of the received DS3 frame and is high for one DS3 clock period.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
97	RxPOS	I	**Receive Positive Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin functions as the "Single-Rail" input for the "incoming" DS3 data stream. The signal at this input pin will be sampled and latched (into the Receive DS3 Framer) on the "user-selected" edge of the RxLineClk signal. **Bipolar Mode:** This input functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxNEG functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a "positive polarity" pulse from the line.
98	RxNEG	I	**Receive Negative Data Input:** The exact role of this input pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This input pin is inactive, and should be pulled ("low" or "high") when the UNI is operating in the Unipolar Mode. **Bipolar Mode:** This input pin functions as one of the dual rail inputs for the incoming AMI/B3ZS encoded DS3 data that has been received from an external Line Interface Unit (LIU) IC. RxPOS functions as the other dual rail input for the UNI. When this input pin is asserted, it means that the LIU has received a "negative polarity" pulse from the line.
99A2	RxLineClk_0	I	**Receiver LIU (Recovered) Clock:** This input signal serves three purposes: 1. The Receive DS3 Framer uses it to sample and "latch" the signals at the RxPOS and RxNEG input pins (into the Receive DS3 Framer circuitry). 2. This input signal functions as the timing reference for the Receive Framer block. 3. The Transmit DS3 Framer block can be configured to use this input signal as its timing reference. **Note:** This signal is the recovered clock from the external DS3 LIU (Line Interface Unit) IC, which is derived from the incoming DS3 data.
100	RxPRed	O	**Receiver Red Alarm Indicator—Receive PLCP Processor:** The UNI asserts this output pin to denote that one of the following events has been detected by the Receive PLCP Processor: • OOF—Out of Frame Condition • LOF—Loss of Frame Condition
101	RxRed	O	**Receiver Red Alarm Indicator—Receive DS3 Framer:** The UNI asserts this output pin to denote that one of the following events has been detected by the Receive DS3 Framer: • LOS—Loss of Signal Condition • OOF—Out of Frame Condition • AIS—Alarm Indication Signal Detection
102	StuffCtl	I	**External PLCP Frame Stuff Control:** This input allows the user to externally exercise or forego trailer nibble stuffing opportunities by the Transmit PLCP Processor. PLCP trailer nibble stuff opportunities occur in periods of three PLCP frames (375µs). The first PLCP frame (first within a "stuff opportunity" period) will have 13 trailer nibbles appended to it. The second PLCP frame (second within a "stuff opportunity" period) will have 14 trailer nibbles appended to it. The third PLCP frame (the location of the stuff opportunity) will contain 13 trailer nibbles if the StuffCtl input is "low" and 14 trailer nibbles is the StuffCtl input is "high".

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
103	TxlineClk	I	**Transmit DS3 Framer—Clock Signal:** The Transmit DS3 Framer can be configured to use this input signal as the timing reference. If this input pin is chosen to be the timing reference, then the user must supply a high quality 44.736 MHz signal to this input pin. In this configuration, frame generation, by the Transmit DS3 Framer, will be asynchronous (with any other timing signals within the UNI). However, frame timing will be based upon this clock signal. ***NOTE:*** *This input pin should be tied to "GND" if it is not used as the Transmit DS3 Framer timing reference.*
104	RxPLOF	O	**Receive PLCP—"Loss of Frame" Output Indicator:** The Receive PLCP Processor will assert this pin, when it declares a "Loss of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition.
105	GND	***	**Ground Signal Pin**
106	RxPOOF	O	**Receive PLCP "Out of Frame" Indicator:** The Receive PLCP Processor will assert this pin, when it declares an "Out of Frame" condition. This output will be negated when the Receive PLCP Processor reaches the "In Frame" Condition.
107	TxFrameRef	I	**Transmit DS3 Framer—Frame Reference Input Pin:** The Transmit DS3 Framer can be configured to use this input signal as the "framing" reference for the Transmit DS3 Framer block. If this input pin is chosen to be the timing reference, then any rising edge at this input will cause the Transmit DS3 Framer to begin its creation a new DS3 M-frame. Consequently, the user must supply a clock signal that is equivalent to the DS3 Frame rate (or 9398.3 Hz). ***NOTE:*** *This input pin should be tied to "GND" if it is not used as the Transmit DS3 Framer frame reference signal.*
108	CC_TxOHInd/ TxPFrame	O	**Transmit Overhead Data Indicator/Transmit PLCP Frame Boundary Indicator—Output:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In the Clear Channel Mode, this pin serves as the transmit OH Indication for the external interface. This pin is pulsed for one bit period of DS3 clock to indicate to the external device that the transmit input interface is going to process OH data at the rising edge of next clock. When the external interface samples TxOHInd as high With the rising edge of DS3 Clk; it is expected NOT to provide useful payload data bit on TxSer pin. Instead it can provide corresponding OH data bit on TxSer input. However, in that case the user has to program a register bit to configure XRT72L71 to accept the OH data from the TxSer input. Otherwise, the OH data will be geaerated internally or be taken from the TxOH pin if TxOHIns is high. This pin is pulsed high for one bit period prior to all DS3 OH bit positions. **ATM UNI Mode:** In ATM UNI mode of operation, this pin functions as Transmit PLCP Frame signal which pulses high once for each outbound PLCP frame, when the last nibble is being routed.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
109	TxPOS	O	**Transmit Positive Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output pin functions as the "Single-Rail" output signal for the "outbound" DS3 data stream. The signal, at this output pin, will be updated on the "user-selected" edge of the TxLineClk signal. **Bipolar Mode:** This output pin functions as one of the two dual rail output signals that commands the sequence of pulses to be driven on the line. TxNEG is the other output pin. This input is typically connected to the TPDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a positive polarity pulse on the line.
110	TxPOHFrame	O	**Transmit PLCP Frame Path Overhead Byte Serial Input Port—Beginning of Frame indicator.** This output pin, along with the TxPOH, TxPOHClk, and TxPOHIns pins comprise the "Transmit PLCP Frame POH Byte Insertion" serial input port. This particular pin will pulse "high" when the "Transmit PLCP POH Byte Insertion" serial input port is expecting the first bit of the Z6 byte at the TxPOH input pin.
111	TxNEG	O	**Transmit Negative Polarity Pulse:** The exact role of this output pin depends upon whether the UNI is operating in the Unipolar or Bipolar Mode. **Unipolar Mode:** This output signal pulses "high" for one bit period, at the end of each "outbound" DS3 frame. This output signal is at a logic "low" for all of the remaining bit-periods of the "outbound" DS3 frames. **Bipolar Mode:** This output pin functions as one of the two dual-rail output signals that commands the sequence of pulses to be driven on the line. TxPOS is the other output pin. This input is typically connected to the TNDATA input of the external DS3 Line Interface Unit IC. When this output is asserted, it will command the LIU to generate a negative polarity pulse on the line.
112	TxLineClk	O	**Transmit Line Interface Clock:** This clock signal is output to the Line Interface Unit, along with the TxPOS and TxNEG signals. The purpose of this output clock signal is to provide the LIU with timing information that it can use to generate the AMI pulses and deliver them over the transmission medium to the Far-End Receiver. The user can configure the source of this clock to be either the RxLineClk (from the Receiver portion of the UNI) or the TxlineClk input. The nominal frequency of this clock signal is 44.736 MHz.
113	VDD	***	**Power Supply Pin**
114	TxSer/ TxPOH	I	**Transmit Serial Payload Data Input/Transmit PLCP Frame POH Byte Insertion Serial Input:** The exact functionality of this output pin depends upon whether the XRT72L71 Framer IC is operating in the Clear Channel or ATM Uni Mode. **Clear Channel Mode:** In clear channel mode, this pin can be used by the external interface to provide the serial input data (payload and OH) that has to be mapped in outgoing DS3 frame. If user want to insert OH data on TxSer pin then the user should configure the XRT72L71 accordingly. **ATM UNI Mode:** This input pin becomes active when the user asserts the TxPOHIns input pin. When this happens the user will be permitted to serially input their own value for PLCP POH bytes into the "outbound" PLCP frame. This data will be clocked into the UNI device via the TxPOHClk output signal. This UNI will also assert the TxPOHMSB output pin when it expects the MSB (Most significant bit) of the Z6 Byte (within the PLCP frame).
115	TxAISEn	I	**Transmit AIS Pattern input:** When this input pin is set "high" the Transmit DS3 Framer will insert the AIS pattern into the DS3 output data stream.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
116	TxPOHIns	I	**Transmit PLCP Frame POH Data Insert Enable:** This input can be asserted to allow the user to input his/her own value for the PLCP POH bytes via the TxPOH input pin, in each PLCP frame, prior to transmission. If this input pin is not asserted, then the UNI will generate its own PLCP POH bytes.
117	TxOHIns	I	**Transmit Overhead Data Insert Input:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L71. This pin is used to indicate if the OH bit should be taken from the external interface. The OH data on TxOH will be considered by the device only if this pin is high during OH positions.
118	TxPOHClk	O	**Transmit PLCP Frame POH Byte Insertion Clock:** This pin, along with the TxPOH and the TxPOHMSB input pins, function as the “Transmit PLCP Frame POH Byte” serial input port. This output pin functions as a clock output signal that is used to sample the user’s POH data at the TxPOH input pin. This output pin is always active, independent of the state of the “TxPOHIns” pin.
119	TxOH	I	**Transmit Overhead Input Pin** The Transmit Overhead Data Input Interface accepts the overhead data via this input pin, and inserts into the "overhead" bit position within the very next "outbound" DS3 frame. If the "TxOHIns" pin is pulled "high", the Transmit Overhead Data Input Interface will sample the data at this input pin (TxOH), on the falling edge of the "TxOHClk" output pin. Conversely, if the "TxOHIns" pin is pulled "low", then the Transmit Overhead Data Input Interface will NOT sample the data at this input pin (TxOH). Consequently, this data will be ignored.
120	TCellTxed	O	**Transmit Cell Processor—Cell Transmitted Indicator:** This output pin pulses “high” each time the Transmit Cell Processor transmits a cell to the Transmit PLCP Processor (or Transmit DS3 Framer).
121	TxOHClk	O	**Transmit Overhead Clock:** The function of this pin is the same in both Clear Channel and ATM UNI Modes of the XRT72L71. This pin serves as the clock signal for the external interface to insert the OH data on the TxOH pin. The user can insert OH data on the TxOH pin at the rising edge of this clock signal.
122	TxOHFrame	O	**Transmit Overhead Framing Pulse:** The function of this pin is same in both Clear Channel and ATM UNI modes of XRT72L71. When the external interface samples this pin high at the rising edge of TxOHClk, it should provide 'X' bit (first OH bit within DS3 frame) on the TxOH pin. This signal is high for one TxOHClk duration and repeats once for each DS3 frame.
123	$\overline{\text{TxUEn}}$	I	**Transmit UTOPIA Interface Block—Write Enable:** This active-low signal, from the ATM Layer processor enables the data on the Transmit UTOPIA Data Bus to be written into the TxFIFO on the rising edge of TxUClk. When this signal is asserted, then the contents of the byte or word that is present, on the Transmit UTOPIA Data Bus, will be latched into the Transmit UTOPIA Interface block, on the rising edge of TxUClk. When this signal is negated, then the Transmit UTOPIA Data bus inputs will be tri-stated.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
124	TxUSoC	I	**Transmitter—Start of Cell (SoC) Indicator Input:** This input pin is driven by the ATM Layer processor and is used to indicate the start of an ATM cell that is being transmitted from the ATM layer processor. This input pin must be pulsed "high" when the first byte (or word) of a new cell is present on the Transmit UTOPIA Data Bus. This input pin must remain "low" at all other times.
125	TxUPrty	I	**Transmit UTOPIA Data Bus—Parity Input:** The ATM Layer processor will apply the parity value of the byte or word which is being applied to the Transmit UTOPIA Data Bus (e.g., TxUData[7:0] or TxUData[15:0]) inputs of the UNI, respectively. Note: this parity value should be computed based upon the odd-parity of the data applied at the Transmit UTOPIA Data Bus. The Transmit UTOPIA Interface block (within the UNI) will independently compute an odd-parity value of each byte (or word) that it receives from the ATM Layer processor and will compare it with the logic level of this input pin.
126	TxUClav	O	**Transmit UTOPIA Interface—Cell Available Output Pin:** This output pin supports data flow control between the ATM Layer processor and the Transmit UTOPIA Interface block. The exact functionality of this pin depends upon whether the UNI is operating in the "Octet Level" or "Cell Level" handshaking mode. **Octet Level Handshaking:** When the Transmit UTOPIA Interface block is operating in the octet-level handshaking mode, this signal is negated (toggles "low") when the TxFIFO is not capable of handling four more write operations; by the ATM Layer processor to the Transmit UTOPIA Interface block. This signal will be asserted when the TxFIFO is capable of receiving four or more write operations of ATM cell data. **Cell Level Handshaking:** When the Transmit UTOPIA Interface block is operating the cell-level handshaking mode, this signal is asserted (toggles "high") when the TxFIFO is capable of receiving at least one more full cell of data from the ATM Layer processor. This signal is negated, if the TxFIFO is not capable of receiving one more full cell of data from the ATM Layer processor. **Multi-PHY Operation:** When the UNI chip is operating in the Multi-PHY mode, this signal will be tri-stated until the TxUClk cycle following the assertion of a valid address on the Transmit UTOPIA Address bus input pins (e.g., when the contents on the Transmit UTOPIA Address bus pins match that within the Transmit UTOPIA Address Register). Afterwards, this output pin will behave in accordance with the cell-level handshake mode.
127	GND	***	Ground Signal Pin.
128	TxUData8	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
129	TxUData0	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
130	TxUData9	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
131	TxUData1	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
132	TxUData10	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
133	TxUData2	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
134	TxUData11	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
135	TxUData3	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
136	VDD	***	**Power Supply Pin**
137	TxUData4	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
138	TxUData12	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
139	TxUData5	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
140	TxUData13	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
141	TxUData6	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
142	TxUData14	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
143	TxUData7	I	**Transmit UTOPIA Data Bus Input:** Please see description for TxUData15 pin 144
144	TxUData15	I	**Transmit UTOPIA Data Bus Input—MSB:** This input pin, along with TxUData14 through TxUData0 comprise the Transmit UTOPIA Data Bus input pins. When the ATM Layer Processor wishes to transmit ATM cell data through the XRT72L71 DS3 UNI, it must place this data on these pins. The data, on the Transmit UTOPIA Data Bus is latched into the Transmit UTOPIA Interface block on the rising edge of TxUClk.
145	VDD	***	**Power Supply Pin**
146	TxUAddr4	I	**Transmit UTOPIA Address Bus—MSB Input:** This input pin, along with TxUAddr3 through TxUAddr0 comprise the Transmit UTOPIA Address Bus input pins. The Transmit UTOPIA Address Bus is only in use when the UNI is operating in the M-PHY mode. When the ATM Layer processor wishes to write data to a particular UNI device, it will provide the address of the “intended UNI” on the Transmit UTOPIA Address Bus. The contents of the Transmit UTOPIA Address Bus input pins are sampled on the rising edge of TxUClk. The DS3 UNI will compare the data on the Transmit UTOPIA Address Bus with the pre-programmed contents of the TxUT Address Register (Address = 70h). If these two values are identical and the $\overline{\text{TxUEN}}$ pin is asserted, then the TxU-Clav pin will be driven to the appropriate state (based upon the TxFIFO fill level) for the Cell Level handshake mode of operation.
147	TxUAddr0	I	**Transmit UTOPIA Address Bus Input—LSB:** (See Description for TxUAddr4 pin 146)
148	TxUAddr3	I	**Transmit UTOPIA Address Bus Input:** (See Description for TxUAddr4 pin 146)
149	TxUAddr1	I	**Transmit UTOPIA Address Bus Input:** (See Description for TxUAddr4 pin 146)
150	TxUAddr2	I	**Transmit UTOPIA Address Bus Input:** (See Description for TxUAddr4 pin 146)

PIN DESCRIPTION (CONTINUED)

PIN NO.	SYMBOL	TYPE	DESCRIPTION
151	TxUClk	I	**Transmit UTOPIA Interface Clock:** The Transmit UTOPIA Interface clock is used to latch the data on the Transmit UTOPIA Data bus, into the Transmit UTOPIA Interface block. This clock signal is also used as the timing source for circuitry used to process the ATM cell data into and through the TxFIFO. During Multi-PHY operation, the data on the Transmit UTOPIA Address bus pins is sampled on the rising edge of TxUClk.
152	GND	***	**Ground Signal Pin**
153	TestMode	***	**Factory Test Mode Pin** ***NOTE:*** *The user should tie this pin to ground.*
154	TxGFCMSB	O	**Transmit GFC Nibble-Field Serial Input Port—MSB Indicator:** This signal, along with TxGFC and TxGFCClk combine to function as the "Transmit GFC Nibble Field" serial input port. This output signal will pulse "high" when the MSB (most significant bit) of the GFC Nibble (for a given cell) is expected at the TxGFC input pin.
155	$\overline{\text{Reset}}$	I	**Reset Input:** When this "active-low" signal is asserted, the UNI device will be asynchronously reset. Additionally, all outputs will be "tri-stated", and all on-chip registers will be reset to their default values.
156	TxGFCClk	O	**Transmit GFC Nibble Field Serial Input Port Clock:** This signal, along with TxGFC, and TxGFCMSB combine to function as the "Transmit GFC Nibble-field" serial input port. The "Transmit GFC Nibble-field" serial input port uses this output clock signal to sample the values applied to the TxGFC pin, on its rising edge. This pin will provide four rising edges for each cell being transmitted.
157	ALE_AS	I	**Address Latch Enable/Address Strobe:** This input is used to latch the address (present at the Microprocessor Interface Address Bus, A[8:0]) into the UNI Microprocessor Interface circuitry and to indicate the start of a READ/WRITE cycle. This input is active-high in the Intel Mode (MOTO = "low") and active-low in the Motorola Mode (MOTO = "high").
158	TxGFC	I	**Transmit GFC Nibble-Field Serial Input Port:** This signal, along with TxGFCClk and TxGFCMSB combine to function as the "Transmit GFC Nibble-field" serial input port. The user will specify the value of the GFC field, within a given ATM cell, by serial transmitting its four bit value into this input. Each of these four bits will be clocked into the UNI via rising edge of the TxGFCClk clock output signal.
159	GND	***	**Ground Signal Pin**
160	Rdy_Dtck	O	**READY or DTACK:** This "active-low" output pin will function as the READY output, when the microprocessor interface is running in the "Intel" Mode; and will function as the DTACK output, when the microprocessor interface is running in the "Motorola" Mode. **"Intel" Mode—READY Output.** When the UNI negates this output pin (e.g., toggles it "low"), it indicates (to the µP) that the current READ or WRITE cycle is to be extended until this signal is asserted (e.g., toggled "high"). **"Motorola" Mode:—DTACK (Data Transfer Acknowledge) Output.** The UNI device will assert this pin in order to inform the local microprocessor that the present READ or WRITE cycle is nearly complete. If the UNI device requires that the current READ or WRITE cycle be extended, then the UNI will delay its assertion of this signal. The 68000 family of µPs requires this signal from its peripheral devices, in order to quickly and properly complete a READ or WRITE cycle.

ABSOLUTE MAXIMUM RATINGS

DC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{CC}	Power Supply Current		120		mA	TxUCLK and RxUCLK are operating at 25MHz
I_{LL}	Data Bus Tri-State Bus Leakage Current				µA	
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage	0.0		0.4	V	
V_{OH}	Output High Voltage	2.4		V_{CC}	V	I_{OC} = 1.6mA
I_{OC}	Open Drain Output Leakage Current				µA	I_{OH} = 40µA
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = V_{CC}
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND

AC ELECTRICAL CHARACTERISTICS

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Transmit UTOPIA Interface Block (See Figure 96)						
t_1	TxUData[15:0] to rising edge of TxU-Clk Setup Time	4			ns	
t_2	TxUData[15:0] Hold Time from rising edge of TxUClk	1			ns	
t_3	TxUTOPIA Write Enable Setup Time to rising edge of TxUClk	4			ns	
t_4	TxUTOPIA Write Enable Hold Time from rising edge of TxUClk	1			ns	
t_5	TxUPrty Setup Time to rising edge of TxUClk	4			ns	
t_6	TxUPrty Hold Time from rising edge of TxUClk	1			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_7	TxUSoC Setup Time to rising edge of TxUClk	4			ns	
t_8	TxUSoC Hold Time from rising edge of TxUClk	1			ns	
t_9	TxUAddr[4:0] Setup Time to rising edge of TxUClk	4			ns	
t_{10}	TxUAddr[4:0] Hold Time from rising edge of TxUClk	1			ns	
t_{11}	TxUClav signal valid (not Hi-Z) from first TxUClk rising edge of valid and correct TxUAddr[4:0]		6	16	ns	
t_{12}	TxUClav signal Hi-Z from first TxUClk rising edge of different TxUAddr[4:0]		9	19	ns	
Transmit Cell Processor (GFC Serial Input Port)—See						
t_{13}	Clock Period of TxGFCClk		232		ns	There will be a periodic clock gap ever six clocks.
fGFCClk	Frequency of TxGFCClk				Hz	
t_{14}	Delay from rising edge of TxGFCClk to rising edge of TxGFCMSB pin		1.43		ns	
t_{15}	Pulse width of TxGFCMSB signal		232		ns	
t_{16}	TxGFC Data Setup time to rising edge of TxGFCClk	7			ns	
t_{17}	TxGFC Data Hold time from rising edge of TxGFCClk	3			ns	
Transmit PLCP Processor (Serial Input Port)—See						
t_{18}	Clock Period of TxPOHClk signal				ns	
t_{19}	Delay from rising edge of TxPOHFrame signal to rising edge of TxPOHClk signal				ns	
t_{20}	TxPOH setup time to rising edge of TxPOHClk signal				ns	
t_{21}	TxPOH signal hold time from rising edge of TxPOHClk signal				ns	
t_{22}	TxPOHIns signal setup time to rising edge of TxPOHClk				ns	
t_{23}	TxPOHIns signal hold time from rising edge of TxPOHClk				ns	
Transmit DS3 Framer (Serial Input Port)—See						
fTxOHClk	Frequency of TxOHClk signal				Hz	
t_{24}	Period of TxOHClk clock signal				ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{25}	Delay from rising edge of TxOHFrame signal to rising edge of TxOHClk signal				ns	
t_{26}	TxOH Data Setup time to rising edge of TxOHClk signal				ns	
t_{27}	TxOH Data Hold time from rising edge of TxOHClk signal				ns	
t_{28}	TxOHIns signal setup time to rising edge of TxOHClk				ns	
t_{29}	TxOHIns signal hold time from rising edge of TxOHClk				ns	
Transmit DS3 Framer (LIU Interface Port)—See						
t_{30}	Delay time of data on TxPOS or TxNEG, following the rising edge of the TxLineClk	0.7		2.0	ns	Transmit DS3 Framer is configured to update TxPOS and TxNEG on the rising edge of TxLineClk.
t_{31}	Delay time of data on TxPOS or TxNEG following the falling edge of the TxLineClk	0.7		1.5	ns	Transmit DS3 Framer is configured to update TxPOS and TxNEG on the falling edge of TxLineClk.
fTxLineClk	Clock frequency of TxLineClk		44.736		MHz	
t_{32}	Period of TxLineClk clock signal				ns	
t_{33}	Bit Period of data on TxPOS or TxNEG pins				ns	
Receive DS3 Framer (Serial Output Port)—See						
fRxOHClk	Frequency of RxOHClk signal				Hz	
t_{34}	Period of RxOHClk clock signal				ns	
t_{35}	Delay Time from rising edge of RxHClk to RxOHFrame signal				ns	
t_{36}	Delay Time from rising edge of RxOHClk to valid data at RxOH				ns	
t_{37}	Bit Period of data at RxOH				ns	
Receive DS3 Framer (LIU Interface Port)—See						
t_{38}	RxPOS/RxNEG data Setup Time to rising edge of RxLineClk	6			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the rising edge of RxLineClk.
t_{39}	RxPOS/RxNEG data Hold Time from rising edge of RxLineClk	3			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the rising edge of RxLineClk.
t_{40}	RxPOS/RxNEG data Setup Time to falling edge of RxLineClk	6			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the falling edge of RxLineClk.
t_{41}	RxPOS/RxNEG data Hold Time from falling edge of RxLineClk	3			ns	Receive DS3 Framer is configured to sample RxPOS and RxNEG on the falling edge of RxLineClk.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
fRxLi-neClk	Clock frequency of RxLineClk		44.736		MHz	
t_{42}	Period of RxLineClk clock signal				ns	
Receive PLCP Processor (Serial Output Port)—See Figure 105						
t_{43}	Clock Period of RxPOHClk signal				ns	
t_{44}	Delay from rising edge of RxPOHClk signal to rising edge of RxPOHFrame signal.	6		1.4	ns	
t_{45}	Delay from rising edge of RxPOHClk to Data valid at RxPOH output				ns	
t_{46}	Bit period of data at RxPOH output signal				ns	
Receive Cell Processor (GFC Serial Output Port)—						
t_{47}	Clock Period of RxGFCClk		232		ns	
t_{48}	Delay from rising edge of RxGFCClk to rising edge of RxGFCMSB pin.	0.06		1.4	ns	
t_{49}	Pulse width of RxGFCMSB signal		232		ns	
t_{50}	Delay from rising edge of RxGFCMSB signal to first valid bit at RxGFC.		0		ns	
t_{51}	Delay from rising edge of RxGFCClk to valid bit at RxGFC.	0.9		2.4	ns	
t_{52}	Pulse width of Bit at RxGFC output.		232		ns	
Receive UTOPIA Interface Block						
t_{53}	Delay time from rising edge of RxUClk to Data Valid at RxData[15:0]	1	9.9	16	ns	
t_{54}	Rx UTOPIA Read Enable setup time to rising edge of RxUClk	4			ns	
t_{55}	Delay time from rising edge of RxUClk to valid RxPrty bit	1	10	16	ns	
t_{56}	Delay time from rising edge of RxUClk to valid RxUSoC bit	1	9.9	16	ns	
t_{57}	Delay time from Read Enable false to Data Bus being tri-stated	1	11.5	16	ns	
t_{58}	Delay time from Read Enable false to RxPrty bit being tri-stated	1	12	16	ns	
t_{59}	Delay time from Read Enable false to RxUSoC bit being tri-stated	1	11.5	16	ns	
t_{60}	RxUAddr[4:0] Setup Time to rising edge of RxUClk	4			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{61}	RxUAddr[4:0] Hold Time from rising edge of RxUClk	1			ns	
t_{62}	RxUClav signal valid (not Hi-Z) from first RxUClk rising edge of valid and correct TxUAddr[4:0]	1	7.8	16	ns	
t_{63}	RxUClav signal Hi-Z from first RxUClk rising edge of different RxUAddr[4:0].	1	9.2	16	ns	
Microprocessor Interface—Intel						
t_{64}	A8—A0 Setup Time to ALE_AS Low	3			ns	
t_{65}	A8—A0 Hold Time from ALE_AS Low.	2			ns	
Intel Type Read Operations						
t_{66}	$\overline{RD}$_DS, $\overline{WR}$_RW Pulse Width	30			ns	
t_{67}	Data Valid from $\overline{RD}$_DS Low.	6		11	ns	
t_{68}	Data Bus Floating from $\overline{RD}$_DS High.				ns	
t_{69}	ALE to RD* Time	4			ns	
t_{70}	$\overline{RD}$ Time to :NOT READY" (e.g., Rdy_Dtck toggling "Low")	15		23	ns	
Intel Type Read Operations						
t_{76}	Minimum Time between Read Burst Access (e.g., the rising edge of RD* to falling edge of RD*)	5			ns	
Intel Type Read Operations						
t_{71}	Data Setup Time to $\overline{WR}$_RW* High	4			ns	
t_{72}	Data Hold Time from $\overline{WR}$_RW* High	2			ns	
t_{73}	High Time between Reads and/or Writes	20			ns	
t_{74}	ALE to WR* Time	4			ns	
t_{77}	min. Time between Write Burst Access (e.g., the rising edge of WR* to the falling edge of WR*)	5			ns	
t_{770}	$\overline{CS}$ Assertion to falling edge of $\overline{WR}$_RW	20			ns	
Microprocessor Interface—Motorola Read Operations						
t_{78}	A8—A0 Setup Time to ALE_AS High	3			ns	
t_{79}	A8—A0 Hold Time from ALE_AS Low	2			ns	
t_{80}	Data Valid from RDB_DS Low.	6			ns	
t_{81}	DTACK Low from RDB_DS Low.	15			ns	

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Test Conditions: T_A = 25°C, V_{CC} = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
t_{82}	Data Bus Floating from RDB_DS High	7		12	ns	
t_{83}	Address Strove (AS) t Data Strobe (DS) Time				ns	
Microprocessor Interface—Motorola Read & Write Operations						
t_{84}	Data Setup Time to rising edge of RDB_DS (Data Strobe) for Write	15			ns	
t_{85}	Data Hold Time from rising edge of RDB_DS (Data Strobe) for Write	2			ns	
t_{86}	AS to DS Time	4			ns	
t_{87}	DS to DTACK Time	15			ns	
t_{88}	Min. time between Read Burst Access	5			ns	
t_{89}	Min. time between Write Burst Access	5				
Reset Pulse Width—Both Motorola and Intel Operations						
t_{90}	ResetB* pulse width	30				

SYSTEM/FUNCTIONAL DESCRIPTION

FUNCTIONAL DESCRIPTION

The XRT72L71 UNI can functionally be subdivided into 6 different sections, as shown in Figure 1 .

- Receive Section
- Transmit Section
- Microprocessor Interface Section
- Performance Monitor Section
- Test and Diagnostic Section
- Line Interface Unit Scan Drive Section

The features of each of these functional sections are briefly outlined below.

THE RECEIVE SECTION

The purpose of the Receiver Section of the XRT72L71 DS3 ATM UNI device is to allow a local ATM Layer (or ATM Adaptation Layer) processor to receive ATM cell data from a remote piece of equipment via a public or leased DS3 transport medium.

The Receive Section of the XRT72L71 DS3 UNI consists of the following functional blocks.

- Receive DS3 Framer Block
- Receive PLCP (Physical Layer Convergence Protocol) Processor Block
- Receive Cell Processor Block
- Receive UTOPIA Interface Block

The Receive Section of the UNI device will:

- The Receive DS3 Framer will synchronize to the incoming DS3 data stream and remove or process the DS3 Framing/Overhead Bits. This procedure will result in either extracting PLCP frame data or “Direct-Mapped” ATM Cell data, from the payload portion of the incoming DS3 data stream. The Receive DS3 Framer can used to receive FEAC (Far End Alarm & Control) messages via an on-chip FEAC Transceiver.

Additionally, the Receive DS3 Framer includes an on-chip LAPD Receiver that can receive incoming path maintenance data link messages from the far-end Transmit DS3 Framer of the “Far End” Terminal.

NOTE: *The Receive DS3 Framer supports both M13 and C-bit Parity Frame Formats.*

- The Receive PLCP Processor will identify the frame boundary of each incoming PLCP frame, extract and process the overhead bytes of these PLCP frames (applies only if the UNI is operating in the PLCP Mode). The Receive PLCP Processor will also perform some error checking on the incoming PLCP frames. The Receive PLCP Processor will inform the Far-End (Transmitting UNI) of the results of this error-checking by internally routing these results to the “Near-End” Transmit PLCP Processor, for transmission back out to the Far-End Terminal.
- The Receive Cell Processor will perform the following functions:
  - Cell Delineation
  - HEC Byte Verification of incoming cells (optional)
  - Cell-payload de-scrambling (optional)
  - Idle cell detection and removal (optional)
  - User and OAM Cell Filtering (optional)
  - OAM Cell Processing (optional)
- The UNI provides 54 bytes of on-chip RAM that allows for the reception and processing of selected OAM cells.
- The RxFIFO, within the Receive UTOPIA Interface block will temporarily hold any ATM cells that pass through the Receive Cell Processor, where they can be read out by the ATM Layer processor, over the Receive UTOPIA Data Bus.

THE TRANSMIT SECTION

The purpose of the Transmit section of the XRT72L71 DS3 ATM UNI device is to allow a local ATM Layer (or ATM Adaptation Layer) processor to transmit ATM Cell data to a remote piece of equipment via a public or leased DS3 transport medium.

The Transmit Section of the XRT72L71 DS3 UNI consists of the following functional blocks.

- Transmit UTOPIA Interface Block
- Transmit Cell Processor Block
- Transmit PLCP Processor Block
- Transmit DS3 Framer Block

The Transmit Section of the UNI device will:

- Allow the ATM Layer processor to write ATM cells into the Transmit FIFO (within the Transmit UTOPIA Interface block) via a standard UTOPIA Level 2 interface.
- The Transmit Cell Processor will read in these cells from the Transmit FIFO (if available) for further processing. If no cell is available within the Transmit FIFO, then the Transmit Cell Processor will automatically generate an Idle cell. The UNI is equipped with on-chip registers to allow for the generation of customized Idle cells.

- The UNI provides 54 bytes of on-chip RAM that allows for the generation and transmission of "user-specified" OAM cells. The Transmit Cell Processor will generate and transmit these OAM cells upon software command.
- The Transmit Cell Processor will (optionally) scramble the Cell Payload bytes and (optionally) compute and insert the HEC (Header Error Check) byte. This HEC byte will be inserted into the fifth octet of each cell prior to being transferred to the Transmit PLCP Processor (or the Transmit DS3 Framer).
- The Transmit PLCP Processor will pack 12 ATM cells into each PLCP frame and automatically determine the nibble-stuffing option of the current PLCP frame. These PLCP frames will also include an overhead byte that reflect BIP-8 (Bit Interleaved Parity) calculation results, a byte that reflects the current stuffing option status of the current PLCP frame, Path Overhead and Identifier bytes, and diagnostic-related bytes reflecting any detected BIP-8 errors and alarm conditions detected in the Receive section of the UNI chip.
- These PLCP frames (or "Direct Mapped" ATM cells) will be inserted into the payload of an outgoing DS3 frame, for transmission to the "Far-End" Terminal, by the Transmit DS3 Framer. The Transmit DS3 Framer will transmit FEAC (Far End Alarm & Control) messages to the Far-End Receiver via an on-chip FEAC Transceiver.Additionally, the Transmit DS3 Framer can transmit path maintenance data link messages to the Far-End Terminal via the on-chip LAPD Transmitter.

Note: The Transmit DS3 Framer will support either M13 or C-bit Parity Framing Formats.

THE MICROPROCESSOR INTERFACE SECTION

The Microprocessor Interface Section allows a user (or a local "housekeeping" processor) to do the following:

- To configure the UNI IC into a wide variety of operating modes; by writing data into any one of a large number of "read/write" registers.
- To monitor many aspects of the UNI's performance by reading data from any one of a large number of "read/write" and "read-only" registers.
- To run in a "polling" or "interrupt-driven" environment. The UNI IC contains an extensive interrupt structure consisting of a wide range of interrupt enable and interrupt status registers.
- To command the UNI IC to transmit OAM cells, FEAC messages and/or LAPD Messages frames, upon software command.
- To read in and process received OAM cells, FEAC messages and/or Path Maintenance Data Link Messages from the UNI IC.
- The Microprocessor Interface allows the user to interface the XRT72L71 DS3 UNI to either an Intel type or Motorola type processor. Additionally, the Microprocessor Interface can be configured to operate over an 8-bit or 16-bit data bus.
- The Microprocessor Interface section includes a "Loss of Clock Signal" protection feature that automatically completes (or terminates) a "Read/Write" operation, should a "Loss of Clock Signal" event occur.

PERFORMANCE MONITOR SECTION

The Performance Monitor Section of the XRT72L71 DS3 UNI consists of a large number of "Reset-upon-Read" and "Read-Only" registers that contains cumulative and "one-second" statistics that reflect the performance/health of the UNI chip/system. These cumulative and "one-second" statistics are kept on some of the following parameters.

- Number of Line Code Violation events detected by the Receive DS3 Framer
- Number of Framing Bit (F- and M-bit) errors detected by the Receive DS3 Framer
- Number of P-bit Errors detected by the Receive DS3 Framer
- Number of FEBE Events detected by the Receive DS3 Framer
- Cumulative number of BIP-8 errors, detected by the Receive PLCP Processor
- Number of PLCP framing errors, detected by the Receive PLCP Processor
- Cumulative sum of the FEBE value, in the incoming G1 bytes (within each PLCP frame), received by the Receive PLCP Processor
- Number of Single-bit HEC byte Errors detected
- Number of Multi-bit HEC byte Errors detected
- Number of Received Idle Cells
- Number of Received Valid (User and OAM) cells discarded
- Number of Discarded Cells
- Number of Transmitted Idle Cells
- Number of Transmitted Valid Cells

TEST AND DIAGNOSTIC SECTION

The Test and Diagnostic Section allows the user to perform a series of tests in order to verify proper functionality of the UNI chip and/or the user's system. The

"Test and Diagnostic" section provides the UNI IC with the following capabilities.

- Allows the UNI to operate in the Line, Cell, and PLCP Loop-back Modes
- Contains an internal Test Cell Generator and an internal Test Cell Receiver. The Test Cell Generator will generate Test Cells with "user-defined" header byte patterns. The Test Cell Generator will also fill the payload portion of these test cells with bytes from an on-chip PRBS generator.
- The Test Cell Generator can generate test cells in "One Shot" Mode (e.g., a burst of 1024 test cells) or in "Continuous" Mode (e.g., a continuous stream of test cells).
- The Test Cell Receiver will identify and collect the Test Cells for further analyses, based upon the "user-defined" header byte patterns. Additionally, the Test Cell Receiver will report the occurrence of any errors by incrementing an on-chip register.

LINE INTERFACE DRIVE AND SCAN SECTION

The Line Interface Drive and Scan Section allows the user to monitor and control many aspects of the XRT7300 E3/DS3/STS-1 Line Interface Unit, via on-chip registers, within the UNI IC. This feature eliminates the need for glue logic to interface the XRT72L71 DS3 UNI to the XRT7300 DS3 Line Interface Unit IC.

- The On-Chip Line Interface Drive register allows the user to control the state of 6 output pins. The function of these output pins, when asserted, are tabulated below.

CLEAR CHANNEL MODE OPERATION

Signal Name	Function of Output Pin
REQB	**Receive Equalizer By-Pass:** Setting this bit-field to "1" configures the XRT7300 device to shut off its internal Receive Equalizer. Setting this bit-field to "0" configures the XRT7300 device to enable its internal Receive Equalizer.
TAOS	**Transmit "All Ones" Pattern.** Setting this bit-field to "1" configures the XRT7300 LIU IC to overwrite the DS3 data that is output via the TxPOS and TxNEG outputs, and transmit an "All Ones" pattern onto the line. Setting this bit-field to "0" configures the XRT7300 LIU IC to transmit data, as is applied to it via the TPDATA and TNDATA input pins.
ENCODIS	**B3ZS Encoder Disable/Enable Select.** Setting this bit-field to "1" disables the B3ZS Encoder, within the XRT7300 device. Setting this bit-field to "0" enables the B3ZS Decoder within the XRT7300 device.
TxLev	**Transmit Output Signal Line Build Out Select.** Setting this bit-field to "1" disables the Transmit Line Build Out circuitry within the XRT7300 device. In this case, the XRT7300 will generate an "unshaped" square wave signal out onto the line (via the TTIP and TRING output pins). *Note: In order to configure the XRT7300 device to generate a line signal that complies with the Transmit Output Pulse Template Requirements (per GR-499-CORE), this setting is advised if the cable length between the Transmit Output of the XRT7300 device and the Cross-Connect is greater than 225 feet.* Setting this bit-field to "0" enables the Transmit Line Build Out circuitry within the XRT7300 device. In this case, the XRT7300 device will generate a "shaped" square wave out onto the line (via the TTIP and TRING output pins). *Note: In order to configure the XRT7300 device to generate a line signal that complies with the Transmit Output Pulse Template Requirements (per GR-499-CORE), this setting is advised if the cable length between the Transmit Output of the XRT7300 device and the Cross-Connect is less than 225 feet.*

Signal Name	Function of Output Pin
RLOOP	**Remote Loop-Back Mode Select:** This bit-field, along with LLOOP can be used to configure the XRT7300 device into one of four different loop-back modes. Setting RLOOP to “1” (with LLOOP = 0) configures the XRT7300 device to operate in the Remote Loop-Back Mode. Setting RLOOP to “1” (with LLOOP = 1) configures the XRT7300 device to operate in the “Digital Local Loop-Back” Mode. Setting RLOOP to “0” (with LLOOP = 1) configures the XRT7300 device to operate in the “Analog Local Loop-Back” Mode. Setting RLOOP to “0” (with LLOOP = 0) configures the XRT7300 device to operate in the “Normal” (No-Loop-back) Mode.
LLOOP	**Local Loop-Back Mode Select:** This bit-field along with RLOOP can be used to configure the XRT7300 device into one of four different loop-back modes. Setting LLOOP to “1” (with RLOOP = 0) configures the XRT7300 device to operate in the “Analog Local Loop-back” Mode. Setting LLOOP to “1” (with RLOOP = 1) configures the XRT7300 device to operate in the “Digital Local Loop-back” Mode. Setting LLOOP to “0” (with RLOOP = 0) configures the XRT7300 device to operate in the “Normal” (No-Loop-back) Mode. Setting LLOOP to “0” (with RLOOP = 1) configures the XRT7300 device to operate in the “Remote Loop-back” Mode.

- The On-Chip Line Interface Scan Register allows the user to monitor the state of 3 input pins. The function of these input pins, when asserted, are tabulated below.

Signal Name	Function of Input Pin if asserted
DMO	Indicates that the "Drive Monitor" circuitry within the XRT7300 has not detected any bipolar signals within the last 128 ± 32 bit periods.
RLOL	Indicates that the "Clock Recovery" circuit, within the XRT7300 has lost "lock" with the incoming DS3 line signal.
RLOS	Indicates that the XRT7300 device is declaring an LOS (Loss of Signal) Condition.

FEATURES

TRANSMIT AND RECEIVE SECTIONS

UTOPIA Interface Blocks

- Compliant with UTOPIA Level 2 Interface Specification (e.g., supports Single-PHY or Multi-PHY operation).
- 8-bit or 16-bit wide UTOPIA Data Bus operation in the Transmit and Receive Directions.
- The UTOPIA Data Bus runs at clock rates of 25 MHz, 33 MHz and 50 MHz
- Supports both Octet-Level and Cell-Level Handshaking between the UNI and the ATM Layer processor.
- The Transmit UTOPIA Interface block performs parity checking of ATM cell data that is written into it, by the ATM Layer processor. Will optionally discard errored cells.
- Contains on-chip 16 cell FIFO in the Transmit Direction (TxFIFO)
- The TxFIFO can be configured to operate with depths of 4, 8, 12 or 16 cells
- Contains on-chip 16 cell FIFO in the Receive Direction (RxFIFO)

TRANSMIT CELL PROCESSOR BLOCK

- Optionally computes and inserts HEC byte into all cells (user, OAM and Idle).
- Optionally scrambles the payload of each cell.
- Idle cells are automatically generated when no user cells are available in the TxFIFO.
- UNI contains on-chip registers that support the generation/transmission of default or custom Idle cells.
- UNI contains the on-chip "Transmit OAM Cell" buffer (54 bytes) that allows the user to write in and store the contents of OAM cells, in preparation for transmission.
- OAM cells are transmitted upon software command.
- Performs "Data Path Integrity" check on all incoming cell data, originating from the ATM Layer processor.
- Provides a serial input port to allow the user to insert the GFC (Generic Flow Control) field externally into the GFC nibble field of an outbound (e.g., Transmit direction) valid ATM Cell.

RECEIVE CELL PROCESSOR BLOCK

- Performs cell delineation on either "Direct Mapped" ATM cell data or PLCP frames.
- Verifies the HEC bytes of incoming cells and corrects most cells with single bit errors. Cells with multi-bit errors are detected and are optionally discarded.
- (Optionally) Performs filtering of Idle Cells.
- (Optionally) Performs filtering of User and OAM cells.
- UNI contains on-chip buffer space ("Receive OAM Cell" buffer) that allows for the reception and processing of selected OAM cells.
- Optionally de-scrambles the payload of each cell.
- Provides a serial output port that allows the user to read the GFC value of an incoming (e.g., Receive direction) ATM Cell.
- Inserts the "Data Path Integrity Check" patterns in all cells that are written to the RxFIFO.

TRANSMIT PLCP PROCESSOR BLOCK

- Can be disabled to support the "Direct Mapped" ATM mode.
- Packs 12 ATM cells into each PLCP frame along with various other overhead bytes.
- The Transmit PLCP Processor will automatically determine its own stuffing options.
- Overhead bytes include those that support BIP-8 calculations (B1), indicator of stuff-option status for current PLCP frame (C1), diagnostic byte that reflects alarms conditions that were detected in the Receive Section of the UNI (G1); and Path Overhead bytes.
- Provides a serial input port for user to insert PLCP Overhead Bytes externally.

RECEIVE PLCP PROCESSOR BLOCK

- Can be disabled to support the "Direct Mapped" ATM mode.
- Determines the frame boundaries of incoming PLCP frames (from the Receive DS3 Framer).
- Extracts and processes the PLCP frame overhead bytes.
- Provides a serial output port for user to read in the contents of the PLCP Overhead Bytes from the incoming data.

TRANSMIT/RECEIVE DS3 FRAMER BLOCK

- Supports the M13 and C-bit Parity Framing Formats.
- Transmit and Receive DS3 Framers can transmit/receive data in the Unipolar or the Bipolar (AMI or B3ZS line codes) format.
- The Transmit DS3 Framer provides a serial input port that allows the user to insert his/her own values for the overhead bits of the "outbound" DS3 frames.
- The Receive DS3 Framer provides a serial output port that allows the user access to the values of the overhead bits of the "incoming" DS3 frames.
- The Receive DS3 Framer can be configured to sample the incoming DS3 data (at the RxPOS and RxNEG input pins) via the rising edge or falling edge of the Receive Line Clock (RxLineClk) input.
- The Transmit DS3 Framer can be configured to update the "outbound" DS3 data (at the TxPOS and TxNEG output pins) at the rising edge or falling edge of the Transmit Line Clock (TxLineClk) output.
- UNI includes on-chip RAM space to support the transmission and reception of path maintenance data link messages via an on-chip LAPD Transceiver
- UNI includes on-chip registers to support the transmission and reception of FEAC (Far End Alarm & Control) messages via an on-chip FEAC Transceiver.
- Contains on-chip FEAC Transceiver.
- Contains on-chip LAPD Transceiver.

MICROPROCESSOR INTERFACE SECTION

- Can be interfaced to Motorola or Intel type of microprocessors/microcontrollers

- Microprocessor interface supports 8 bit wide or 16-bit wide read/write accesses.
- Supports polled or interrupt-driven environments.
- Supports burst mode “Read and Write” operations between the “local” microprocessor and the UNI on-chip registers and RAM locations.
- Includes a “Loss of Clock Signal” protection feature that terminates “Read/Write” cycles with the local µP, during a “Loss of Clock signal” event.

Performance Monitor Section

Contains numerous on-chip “Read-Only” registers that allows the user to monitor the overall “health” of the system.

Test and Diagnostic Section

- Supports Line, PLCP, and Cell Loop-back Modes
- Supports Line-Side Testing
- Contains an on-chip Test Cell Generator and an on-chip Test Cell Receiver
- Test Cell Generator can generate a “continuous” stream of test cells, or a “one-shot” burst of 1024 test cells.
- The Test Cell Receiver identifies, collects and evaluates Test Cells for errors.
- The Test Cell Receiver also reports the occurrence of errors to the user.

Line Interface Drive and Scan Section

- Consists of an on-chip “Read/Write” register that allows the user to control the state of 6 output pins.

Consists of an on-chip “Read-Only” register that allows the user to monitor the state of 3 input pins.

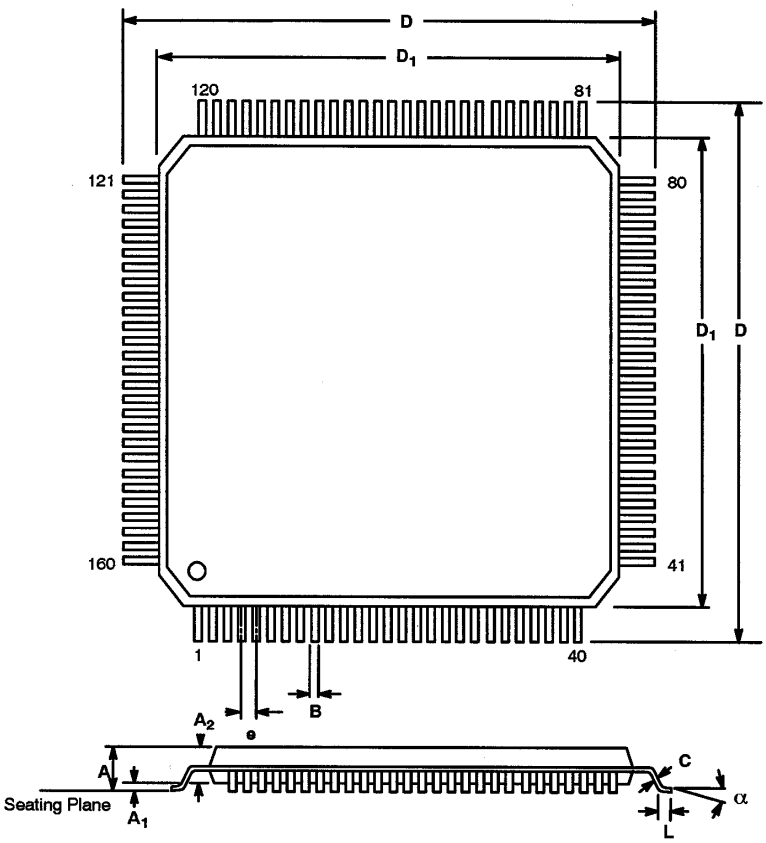
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT72L71SIQ160	28 x28 mm Plastic QFP	-40°C to +85°C

PACKAGE DIMENSIONS

160 LEAD PLASTIC QUAD FLAT PACK
(28 mm x 28 mm, QFP)

Rev. 1.00



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.127	0.160	3.22	4.07
A_1	0.002	0.016	0.05	0.40
A_2	0.125	0.144	3.17	3.67
B	0.009	0.015	0.22	0.38
C	0.005	0.009	0.13	0.23
D	1.218	1.238	30.95	31.45
D_1	1.098	1.106	27.90	28.10
e	0.0256 BSC		0.65 BSC	
L	0.029	0.040	0.73	1.03
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

REVISION HISTORY

REV. P1.0.1 made edits to device name, general information and added description for test mode pin.

NOTICE

Datasheet April 2000.