Mixed-Signal Products

UT14AD03 RadHard Pipelined Analog to Digital Converter

Advanced Data Sheet
January 24, 2008

FEATURES

- 14-bit Resolution
- Monolithic RadHard CMOS technology
- 3 MSPS conversion rate
- Integral non-linearity +/- 2 LSB
- Differential non-linearity +/- 1 LSB
- Internal reference
- Differential analog input
- µP-compatible parallel interface or SPI serial interface
- Low power
- Radiation performance
  - Intrinsic total-dose: 300 krad(Si)
  - SEL Immune >111 MeV-cm^2/mg
- Packaging:
  - Available in 48-pin ceramic quad flat pack for parallel interface
  - Available in 48-TQFP for industrial/medical
- Standard Microcircuit Drawing TBD
  - QML Q and V

APPLICATIONS

- Motor/motion control of radiation therapy equipment
- Cargo security scanning imaging
- Satellite system telemetry
- Nuclear power plant sensors

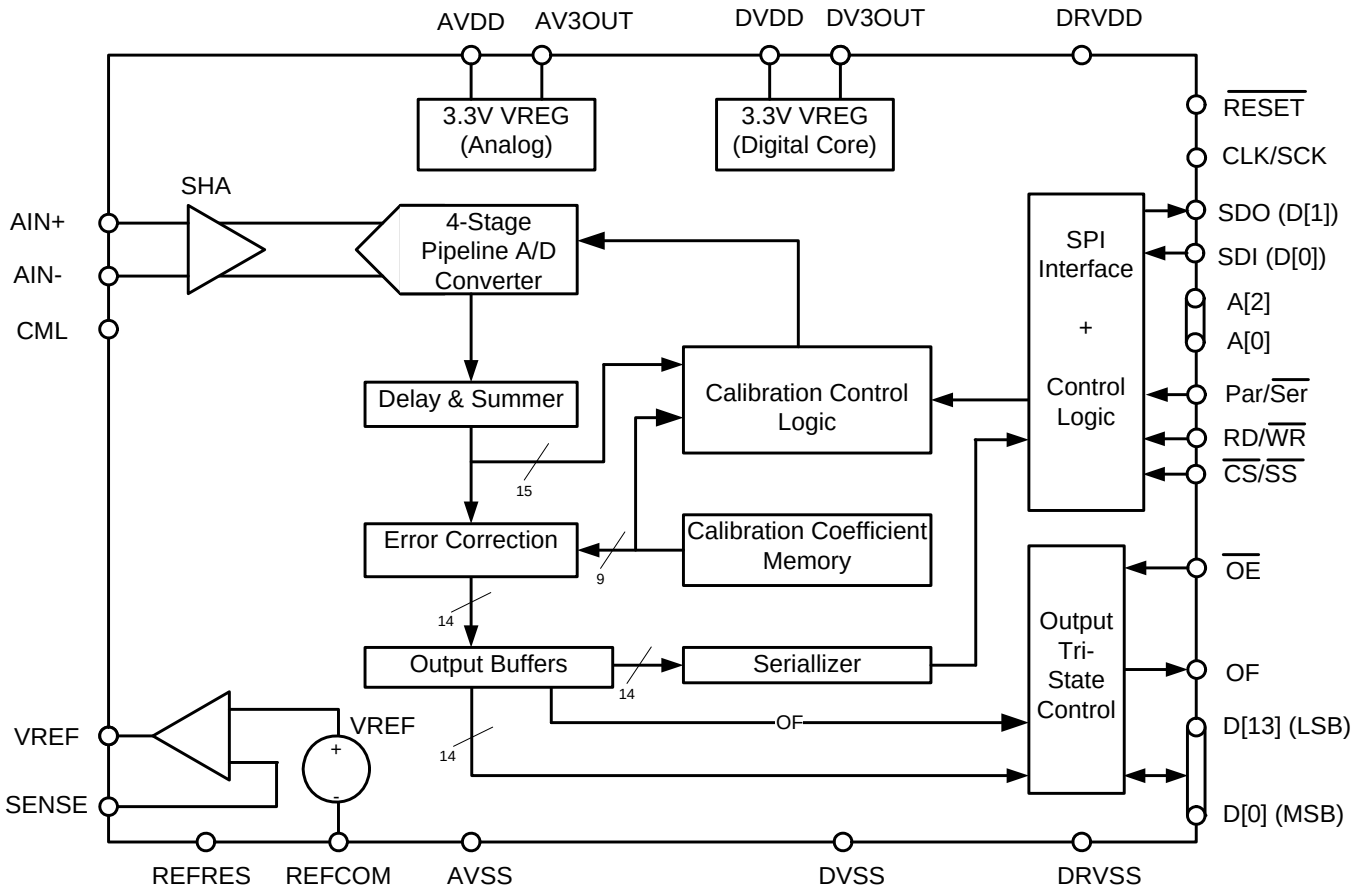
INTRODUCTION

The UT14AD03 is a RadHard 14-bit, 3MSPS analog-to-digital converter (A/D) with an internal reference, differential analog input, and an integrated sample-and-hold amplifier. This single 5V supply A/D has both parallel and serial interfaces. The parallel or serial interface may be operated at either 5V or 3.3V without a separate 3.3V supply, by connecting the DV3OUT pin to the DRVDD pin.

In parallel interface mode, the user provides a clock with the desired sample frequency. In serial interface mode, the UT14AD03 uses the SCK from the host, which must be 16x the desired sampling rate. In either case, the latency is 3.5 sample cycles.

The UT14AD03 is radiation hardened for use in multiple, harsh environment applications such as radiation therapy equipment control, nuclear power plant monitoring , and satellite telemetry.

BLOCK DIAGRAM



PACKAGE PIN OUT

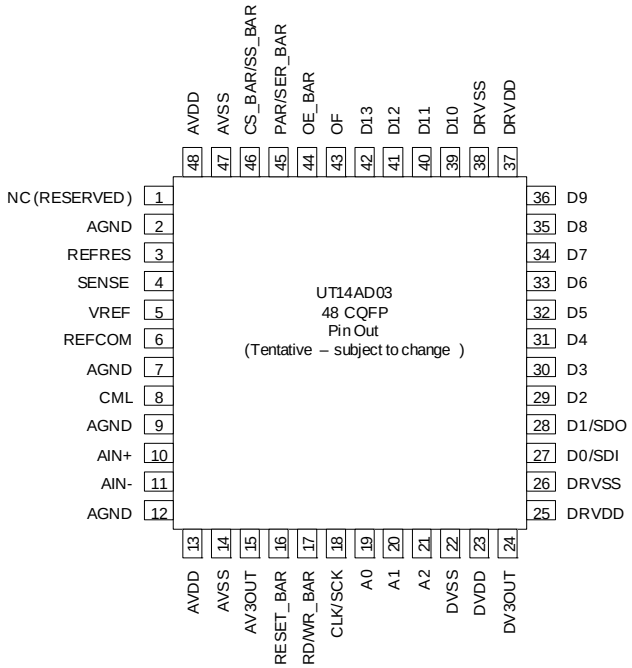


Figure 1: UT14AD03 Pin-Out (DRAFT: SUBJECT TO)

PIN FUNCTIONS (DRAFT: Pin location subject to change)

PIN	NAME	DESCRIPTION	ELECTRICAL
1	(Reserved)	Factory Use Only	Tie to 0V
2	AGND	Analog Ground	0 V
3	REFRES	Analog Bias Current Input	Resistor to AV3OUT
4	SENSE	Reference sense	
5	VREF	Analog Voltage Reference High	2.0 V
6	REFCOM	Analog Voltage Reference Low	AGND
7	AGND	Analog Ground	0 V
8	CML	Reference midpoint	Bypass to REFCOM
9	AGND	Analog Ground	0 V
10	AIN+	Analog Input	Vpp (AIN+ - AIN-) 2.0 V
11	AIN-	Inverted Analog Input	Vpp (AIN+ - AIN-) 2.0 V
12	AGND	Analog Ground	0 V
13	AVDD	Analog Power	5 V
14	AVSS	Analog Return	0 V
15	AV3OUT	Regulated Analog Voltage Output	Bypass to AVSS
16	RESET BAR	Reset	CMOS Input
17	RD/WR_BAR	Read/Write	CMOS Input
18	CLK/SCK	System Clock or SPI Clock	CMOS Input
19	A0	Address bus MSB	CMOS Input
20	A1	Address bus	CMOS Input
21	A2	Address bus LSB	CMOS Input
22	DVSS	Digital Power Return	0 V
23	DVDD	Digital Power	5 V
24	DV3OUT	Regulated Digital Voltage Output	Bypass TBD pF to DVSS
25	DRVDD	Digital Output Power	5 V or 3.3 V
26	DRVSS	Digital Output Return	0 V
27	D0 (MSB)/SDI	Parallel Digital Data I/O or SPI MOSI	CMOS bidirect
28	D1/SDO	Parallel Digital Data I/O or SPI MISO	CMOS bidirect
29	D2	Parallel Digital Data I/O	CMOS bidirect
30	D3	Parallel Digital Data I/O	CMOS bidirect
31	D4	Parallel Digital Data I/O	CMOS bidirect
32	D5	Parallel Digital Data I/O	CMOS bidirect
33	D6	Parallel Digital Data I/O	CMOS bidirect
34	D7	Parallel Digital Data I/O	CMOS bidirect

PIN	NAME	DESCRIPTION	ELECTRICAL
35	D8	Parallel Digital Data I/O	CMOS bidirect
36	D9	Parallel Digital Data I/O	CMOS bidirect
37	DRVDD	Digital Output Power	5 V or 3.3 V
38	DRVSS	Digital Output Return	5 V or 3.3 V
39	D10	Parallel Digital Data I/O	CMOS bidirect
40	D11	Parallel Digital Data I/O	CMOS bidirect
41	D12	Parallel Digital Data I/O	CMOS bidirect
42	D13 (LSB)	Parallel Digital Data I/O	CMOS bidirect
43	OF	Overflow Indicator	CMOS output
44	OE_BAR	Output Enable	CMOS Input
45	PAR/SER_BAR	Parallel or Serial Select	CMOS Input
46	CS_BAR/SS_BAR	Chip Select or SPI Slave Select	CMOS Input
47	AVSS	Analog Power Return	0 V
48	AVDD	Analog Power	5 V

ABSOLUTE MAXIMUM RATINGS

Over operating, free-air temperature range unless otherwise noted. (1)

SYMBOL	PARAMETER	LIMITS
AV_{DD} to AV_{SS}	Analog Supply Voltage	-0.3 V to 6.5 V
DV_{DD} to DV_{SS}	Digital Supply Voltage	-0.3 V to 6.5 V
AV_{SS}/DV_{SS} to AGND	Analog/Digital Return	0 V
	Reference Input Voltage Range	-0.3 V to AV_{DD} + 0.3 V
	Analog Input Voltage Range	-0.3 V to AV_{DD} + 0.3 V
	Digital Input Voltage Range	-0.3 V to DV_{DD} + 0.3 V
TQFP Package CQFP Package	Operating, free-air temperature range, T_A: Industrial Grades Military, Aerospace Grades	 $-40^oC + 85^oC$ $-55^oC + 125^oC$
T_{STG}	Un-Powered Storage Temperature	$-65^oC + 150^oC$
	Lead soldering temperature 1.6 mm (1/16 inch) from body < 10 sec	$+260^oC$

Notes:

1. Stresses beyond those listed above may result in permanent damage to the device, and will affect device reliability. Functional operation of the device, beyond those indicated below in REOMMENDED OPERATING CONDITIONS (but within ABSOLUTE MAXIMUM RATINGS) for extended periods of time, may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
Analog supply Voltage, AV_{DD} to AV_{SS}	4.5	5.0	5.5	V
Digital supply Voltage, DV_{DD} to DV_{SS}	4.5	5.0	5.5	V
I/O Supply Voltage, DRVDD TO DRVSS	3.0		5.5	V
Digital Input or Bidirect, Logic 1, (V_{IH})	2.0	DRV_{DD}	DRV_{DD}+0.3	V
Digital Input or Bidirect, Logic 0, (V_{IL})	DV_{SS} - 0.3		0.8	V
Analog Input, AIN+, AIN-	AV_{SS}		AV_{DD}	V
Analog Input, A_{IN}+ to A_{IN}-			2.0	Vpp
System Clock (1) Input frequency, f_{CLK}	0.1		3	MHz
SPI Clock (2) Input frequency, f_{CLK}	1.6		48	MHz
System Clock Duty Cycle	40	50	60	%
Free-air Operating Temperature:				
Industrial/Medical (TQFP)	-40		85	^oC
QML-Q, QML-V	-55		125	^oC

Notes:

1. CLK in Parallel Mode (PAR/SER_BAR held HIGH).
2. SCK in Serial Mode (PAR/SER_BAR held LOW).

DC ELECTRICAL CHARACTERISTICS (Pre and Post-Radiation)*

(-55°C to +125°C for (C) screening, -40°C to +125°C for (W) screening and -40°C to +85°C for Industrial/Medical screening)

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
Power					
AV_{DD} to AV_{SS}		3.0		5.5	V
DV_{DD} to DV_{SS}		3.0		5.5	V
AV_{SS}, DV_{SS} to A_{GND}	AV_{SS} AND DV_{SS} must be same potential as AGND	0.0		0.0	V
Digital Power Supply, I_{DDD}	AV_{DD} to AV_{SS} = 5.0 V, f_{CLK} = 36 MHz			TBD	mA
Analog Power Supply, I_{DDA}	DV_{DD} to DV_{SS} = 5.0 V, f_{CLK} = 36 MHz			TBD	mA
Total Power, Operating	AV_{DD} = DV_{DD} = 5.0 V, f_{CLK} = 36 MHz			100	mW
DC Characteristics					
Resolution		14		14	bits
DNL		-0.5		0.5	LSB
INL		-2		2	LSB
Offset Error (1)	$A_{IN}+$ = $A_{IN}-$ = AGND			0.3	% FSR
Gain Accuracy				2.0	% FSR
Offset Temperature Stability				TBD	ppm/°C
Gain Temperature Stability				TBD	ppm/°C
AC Characteristics					
System Clock (1)		0.1		3	MHz
SPI Clock (2)		1.6		48	MHz
Conversion Speed	Conversion Speed = CLK or SCK/16	0.1		3	MSPS
Parallel Mode t_{CLK}	Clock period	10		0.333	µs
Serial Mode t_{CLK}	Clock period	20.8		625	ns
t_{DO}		TBD		TBD	ns
t_{DIS}		TBD		TBD	ns
t_{DEN}		TBD		TBD	ns
Analog Characteristics					
Analog Input Voltage		AVSS		AVDD	V
Analog Input Voltage Span				2.0	V_{PP}
Input Referred Noise				0.5	LSB,rms
Input Impedance			10		kΩ
Input Bandwidth				TBD	MHz
ENOB		13.2			bits

PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNITS
THD	Input waveform = 100kHZ; f_{CLK} = 36 MHz		TBD		dB
	Input waveform = 1MHz; f_{CLK} = 36 MHz		TBD		dB
SNR	Input waveform = 100kHZ; f_{CLK} = 36 MHz		TBD		dB
	Input waveform = 1MHz; f_{CLK} = 36 MHz		TBD		dB
SINAD	Input waveform = 100kHZ; f_{CLK} = 36 MHz		79.4		dB
	Input waveform = 1MHz; f_{CLK} = 36 MHz		TBD		dB
PSRR	dc rejection with changing AVDD=DVDD, T_A=25C	-200		200	ppm/V
	ac rejection, 1kHZ 100mVpp on AVDD		-48		dB
Digital Characteristics					
Bidirects/Outputs, V_{OH}		2.6			V
Inputs/Bidirects, V_{IH}	for SI, SO, SCK, use DV_{DD} = 3.3V	2.0		DV_{DD}+0.3	V
Bidirects/Outputs, V_{OL}				0.4	V
Inputs/Bidirects, V_{IL}		DV_{SS}-0.3		0.8	V
Bidirect/Output Current, I_{OH}	output load = 10 pF		50		µA
Input Capacitance	DV_{DD} = 5.5 V			10	pF
Output Capacitance	DV_{DD} - 5.5 V		5		pF

Notes:
1. CLK frequency with PAR/SER_BAR tied HIGH.
2. SCK frequency with PAR/SER_BAR tied LOW.
3. Specifications subject to change without notice.

PARALLEL INTERFACE OPERATION

For normal operation (reading converted data) in parallel interface mode, the PAR/SER_BAR pin is held HIGH, the RD/WR_BAR pin is held HIGH, and CS_BAR/SS_BAR is held LOW. The pipeline A/D performs a new conversion every CLK cycle, with maximum conversion rate of 3 MSPS. The pipeline latency is 3.5 samples (i.e. a new conversion result appears at the digital outputs 3.5 CLK cycles after the analog input signal was sampled. Details are shown in Figure 3.

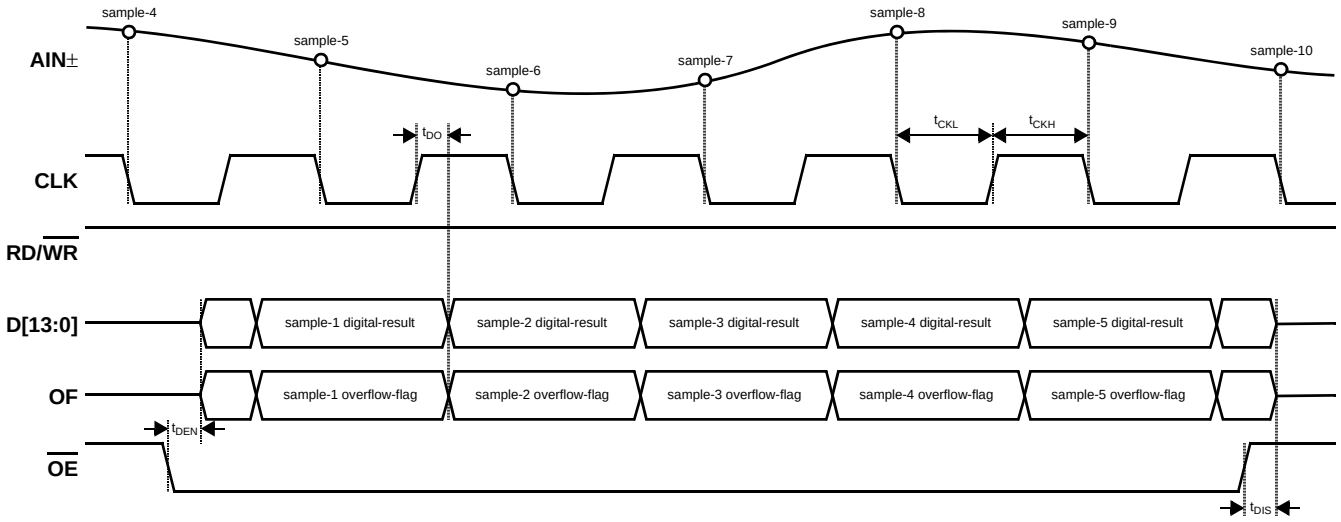


Figure 2: Parallel Interface Timing Diagram for Normal Data Conversion (Read) Mode

SERIAL INTERFACE OPERATION

For normal operation (reading converted data) in serial interface mode, the PAR/SER_BAR pin is held LOW, the RD/WR_BAR pin is held HIGH, and CS_BAR/SS_BAR is held LOW. The pipeline A/D performs a new conversion every 16 SCK cycles. The pipeline latency is 3.5 samples (i.e. a new conversion result appears at the digital outputs 56 SCK cycles after the analog input signal was sampled.) The next revision of this datasheet will give details on burst mode data conversion using the SPI.

CONVERSION TIMING USING PARALLEL INTERFACE

The UT14AD03's pipelined A/D architecture performs a new conversion at every CLK cycle, with maximum *conversion rate* of 4 MSPS. The conversion *latency* is 3.5 samples (i.e. a new conversion result appears at the digital outputs 3.5 CLK cycles after the analog input signal was sampled). Pipelined conversion reads are shown in Figure 3, which also depicts output-enable ($\overline{OE}$) behavior.

CONFIGURATION TIMING USING PARALLEL INTERFACE

The UT14AD03 supports a variety of configuration options, and supports write operations into an *addressed* register set. To help minimize pin count, the address of a target register is internally latched from the 6 LSBs of data bus D[5:0] during an address-latch cycle (via pin ALE); note that $\overline{CS}$ is also latched at this time. As long as the address is not 00 (the address for A/D conversion results), asserting OF high during an ALE cycle will *auto-increment* the internally-latched address for the following read or write. Note that all inputs - except for $\overline{OE}$ - are registered at CLK-rise, and until changed via ALE, the internally-latched address defaults to 00 (the address for A/D conversion results).

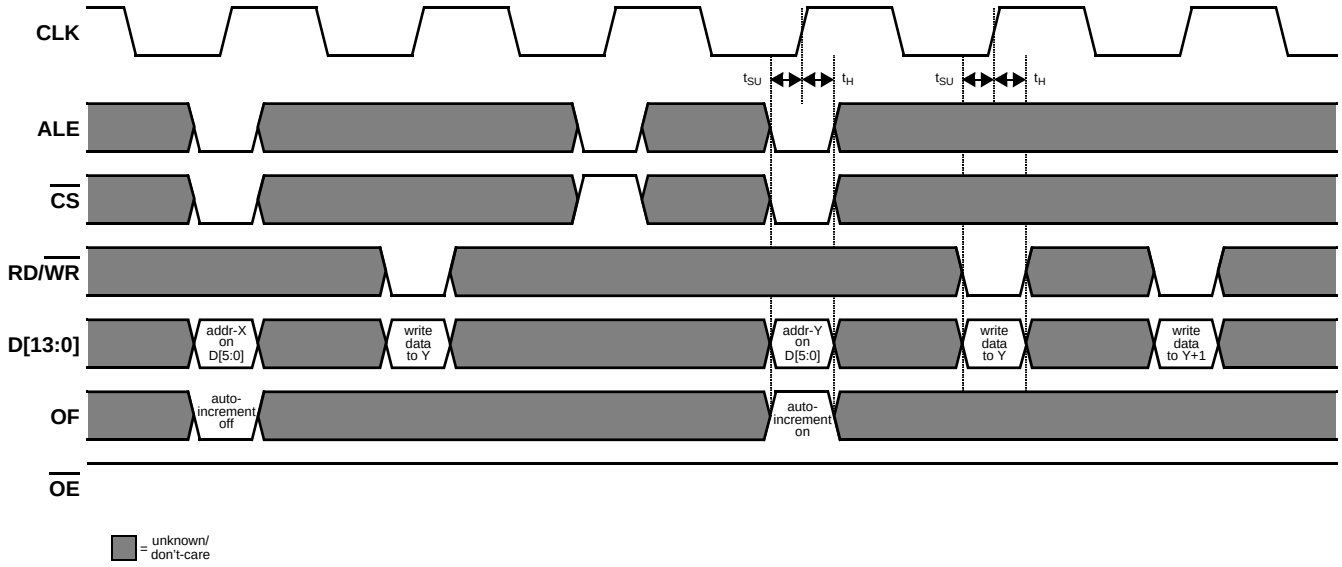


Figure 3: Parallel Interface Timing Digram for Configuration Writes

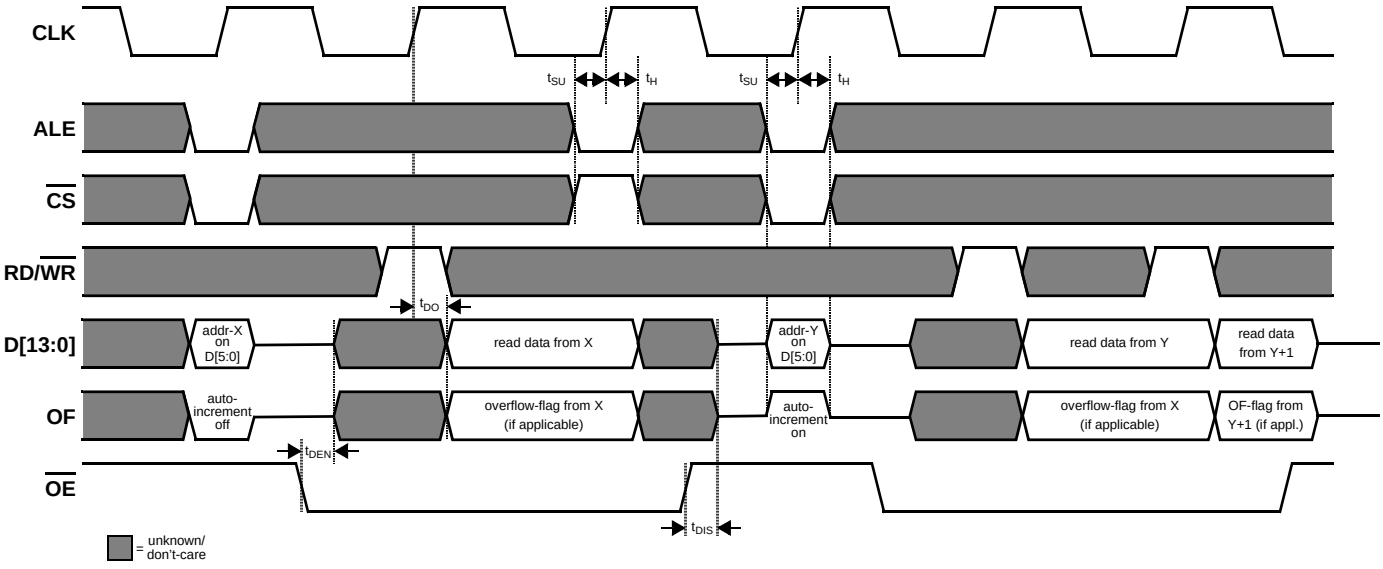


Figure 4: Parallel Interface Timing Digram for Configuration Reads

Conversion Timing Using Serial Peripheral Interface (SPI)

Conversions in UT14AD03 always exhibit a one-transfer *latency*, in that the signal level sampled at the beginning of one transfer will cause the resulting conversion read-data to appear on SDO during the *following* transfer.

UT14AD03's SPI interface is designed to support *cascading* of devices - UT14AD03 behaves like a *16-bit-long serial-shift-register*, and input data appearing at SDI will simply exit out of UT14AD03's SDO pin (feeding a downstream device) after UT14AD03's own 16 bits of conversion read-data.

The UT14AD03 supports a *burst transfer mode*, where cascaded operation (see above) is temporarily disabled and continuous conversions occur every 16 SCK cycles. *If burst mode was initiated by a read command*, then the mode will be exited once $\overline{SS}$ is released (but note that the last 16 bits of SDI will be acted-upon - see next section); however, *if burst mode was initiated due to a configuration setting*, then it will re-start with the next transfer.

The analog input is always sampled at the first rising-edge of SCK after $\overline{SS}$ becomes active-low, and (if in burst mode) at the rising-edge of every 16th SCK cycle thereafter; however, note there is a slight delay (t_{SH}) between the external SCK edge and the internal sampling point (note this is not the same as aperture delay, which is also related to the signal-path delay to the S/H circuit).

Byte-level odd-parity bits are included in transmitted UT14AD03 serial data. Note that for cascaded operation, SDI data passed-through to SDO will not be altered for parity or for any other reason.

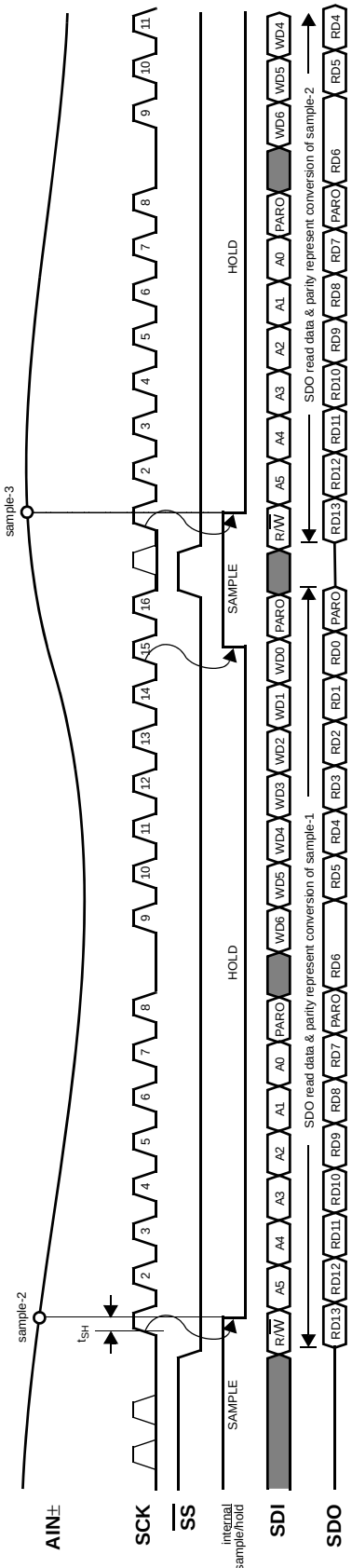


Figure 5: Two non-cascaded, non-burst conversion transfers depicts latency between input samples and SDO read-data

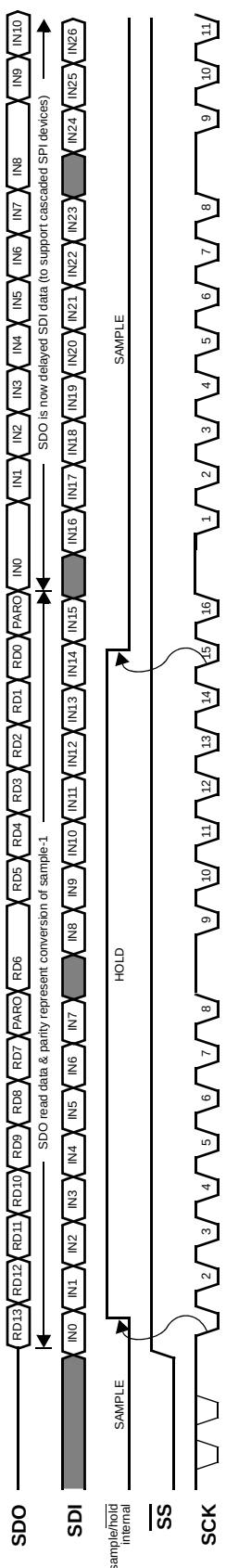


Figure 6: A cascaded, non-burst conversion transfer depicts the 16-bit shift-register behavior from SDI to SDO.

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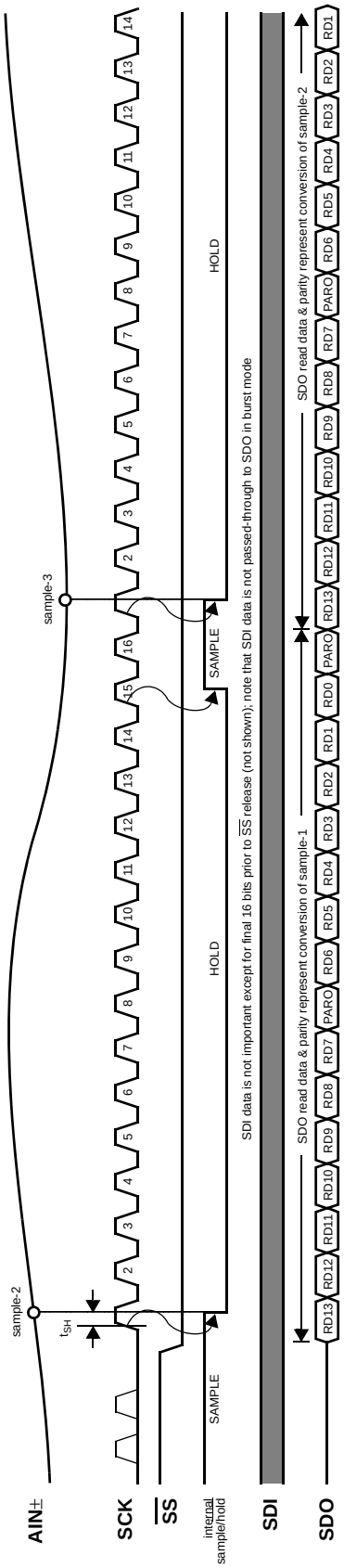


Figure 7: A burst transfer (*never* cascaded) depicts burst-mode sampling and transfer behavior.

Configuration Timing Using Serial Peripheral Interface (SPI)

UT14AD03's SPI interface is designed to support *cascading* of devices - UT14AD03 behaves like a *16-bit-long serial-shift-register*, and the most recent 16-bits appearing at SDI (the extended-address plus write-data) will be acted-upon when $\overline{SS}$ is released. Thus, any SDI data *prior to the last 16 bits* simply exit out of UT14AD03's SDO pin (feeding a downstream device) after UT14AD03's own 16 bits of read data, and are *ignored* by UT14AD03.

Configuration reads from UT14AD03 always exhibit a one-transfer *latency*, in that an addressed configuration-read during a transfer will cause the resulting read-data to appear on SDO during the *following* transfer. If the SDI data during that second transfer is another read, then this *pipelined* read behavior will be continued (but could instead be a valid write). Note that this behavior is similar to the one-transfer latency of a sampling-event versus the readout of corresponding conversion results.

Note again that byte-level odd-parity bits are included in both received and transmitted UT14AD03 serial data; if received data fails parity, then that command will be ignored (the SDO data for the transfer is unaffected) and non-burst conversion operation will resume. Note that for cascaded operation, SDI data passed-through to SDO will not be altered for parity or for any other reason.

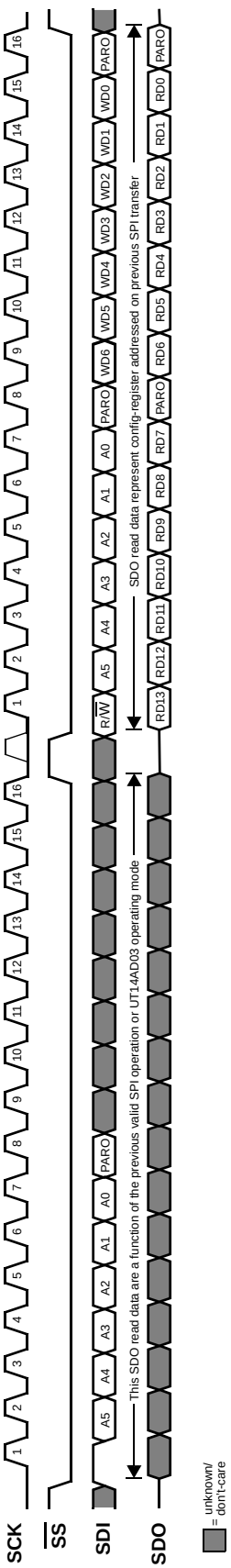


Figure 8: A non-cascaded read operation depicts the one-transfer latency before read-data appears on SDO.

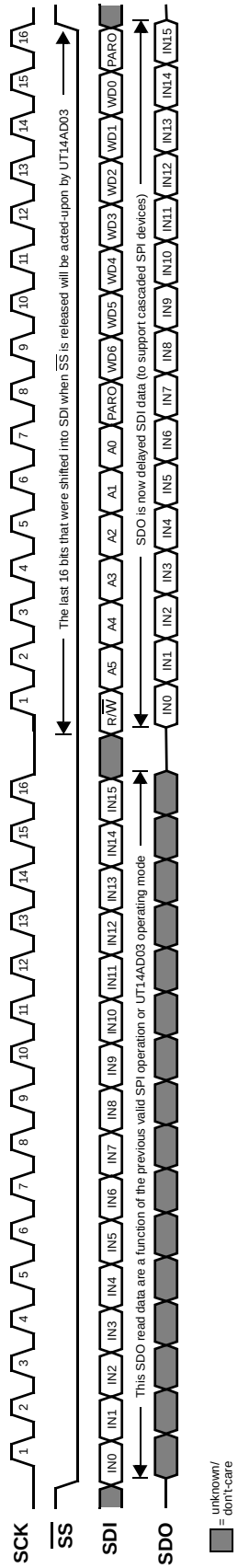
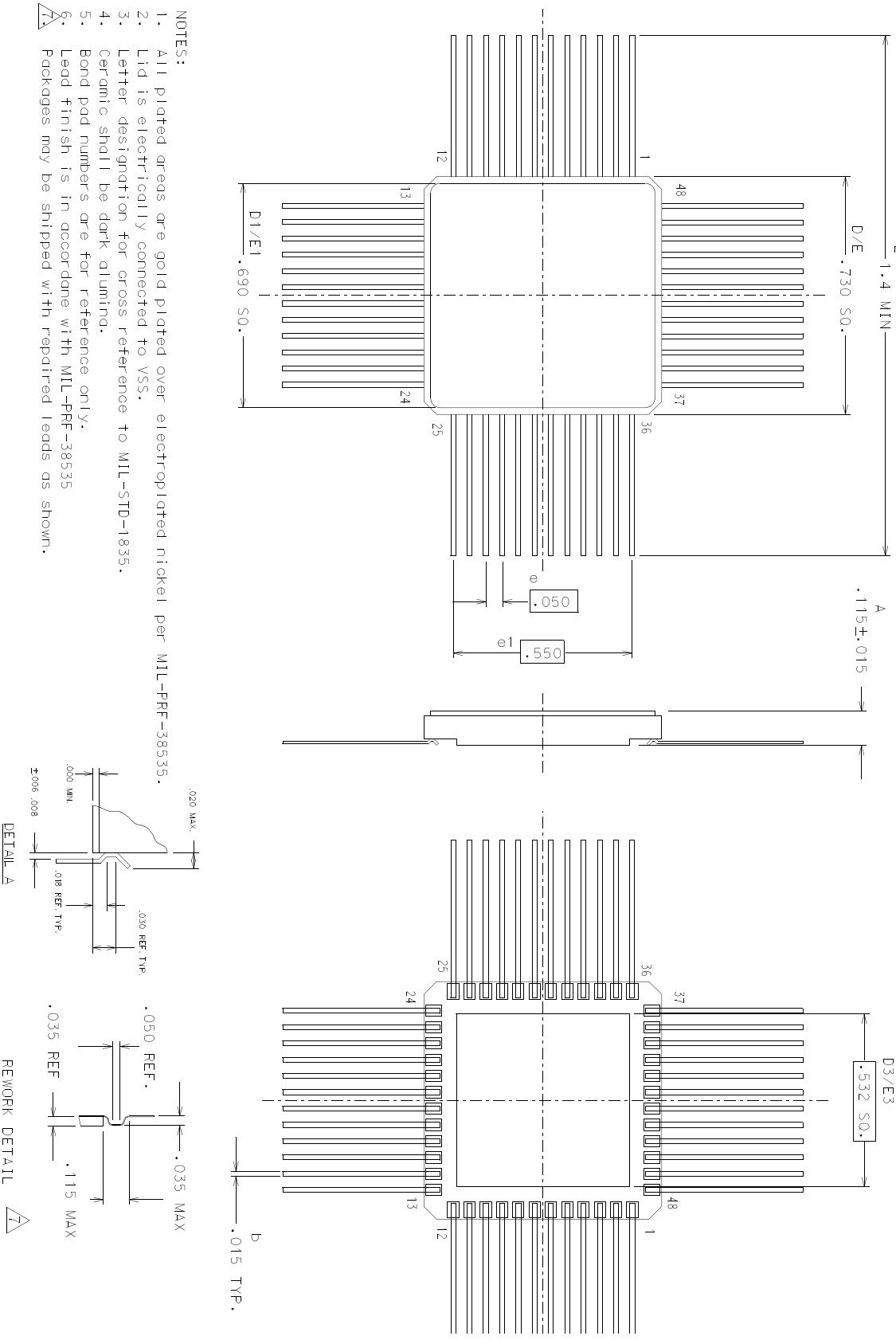


Figure 9: A cascaded configuration depicts the 16-bit shift-register behavior from SDI to SDO, as well as the last 16-bits into SDI being acted-upon by the device when SS is released.

Packaging

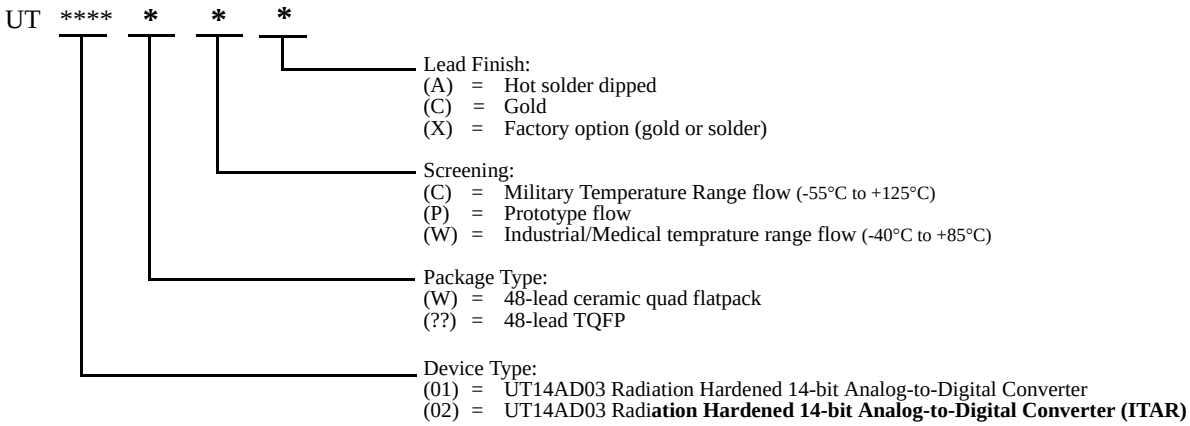


NOTES:

1. All plated areas are gold plated over electroplated nickel per MIL-PRF-38535.
2. Lid is electrically connected to VSS.
3. Letter designation for cross reference to MIL-STD-1835.
4. Ceramic shall be dark alumina.
5. Bond pad numbers are for reference only.
6. Lead finish is in accordane with MIL-PRF-38535
7. Packages may be shipped with repaired leads as shown.

ORDERING INFORMATION

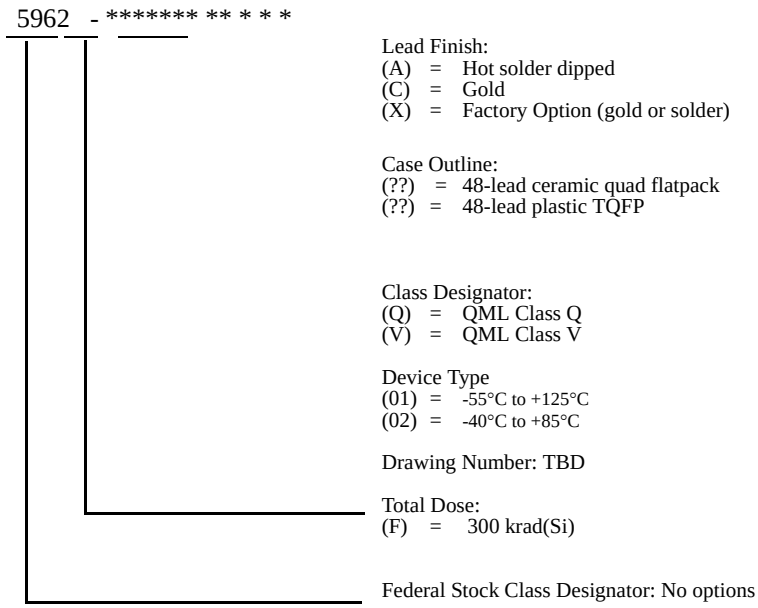
UT14AD03



Notes:

1. Lead finish (A,C, or X) must be specified.
2. If an "X" is specified when ordering, then the part marking will match the lead finish and will be either "A" (solder) or "C" (gold).
3. Prototype flow per Aeroflex Colorado Springs Manufacturing Flows Document. Tested at 25°C only. Lead finish is GOLD ONLY. Radiation neither tested nor guaranteed.
4. Military Temperature Range flow per Aeroflex Colorado Springs Manufacturing Flows Document. Devices are tested at -55°C,

UT14AD03: SMD



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Aeroflex Colorado Springs - Datasheet Definition

Advanced Datasheet - Product In Development

Preliminary Datasheet - Shipping Prototype

Datasheet - Shipping QML & Reduced Hi-Rel

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