

CMOS DUAL 4-STAGE SHIFT REGISTER

FEATURES

- ◆ Serial Input/Parallel Output
- ◆ Direct Reset
- ◆ Two Independent Sections
- ◆ Fully Static Operation - DC to 5MHz @ 10Vdc

DESCRIPTION

The 4015B consists of two identical, independent, 4-stage Serial-Input/Parallel-Output Registers. Each register has independent Clock and Reset inputs as well as a single serial Data input. Q outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the Data input is transferred into the first register stage and shifted right one stage at each positive-going Clock transition. Resetting of all stages is accomplished by a high level on the Reset line. Register expansion to 8 stages using one 4015B package, or to more than 8 stages using additional 4015B's, is possible.

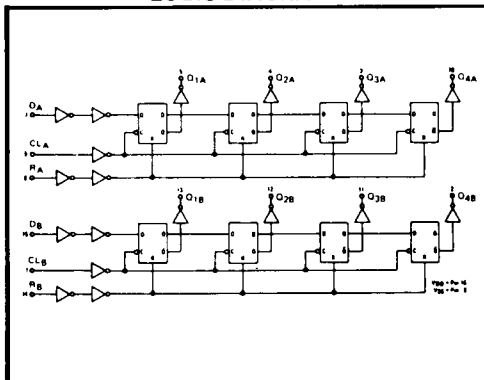
TRUTH TABLE

CL*	D	R	Q ₁	Q _n
	0	0	0	Q _{n-1}
	1	0	1	Q _{n-1}
	X	0	Q ₁	Q _n
X	X	1	0	0

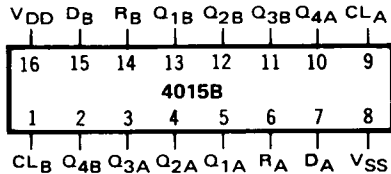
(NO CHANGE)

* = LEVEL CHANGE
X = DON'T CARE

LOGIC DIAGRAM



CONNECTION DIAGRAM (all packages)



Add suffix for package:

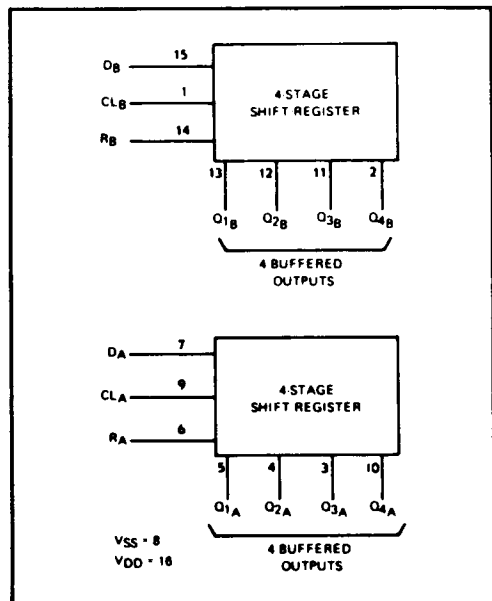
- C 16-pin Cerdip
- D 16-pin Ceramic
- E 16-pin Epoxy
- F 16-pin Flat
- H Chip

RECOMMENDED OPERATING CONDITIONS

For maximum reliability:

DC Supply Voltage	V _{DD} - V _{SS}	3 to 15	Vdc
Operating Temperature	T _A	-55 to +125	°C
C, D, F, H Device		-40 to +85	°C

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

STATIC CHARACTERISTICS¹

PARAMETER	V _{DD} (Vdc)	CONDITIONS	T _{LOW} ²		+25°C			T _{HIGH} ²		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	V _{DD}	V _{IN} =V _{SS} or V _{DD} All valid input combinations	—	5	—	0.05	5	—	150	μAdc
			—	10	—	0.1	10	—	300	
			—	15	—	0.2	20	—	600	

NOTES: ¹ Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

² T_{LOW} = -55°C for C, D, F, H device.

= -40°C for E device.

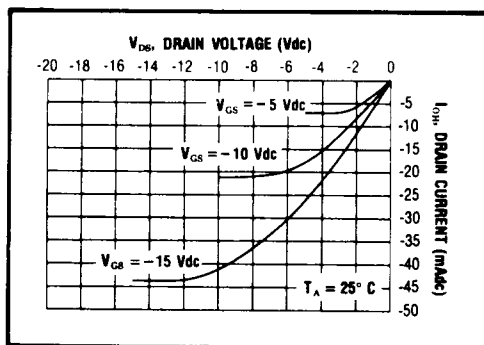
T_{HIGH} = +125°C for C, D, F, H device.

= + 85°C for E device.

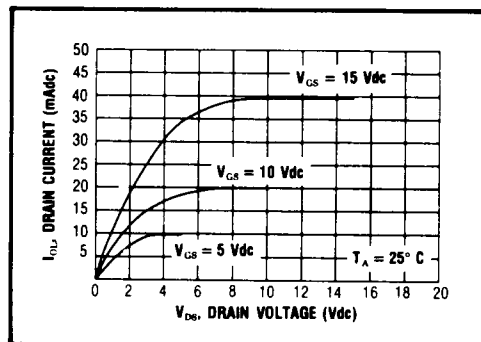
DYNAMIC CHARACTERISTICS (C_L = 50pF, T_A = 25°C)

PARAMETER		V _{DD} (Vdc)	Min.	Typ.	Max.	Units
CLOCKED OPERATION						
PROPAGATION DELAY TIME	t _{PLH} , t _{PHL}	5	—	250	500	ns
		10	—	100	200	
		15	—	90	180	
OUTPUT TRANSITION TIME	t _{TLH} , t _{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM CLOCK PULSE WIDTH	PW _{CL}	5	—	200	400	ns
		10	—	100	200	
		15	—	80	160	
MAXIMUM CLOCK FREQUENCY	f _{CL}	5	1.25	2.5	—	MHz
		10	2.5	5.0	—	
		15	3.0	6.0	—	
MAXIMUM CLOCK RISE AND FALL TIME ¹	t _{rCL} , t _{fCL}	5	15	—	—	μs
		10	15	—	—	
		15	5	—	—	
MINIMUM DATA INPUT DATA SETUP TIME	t _{setup}	5	—	150	300	ns
		10	—	50	100	
		15	—	40	80	
MINIMUM DATA INPUT HOLD TIME	t _{hold}	5	—	0	50	ns
		10	—	0	25	
		15	—	0	15	
RESET OPERATION						
PROPAGATION DELAY TIME	t _{PHL}	5	—	200	400	ns
		10	—	100	200	
		15	—	90	180	
MINIMUM RESET PULSE WIDTH	PW _R	5	—	200	400	ns
		10	—	80	160	
		15	—	60	120	
RESET REMOVAL TIME	t _{rem}	5	—	375	750	ns
		10	—	125	250	
		15	—	100	200	

¹ When units are cascaded, the maximum rise and fall times of the clock input should be equal to or less than the transition times of the data outputs driving data inputs, plus the propagation delay of the output driving stage for the output capacitive load.



Typical P-Channel
Source Current Characteristics



Typical N-Channel
Sink Current Characteristics