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NTE4018B
Integrated Circuit
CMOS, Presettable Divide–By–N Counter
16–Lead DIP Type Package

Description:

The NTE4002B contains five Johnson counter stages which are asynchronously presettable and resettable. The counters are synchronous, and increment on the positive going edge of the clock.

Presetting is accomplished by a logic “1” on the preset enable input. Data on the Jam inputs will then be transferred to their respective $\overline{Q}$ outputs (inverted). A logic “1” on the reset input will cause all $\overline{Q}$ outputs to go to a logic “1” state.

Division by any number from 2 to 10 can be accomplished by connecting appropriate $\overline{Q}$ outputs to the data input, as shown in the Function Selection table. Anti–lock gating is included in the NTE4018B to assure proper counting sequence.

Features:

- Fully Static Operation
- Schmitt Trigger on Clock Input
- Capable of Driving Two Low–Power TTL Loads or One Low–Power Schottky TTL Load Over the Rated Temperature Range

Absolute Maximum Ratings: (Voltages referenced to V_{SS}, Note 1)

DC Supply Voltage, V_{DD} . . . . . –0.5 to +18.0V
Input Voltage (DC or Transient), V_{in} . . . . . –0.5 to V_{DD} to +0.5V
Output Voltage (DC or Transient), V_{out} . . . . . –0.5 to V_{DD} to +0.5V
Input Current (DC or Transient, Per Pin), I_{in} . . . . . ±10mA
Output Current (DC or Transient, Per Pin), I_{out} . . . . . ±10mA
Power Dissipation (Per Package), P_D 500mW
Temperature Derating (from +65° to +125°C) . . . . . –7.0mW/°C
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 8sec max), T_L . . . . . +260°C

Note 1. Maximum Ratings are those values beyond which damage to the device may occur.

Electrical Characteristics: (Voltages referenced to V_{SS}, Note 2)

Parameter	Symbol	V_{DD} Vdc	−55°C		+25°C			+125°C		Unit
			Min	Max	Min	Typ	Max	Min	Max	
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0		10	–	0.05	–	0	0.05	–	0.05	Vdc
		15	–	0.05	–	0	0.05	–	0.05	Vdc
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	Vdc
		15	14.95	–	14.95	15	–	14.95	–	Vdc
Input Voltage "0" Level	V_{IL}									
(V_O = 4.5 or 0.5Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
(V_O = 9.0 or 1.0Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	Vdc
(V_O = 13.5 or 1.5Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	Vdc
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	Vdc
(V_O = 1.5 or 13.5Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	Vdc
Output Drive Current Source	I_{OH}									
(V_{OH} = 2.5Vdc)		5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
(V_{OH} = 4.6Vdc)		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	mAdc
(V_{OH} = 9.5Vdc)		10	–1.6	–	–1.3	–2.25	–	–0.9	–	mAdc
(V_{OH} = 13.5Vdc)		15	–4.2	–	–3.4	–8.8	–	–2.4	–	mAdc
Sink	I_{OL}									
(V_{OL} = 0.4Vdc)		5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	mAdc
(V_{OL} = 1.5Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	mAdc
Input Current	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance (V_{IN} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	µAdc
		15	–	20	–	0.015	20	–	600	µAdc
Total Supply Current (Dynamic plus Quiescent, Per Package, C_L = 50pF on all buffers switching, Note 3, Note 4)	I_T	5.0	I_T = (0.3µA/kHz) f + I_{DD}							µAdc
		10	I_T = (0.7µA/kHz) f + I_{DD}							µAdc
		15	I_T = (1.0µA/kHz) f + I_{DD}							µAdc

Note 2. Data labeled "Typ" is not to be used for design purposes but is intended as an indication of the device's potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Note 4. To calculate total supply current at loads other than 50pF:

$$I_T(C_L) = I_T(50pF) + (C_L - 50)\ V_{fk}$$

where: I_T is in µA (per package), C_L in pF, V = (V_{DD} − V_{SS}) in volts, f in kHz is input frequency, and k = 0.001.

Switching Characteristics: (C_L = 50pF, T_A = +25°C, Note 2)

Parameter	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}					
t_{TLH}, t_{THL} = (1.35ns/pf) C_L + 32ns		5.0	–	100	200	ns
t_{TLH}, t_{THL} = (0.60ns/pf) C_L + 20ns		10	–	50	100	ns
t_{TLH}, t_{THL} = (0.40ns/pf) C_L + 20ns		15	–	40	80	ns
Propagation Delay Time	t_{PLH}. t_{PHL}					
Clock to $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 265ns		5.0	–	310	620	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 102ns		10	–	120	240	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 72ns		15	–	85	170	ns
Reset to $\overline{Q}$						
t_{PLH} = (0.90ns/pf) C_L + 325ns		5.0	–	370	740	ns
t_{PLH} = (0.36ns/pf) C_L + 132ns		10	–	150	300	ns
t_{PLH} = (0.26ns/pf) C_L + 81ns		15	–	100	200	ns
Preset Enable to $\overline{Q}$						
t_{PLH}, t_{PHL} = (0.90ns/pf) C_L + 325ns		5.0	–	370	740	ns
t_{PLH}, t_{PHL} = (0.36ns/pf) C_L + 132ns		10	–	150	300	ns
t_{PLH}, t_{PHL} = (0.26ns/pf) C_L + 81ns		15	–	100	200	ns
Setup Time	t_{su}					
Data (Pin1) to Clock		5.0	200	0	–	ns
		10	100	0	–	ns
		15	80	0	–	ns
Jam Inputs to Preset Enable		5.0	200	0	–	ns
		10	100	0	–	ns
		15	80	0	–	ns
Data (Jam Inputs)–to–Preset Enable Hold Time	t_h	5.0	540	270	–	ns
		10	500	250	–	ns
		15	480	240	–	ns
Clock Pulse Width	t_{WH}	5.0	400	200	–	ns
		10	200	100	–	ns
		15	160	80	–	ns
Reset or Preset Enable Pulse Width	t_{WH}	5.0	290	145	–	ns
		10	130	65	–	ns
		15	110	55	–	ns
Clock Rise and Fall Time	t_{TLH}, t_{THL}	5.0	No Limit			ns
		10				ns
		15				ns
Clock Pulse Frequency	f_{CL}	5.0	–	2.5	1.25	MHz
		10	–	6.5	3.25	MHz
		15	–	8.0	4.0	MHz

Note 2. Data labeled “Typ” is not to be used for design purposes but is intended as an indication of the device’s potential performance.

Note 3. The formulas given are for the typical characteristics only at +25°C.

Functional Truth Table

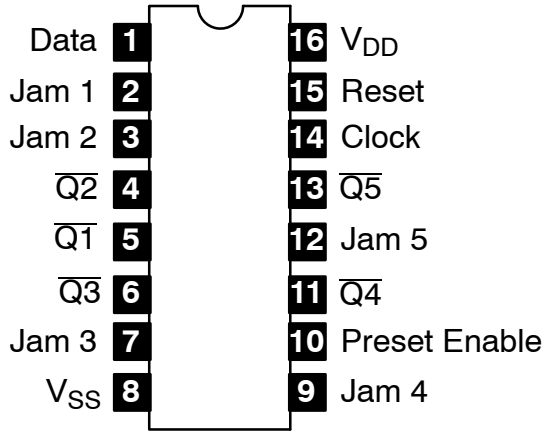
Clock	Reset	Preset Enable	Jam Input	Q_n
↓	0	0	X	$\overline{Q}_n$
↑	0	0	X	$\overline{D}_n$ *
X	0	1	0	1
X	0	1	1	0
X	1	X	X	1

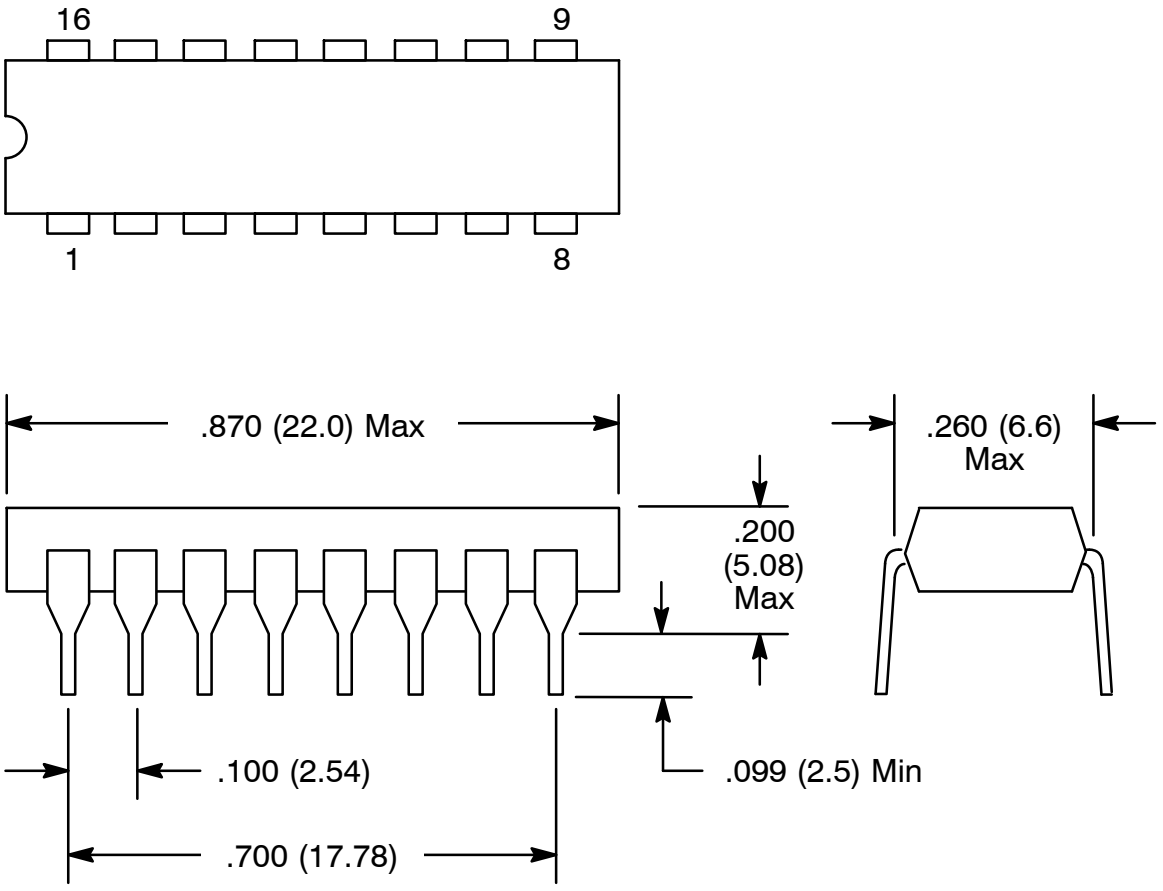
* D_n is the Data Input for the stage. Stage 1 has Data brought out to Pin1.

Functional Selection

Counter Mode	Connect Data Input (Pin1) to:	Comments
Divide by 10	$\overline{Q}_5$	No external components needed
Divide by 8	$\overline{Q}_4$	
Divide by 6	$\overline{Q}_3$	
Divide by 4	$\overline{Q}_2$	
Divide by 2	$\overline{Q}_1$	
Divide by 9	$\overline{Q}_5 \bullet \overline{Q}_4$	Gate package needed to provide AND function. Counter Skips all 1's state
Divide by 7	$\overline{Q}_4 \bullet \overline{Q}_3$	
Divide by 5	$\overline{Q}_3 \bullet \overline{Q}_2$	
Divide by 3	$\overline{Q}_2 \bullet \overline{Q}_1$	

Pin Connection Diagram




16
9
1
8
.870 (22.0) Max
.260 (6.6)
Max
.200
(5.08)
Max
.100 (2.54)
.099 (2.5) Min
.700 (17.78)