Integrated Device Technology, Inc.

CMOS STATIC RAM 64K (8K x 8-BIT)

IDT 7164S
IDT 7164L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select access time
  - Military: 25/30/35/45/55/70/85/100/120/150/200ns (max.)
  - Commercial: 19/20/25/30/35/45ns (max.)
- Low power consumption
  - IDT7164S
    Active: 300mW (typ.)
    Standby: 100μw (typ.)
  - IDT7164L
    Active: 250mW (typ.)
    Standby: 30μw (typ.)
- Battery backup operation – 2V data retention voltage (L Version only)
- Produced with advanced CEMOS™ high-performance technology
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Three-state output
- Static operation: no clocks or refresh required
- Available in standard 28-pin DIP (600 mil), 28-pin THINDIP (300 mil), 28-pin LCC, 32-pin LCC and PLCC and 28-pin SOIC
- Pin-compatible with standard 64K static RAM and EPROM
- Military product available compliant to MIL-STD-883, Class B
- Standard Military Drawing# 5962-85525 is listed on this function. Refer to Section 2/page 2-2.

DESCRIPTION:

The IDT7164 is a 65,536 bit high-speed static RAM organized as 8K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. Timing parameters have been specified to meet the demands of the fastest IDT79R3000 RISC processors.

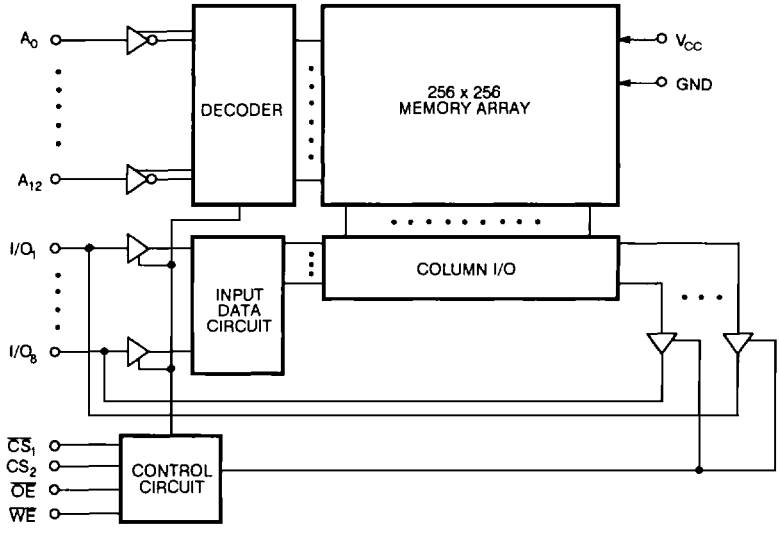
Address access times as fast as 19ns are available with typical power consumption of only 250mW. The circuit also offers a reduced power standby mode. When $\overline{CS}_1$ goes high or CS_2 goes low, the circuit will automatically go to, and remain in, a low-power standby mode. In the full standby mode, the low-power device typically consumes less than 30μW. The low-power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 10μW operating off a 2V battery.

All inputs and outputs of the IDT7164 are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT7164 is packaged in a 28-pin, 300 mil THINDIP; 28-pin, 600 mil DIP; 32-pin LCC and PLCC and 28-pin LCC and SOIC (gull-wing and J-bend), providing high board-level packing densities.

Military grade product is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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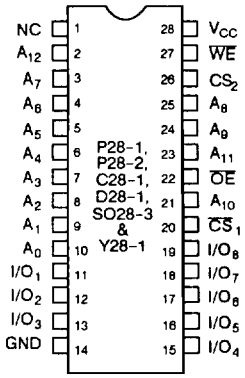
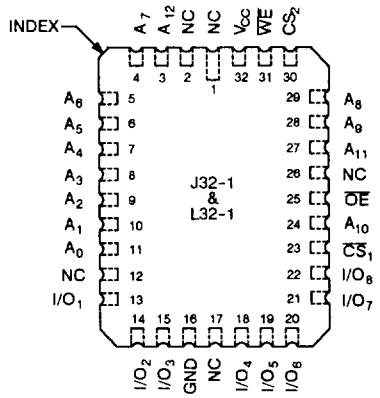
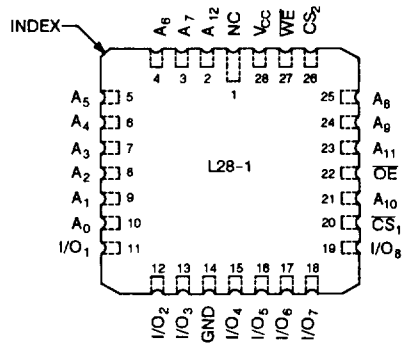
PIN CONFIGURATIONS



DIP/SOIC
TOP VIEW

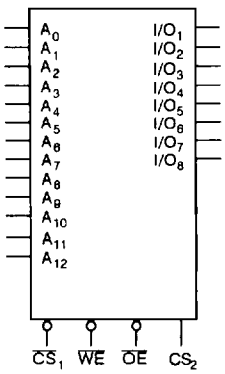


32-PIN LCC/PLCC
TOP VIEW



28-PIN LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0- A_{12}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}_1$	Chip Select	GND	Ground
CS_2	Chip Select	V_{CC}	Power

ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	–	0.8	V

NOTE:

1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT7164S MIN.	IDT7164S TYP.[1]	IDT7164S MAX.	IDT7164L MIN.	IDT7164L TYP.[1]	IDT7164L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}_1$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 10mA, V_{CC} = Min.		–	–	0.5	–	–	0.5	V
		I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:

1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS [1]

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	7164S19/20 7164L20 COM'L.	7164S19/20 7164L20 MIL.	7164S25[4] 7164L25[4] COM'L.	7164S25[4] 7164L25[4] MIL.	7164S30 7164L30 COM'L.	7164S30 7164L30 MIL.	7164S35 7164L35 COM'L.	7164S35 7164L35 MIL.	7164S45 7164L45 COM'L.	7164S45 7164L45 MIL.	7164S55 7164L55 COM'L.	7164S55 7164L55 MIL.	7164S70 7164L70 COM'L.	7164S70 7164L70 MIL.	7164S85[2] 7164L85[2] COM'L.	7164S85[2] 7164L85[2] MIL.	UNIT
I_{CC1}	Operating Power Supply Current, $\overline{CS}_1$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = 0[3]	S	100	–	90	110	90	100	90	100	90	100	–	100	–	100	–	100	mA
		L	90	–	80	100	80	90	80	90	80	90	–	90	–	90	–	90	
I_{CC2}	Dynamic Operating Current, $\overline{CS}_1$ = V_{IL}, Outputs Open, CS_2 = V_{IH} V_{CC} = Max., f = f_{MAX}[3]	S	190	–	170	190	160	170	150	160	150	160	–	160	–	160	–	160	mA
		L	170	–	150	170	140	150	130	140	120	130	–	125	–	120	–	120	
I_{SB}	Standby Power Supply Current (TTL Level), f = f_{MAX}[3], $\overline{CS}_1$ ≥ V_{IH}, or CS_2 ≥ V_{IL}, V_{CC} = Max., Outputs Open	S	20	–	20	20	20	20	20	20	20	20	–	20	–	20	–	20	mA
		L	3	–	3	5	3	5	3	5	3	5	–	5	–	5	–	5	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) f = 0[3] 1. $\overline{CS}_1$ ≥ V_{HC} and CS_2 ≥ V_{HC} 2. CS_2 ≤ V_{LC}, V_{CC} = Max.	S	15	–	15	20	15	20	15	20	15	20	–	20	–	20	–	20	mA
		L	0.2	–	0.2	1.0	0.2	1.0	0.2	1.0	0.2	1.0	–	1.0	–	1.0	–	1.0	

NOTES:

1. All values are maximum guaranteed values.
2. Also available: 100, 120, 150 and 200ns military devices.
3. At f = f_{MAX} address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.
4. Military values are preliminary only.

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

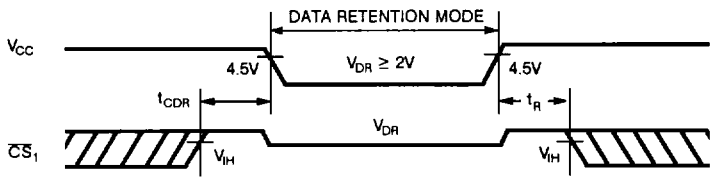
SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	1. $\overline{CS}_1 \geq V_{HC}$, $CS_2 \geq V_{HC}$ 2. $CS_2 \leq V_{LC}$	MIL.	–	10	15	200	300	µA
			COM'L.	–	10	15	60	90	
t_{CDR}	Chip Deselect to Data Retention Time			0	–		–		ns
t_R	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$(3)	Input Leakage Current			–	–		2		µA

NOTES:

1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not tested.

4

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

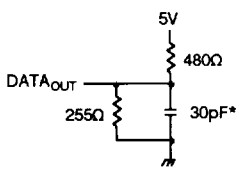


Figure 1. Output Load

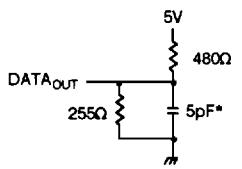


Figure 2. Output Load
(for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig.

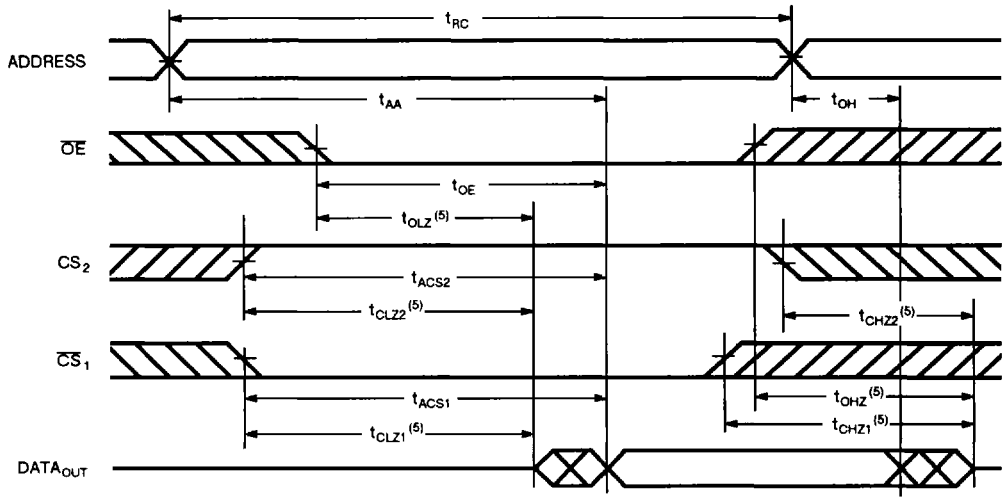
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S19/20[1] 7164L20[1]		7164S25 7164L25		7164S30 7164L30		7164S35 7164L35		7164S45 7164L45		7164S55[2] 7164L55[2]		7164S70[2] 7164L70[2]		7164S85[2] 7164L85[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	–	ns
t_{AA}	Address Access Time	–	19/20	–	25	–	29	–	35	–	45	–	55	–	70	–	85	ns
t_{ACS1}	Chip Select-1 Access Time[3]	–	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	ns
t_{ACS2}	Chip Select-2 Access Time[3]	–	25	–	30	–	35	–	40	–	45	–	55	–	70	–	85	ns
$t_{CLZ1,2}$	Chip Select-1, 2 to Output in Low Z[4]	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	12	–	15	–	18	–	25	–	30	–	35	–	40	ns
t_{OLZ}	Output Enable to Output in Low Z[4]	3	–	3	–	3	–	3	–	3	–	3	–	3	–	3	–	ns
$t_{CHZ1,2}$	Chip Select-1, 2 to Output in High Z[4]	–	9	–	13	–	13	–	15	–	20	–	25	–	30	–	35	ns
t_{OHZ}	Output Disable to Output in High Z[4]	–	8	–	10	–	12	–	15	–	20	–	25	–	30	–	35	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}	Chip Select to Power Up Time[4]	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}	Chip Select to Power Down Time[4]	–	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	ns

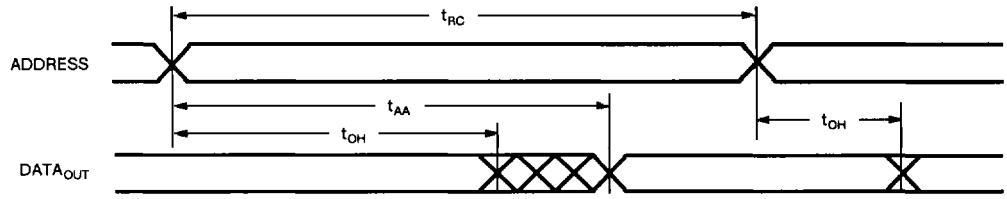
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. Both chip selects must be active for the device to be selected.
4. This parameter guaranteed but not tested.

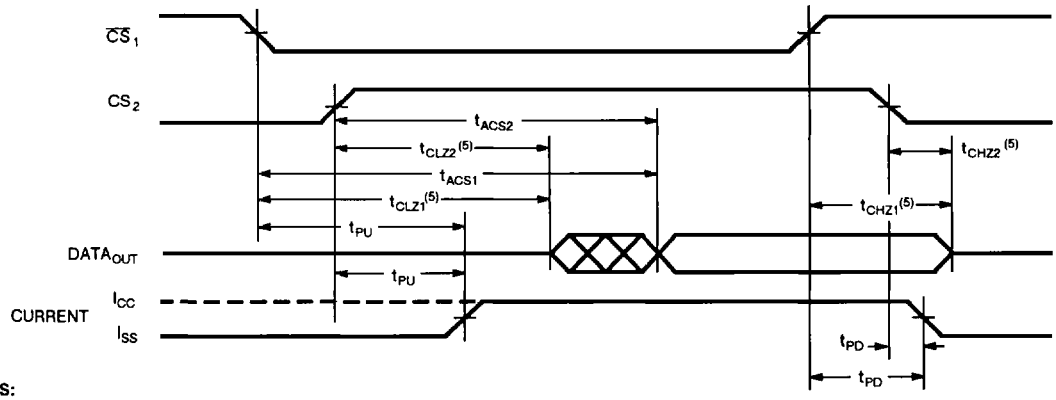
TIMING WAVEFORM OF READ CYCLE NO. 1 [1]



TIMING WAVEFORM OF READ CYCLE NO. 2 [1, 2, 4]



TIMING WAVEFORM OF READ CYCLE NO. 3 [1, 3, 4]



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}_1 = V_{IL}$, $CS_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{CS}_1$ transition low and CS_2 transition high.
4. $\overline{OE} = V_{IL}$
5. Transition is measured ±200mV from steady state.

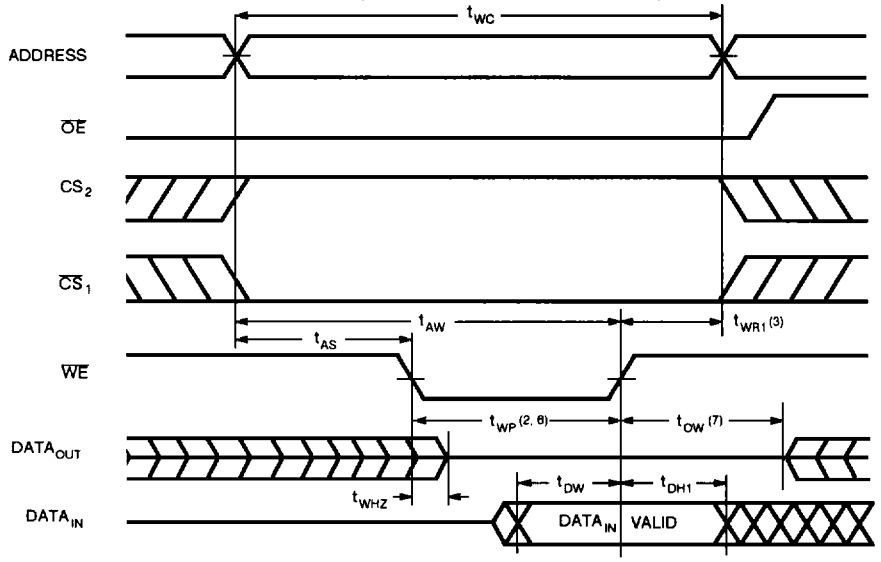
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	7164S19/20[1] 7164L20[1]		7164S25 7164L25		7164S30 7164L30		7164S35 7164L35		7164S45 7164L45		7164S55[2] 7164L55[2]		7164S70[2] 7164L70[2]		7164S85[2] 7164L85[2]		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
t_{WC}	Write Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	70	–	85	–	ns
$t_{CW1,2}$	Chip Select to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	60	–	75	–	ns
t_{AW}	Address Valid to End of Write	15	–	18	–	22	–	25	–	33	–	50	–	60	–	75	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WP}	Write Pulse Width	15	–	21	–	23	–	25	–	25	–	50	–	60	–	75	–	ns
t_{WR1}	Write Recovery Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WR2}	Write Recovery Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{WHZ}	Write Enable to Output High Z[3]	–	8	–	10	–	12	–	14	–	18	–	25	–	30	–	35	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	13	–	15	–	20	–	25	–	30	–	35	–	ns
t_{DH1}	Data Hold from Write Time ($\overline{CS}_1$, $\overline{WE}$)	0	–	0	–	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{DH2}	Data Hold from Write Time (CS_2)	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OW}	Output Active from End of Write[3]	5	–	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns

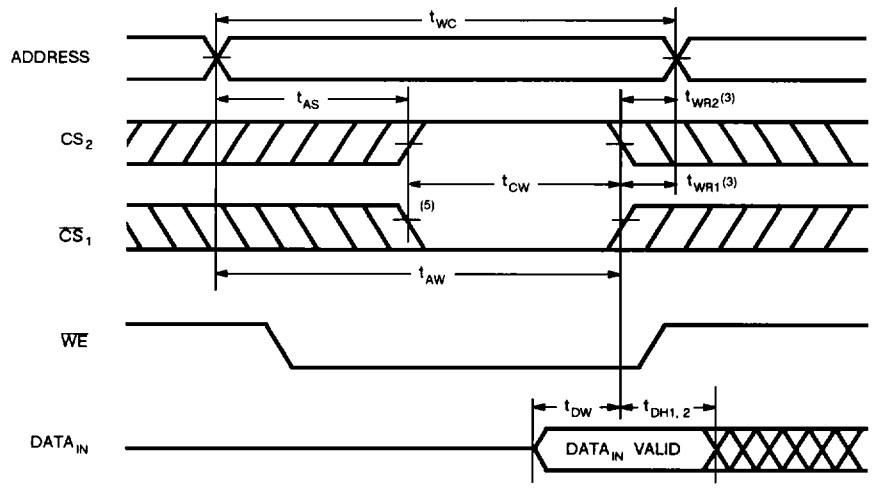
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only. Also available: 100, 120, 150 and 200ns military devices.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)[1]



NOTES:

1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}_1$ and a high CS_2.
3. $t_{WR1,2}$ is measured from the earlier of $\overline{CS}_1$ or $\overline{WE}$ going high or CS_2 going low to the end of write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}_1$ low transition or CS_2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WR}
7. $DATA_{OUT}$ is the same phase of write data of this write cycle.
8. If $\overline{CS}_1$ is low and CS_2 is high during this period, I/O pins are in the output state. Data input signals must not be applied.
9. Transition is measured ±200mV from steady state.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization but is not production tested.

TRUTH TABLE

$\overline{WE}$	$\overline{CS}_1$	CS_2	$\overline{OE}$	I/O	MODE
X	H	X	X	HIGH Z	Standby (I_{SB})
X	X	L	X	HIGH Z	Standby (I_{SB})
X	V_{HC}	V_{HC} or V_{LC}	X	HIGH Z	Standby (I_{SB1})
X	X	V_{LC}	X	HIGH Z	Standby (I_{SB1})
H	L	H	H	HIGH Z	Output disable
H	L	H	L	D_{OUT}	Read
L	L	H	X	D_{IN}	Write

NOTE:
1. CS_2 will power-down $\overline{CS}_1$, but $\overline{CS}_1$ will not power-down CS_2.

ORDERING INFORMATION