TENTATIVE TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

2,097,152-WORD BY 16-BIT CMOS PSEUDO STATIC RAM

DESCRIPTION

The TC51W3217XB is a 33,554,432-bit pseudo static random access memory(PSRAM) organized as 2,097,152 words by 16 bits. Using Toshiba's CMOS technology and advanced circuit techniques, it provides high density, high speed and low power. The device operates single power supply. The device also features SRAM-like write timing whereby data is written to memory cells on the rising edge of the $\overline{\text{WE}}$ signal. The device has the page access operation. Page size is 4 words. The device also supports deep power-down mode, realizing low-power standby.

FEATURES

- Organized as 2,097,152 words by 16 bits
- Single power supply voltage of 2.5 to 3.1 V
- Direct TTL compatibility for all inputs and outputs
- Deep power-down mode: Memory cell data invalid
- Page operation mode :
  Page read operation by 4 words
- Logic compatible with SRAM R/W($\overline{\text{WE}}$) pin
- Standby current

Standby	70 μA
Deep power-down standby	5 μA

- Access Times:

	TC51W3217
$\overline{\text{CE}}$ Access Time	80 ns
$\overline{\text{OE}}$ Access Time	80 ns
Page Access Time	25 ns

- Packages:
  P-TFBGA48-0609-0.80AZ (Weight: g typ.)

PIN ASSIGNMENT (TOP VIEW)

	1	2	3	4	5	6
A	A4	A17	$\overline{\text{UB}}$	CS	A8	A12
B	A3	A7	$\overline{\text{LB}}$	$\overline{\text{WE}}$	A9	A13
C	A2	A6	A18	A20	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	I/O1	I/O3	I/O6	I/O8	A16
F	$\overline{\text{CE}}$	I/O9	I/O11	I/O13	I/O15	NC
G	$\overline{\text{OE}}$	I/O10	I/O12	V_{DD}	I/O14	I/O16
H	GND	I/O2	I/O4	I/O5	I/O7	GND

(FBGA48)

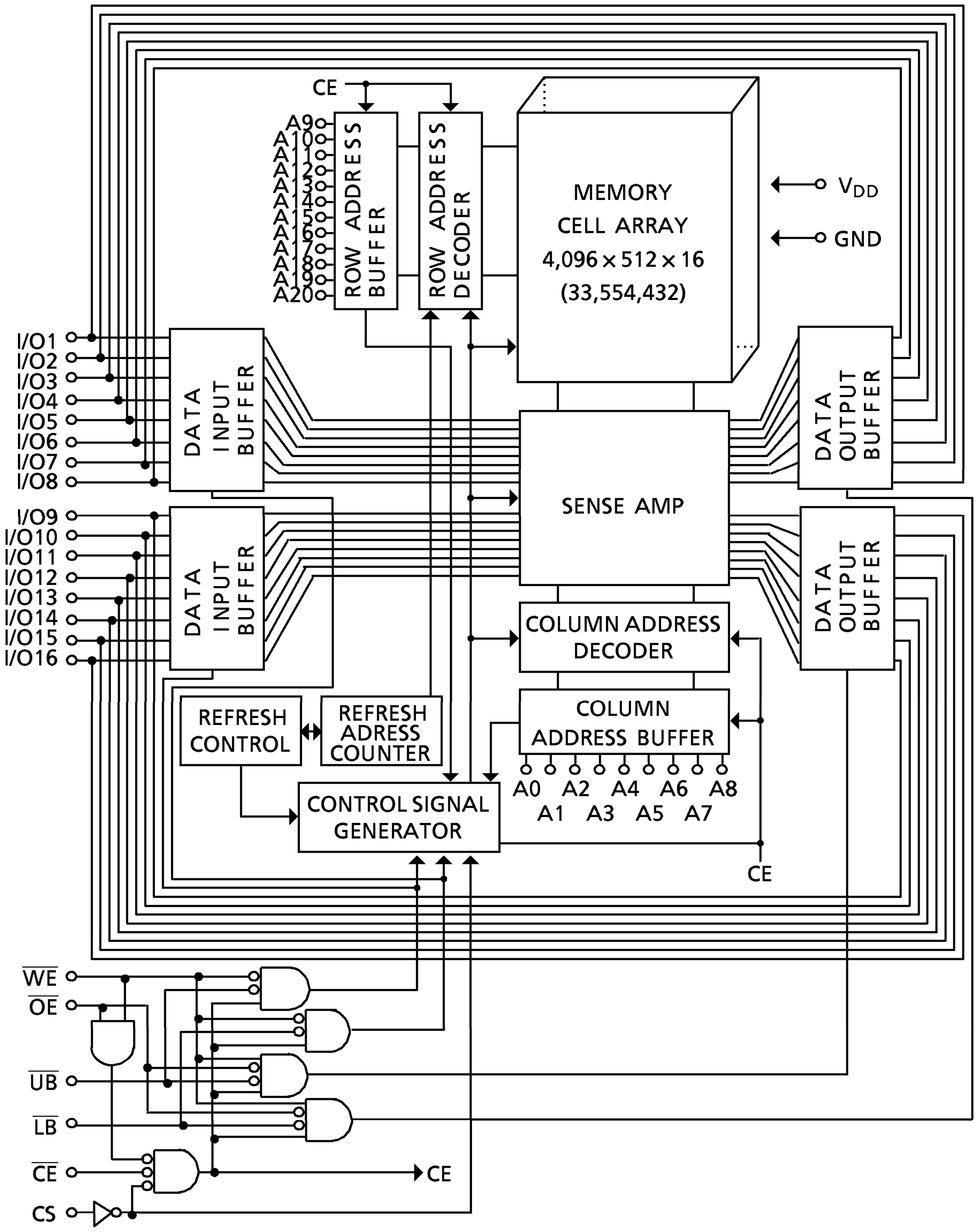
PIN NAMES

A0 to A20	Address Inputs
A0 to A1	Page Address Inputs
I/O1 to I/O16	Data Inputs / Outputs
$\overline{\text{CE}}$	Chip Enable Input
CS	Chip Select Input
$\overline{\text{WE}}$	Write Enable Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{LB}}$, $\overline{\text{UB}}$	Data Byte Control Inputs
V_{DD}	Power
GND	Ground
NC	No Connection

000707EBA2

- TOSHIBA is continually working to improve the quality and reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to comply with the standards of safety in making a safe design for the entire system, and to avoid situations in which a malfunction or failure of such TOSHIBA products could cause loss of human life, bodily injury or damage to property.
  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
- The TOSHIBA products listed in this document are intended for usage in general electronics applications (computer, personal equipment, office equipment, measuring equipment, industrial robotics, domestic appliances, etc.). These TOSHIBA products are neither intended nor warranted for usage in equipment that requires extraordinarily high quality and/or reliability or a malfunction or failure of which may cause loss of human life or bodily injury ("Unintended Usage"). Unintended Usage include atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, medical instruments, all types of safety devices, etc.. Unintended Usage of TOSHIBA products listed in this document shall be made at the customer's own risk.
- The products described in this document are subject to the foreign exchange and foreign trade laws.
- The information contained herein is presented only as a guide for the applications of our products. No responsibility is assumed by TOSHIBA CORPORATION for any infringements of intellectual property or other rights of the third parties which may result from its use. No license is granted by implication or otherwise under any intellectual property or other rights of TOSHIBA CORPORATION or others.
- The information contained herein is subject to change without notice.

BLOCK DIAGRAM



OPERATION MODE

MODE	$\overline{CE}$	CS	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	Add	I/O1 to I/O8	I/O9 to I/O16	POWER
Read(Word)	L	H	L	H	L	L	× ×	D_{OUT}	D_{OUT}	I_{DDO}
Read(Lower Byte)	L	H	L	H	L	H	× ×	D_{OUT}	High-Z	I_{DDO}
Read(Upper Byte)	L	H	L	H	H	L	× ×	High-Z	D_{OUT}	I_{DDO}
Write(Word)	L	H	×	L	L	L	× ×	D_{IN}	D_{IN}	I_{DDO}
Write(Lower Byte)	L	H	×	L	L	H	× ×	D_{IN}	Invalid	I_{DDO}
Write(Upper Byte)	L	H	×	L	H	L	× ×	Invalid	D_{IN}	I_{DDO}
Outputs Disabled	L	H	H	H	×	×	× ×	High-Z	High-Z	I_{DDS}
Standby	H	H	×	×	×	×	×	High-Z	High-Z	I_{DDS}
Deep Power-down Standby	H	L	×	×	×	×	×	High-Z	High-Z	I_{DDSD}

L = Low-level Input(V_{IL}), H = High-level Input(V_{IH}), × = V_{IH} or V_{IL}, High-Z = High-impedance

× × = At $\overline{CE}$ falling edge, all addresses(A2 to A20) are valid "IN". Page address signals(A0 and A1) must be V_{IH} or V_{IL}, during entire cycle.

ABSOLUTE MAXIMUM RATINGS (See Note 1)

SYMBOL	RATING	VALUE	UNIT
V_{DD}	Power Supply Voltage	– 1.0 to 3.6	V
V_{IN}	Input Voltage	– 1.0 to 3.6	V
V_{OUT}	Output Voltage	– 1.0 to 3.6	V
Topr.	Operating Temperature	– 20 to 85	°C
Tstrg.	Storage Temperature	– 55 to 150	°C
Tsolder	Soldering Temperature (10 s)	260	°C
P_D	Power Dissipation	0.6	W
I_{OUT}	Short Circuit Output Current	50	mA

DC RECOMMENDED OPERATING CONDITIONS (Ta = – 20°C to 85°C)

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
V_{DD}	Power Supply Voltage	2.5	2.75	3.1	V
V_{IH}	Input High Voltage	2.0	–	V_{DD} + 0.3*	V
V_{IL}	Input Low Voltage	– 0.3*	–	0.4	V
V_{DH}	Data Retention Supply Voltage	2.5	–	3.1	V

* : V_{IH}(Max) V_{DD} + 1.0 V with 10 ns pulse width
V_{IL}(Min) –1.0 V with 10 ns pulse width

DC CHARACTERISTICS (Ta = – 20°C to 85°C, V_{DD} = 2.5 to 3.1 V) (See Note 3 to 4)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP.	MAX	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0 V to V_{DD}		–1.0	–	+ 1.0	µA
I_{LO}	Output Leakage Current	Output disable, V_{OUT} = 0 V to V_{DD}		–1.0	–	+ 1.0	µA
V_{OH}	Output High Voltage	I_{OH} = – 0.5 mA		2.0	–	–	V
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA		–	–	0.4	V
I_{DDO1}	Operating Current	$\overline{\text{CE}}$ cycling CS = V_{IH}, I_{OUT} = 0 mA	t_{RC} = min	–	–	40	mA
			t_{RC} = 1 µs	–	–	5	mA
I_{DDO2}	Page Access Operating Current	$\overline{\text{CE}}$ = V_{IL}, CS = V_{IH} Page add. cycling I_{OUT} = 0 mA	t_{PC} = min	–	–	25	mA
I_{DDS1}	Standby Current (TTL)	$\overline{\text{CE}}$ = V_{IH}, CS = V_{IH}		–	–	3	mA
I_{DDS2}	Standby Current (MOS)	$\overline{\text{CE}}$ = V_{DD} – 0.2 V, CS = V_{DD} – 0.2 V		–	–	70	µA
I_{DDSD}	Deep Power-down Standby Current	CS = 0.2 V		–	–	5	µA

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	V_{IN} = GND	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = GND	10	

Note: This parameter is sampled periodically and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS (Ta = – 20°C to 85°C, V_{DD} = 2.5 to 3.1 V) (See Note 5 to 12)

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{RC}	Read or Write Cycle Time	100	–	ns
t_{CE}	$\overline{CE}$ Pulse Width	80	10000	ns
t_{P}	Pre-charge Time	20	–	ns
t_{CEA}	$\overline{CE}$ Access Time	–	80	ns
t_{OEA}	$\overline{OE}$ Access Time	–	80	ns
t_{OEP}	$\overline{OE}$ Pulse Width	80	10000	ns
t_{BEA}	$\overline{LB}$, $\overline{UB}$ Access Time	–	25	ns
t_{APH}	Address(A0 and A1) Hold Time	80	–	ns
t_{ASC}	Address Set-up Time	– 25	–	ns
t_{AHC}	Address Hold Time	50	–	ns
t_{ASO}, t_{ASW}	Address Set-up Time	0	–	ns
t_{AHO}, t_{AHW}	Address Hold Time	50	–	ns
t_{WHC}	$\overline{WE}$ Hold Time	10	–	ns
t_{RCS}	Read Command Set-up Time	10	–	ns
t_{WOS}	Write Command Set-up Time	20	–	ns
t_{RCH}	Read Command Hold Time	10	–	ns
t_{WP}	$\overline{WE}$ Pulse Width	80	10000	ns
t_{WCH}	$\overline{CE}$ to End of Write	60	–	ns
t_{CWL}	Write Command to $\overline{CE}$ Lead Time	80	–	ns
t_{WBH}	$\overline{LB}$, $\overline{UB}$ to End of Write	50	–	ns
t_{BWL}	Write Command to $\overline{LB}$, $\overline{UB}$ Lead Time	50	–	ns
t_{WR}	Write Recovery Time	0	–	ns
t_{DSW}	Data Set-up Time from $\overline{WE}$	30	–	ns
t_{DSC}	Data Set-up Time from $\overline{CE}$	30	–	ns
t_{DSB}	Data Set-up Time from $\overline{LB}$, $\overline{UB}$	30	–	ns
t_{DHW}	Data Hold Time from $\overline{WE}$	0	–	ns
t_{DHC}	Data Hold Time from $\overline{CE}$	0	–	ns
t_{DHB}	Data Hold Time from $\overline{LB}$, $\overline{UB}$	0	–	ns
t_{CLZ}	$\overline{CE}$ Low to Output Active	10	–	ns
t_{OLZ}	$\overline{OE}$ Low to Output Active	0	–	ns
t_{BLZ}	$\overline{LB}$, $\overline{UB}$ Low to Output Active	0	–	ns
t_{WLZ}	$\overline{WE}$ Low to Output Active	0	–	ns
t_{CHZ}	$\overline{CE}$ High to Output High-Z	–	20	ns
t_{OHZ}	$\overline{OE}$ High to Output High-Z	–	20	ns
t_{BHZ}	$\overline{LB}$, $\overline{UB}$ High to Output High-Z	–	20	ns
t_{WHZ}	$\overline{OE}$ High to Output High-Z	–	20	ns
t_{PC}	Page Mode Cycle Time	25	–	ns
t_{AA}	Page Mode Address Acess Time	–	25	ns
t_{AOH}	Page Mode Output Data Hold Time	5 *	–	ns
t_{CS}	CS Set-up Time	0	–	ns
t_{CH}	CS Hold Time	200	–	μs
t_{DPD}	CS Pulse Width(Deep Power Down)	10	–	ms

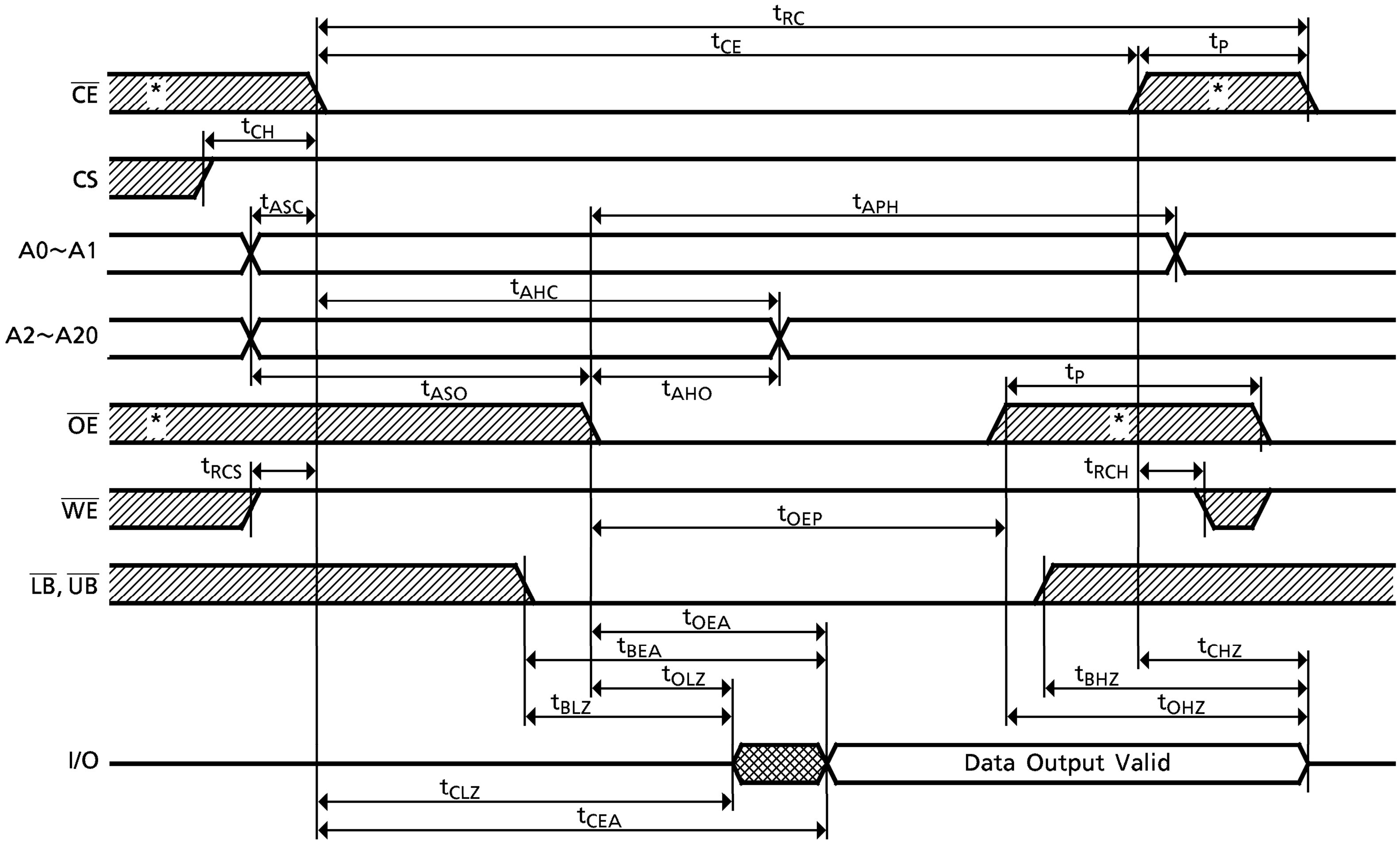
* : Guarantee minimum 10ns of data valid time under any specific operating condition

AC TEST CONDITIONS

Output load: 30 pF + 1TTL Gate
Input pulse level: $V_{DD} - 0.2V$, 0.2V
Timing measurements: $V_{DD} \times 0.5$
Reference level: $V_{DD} \times 0.5$
t_R, t_F: 5 ns

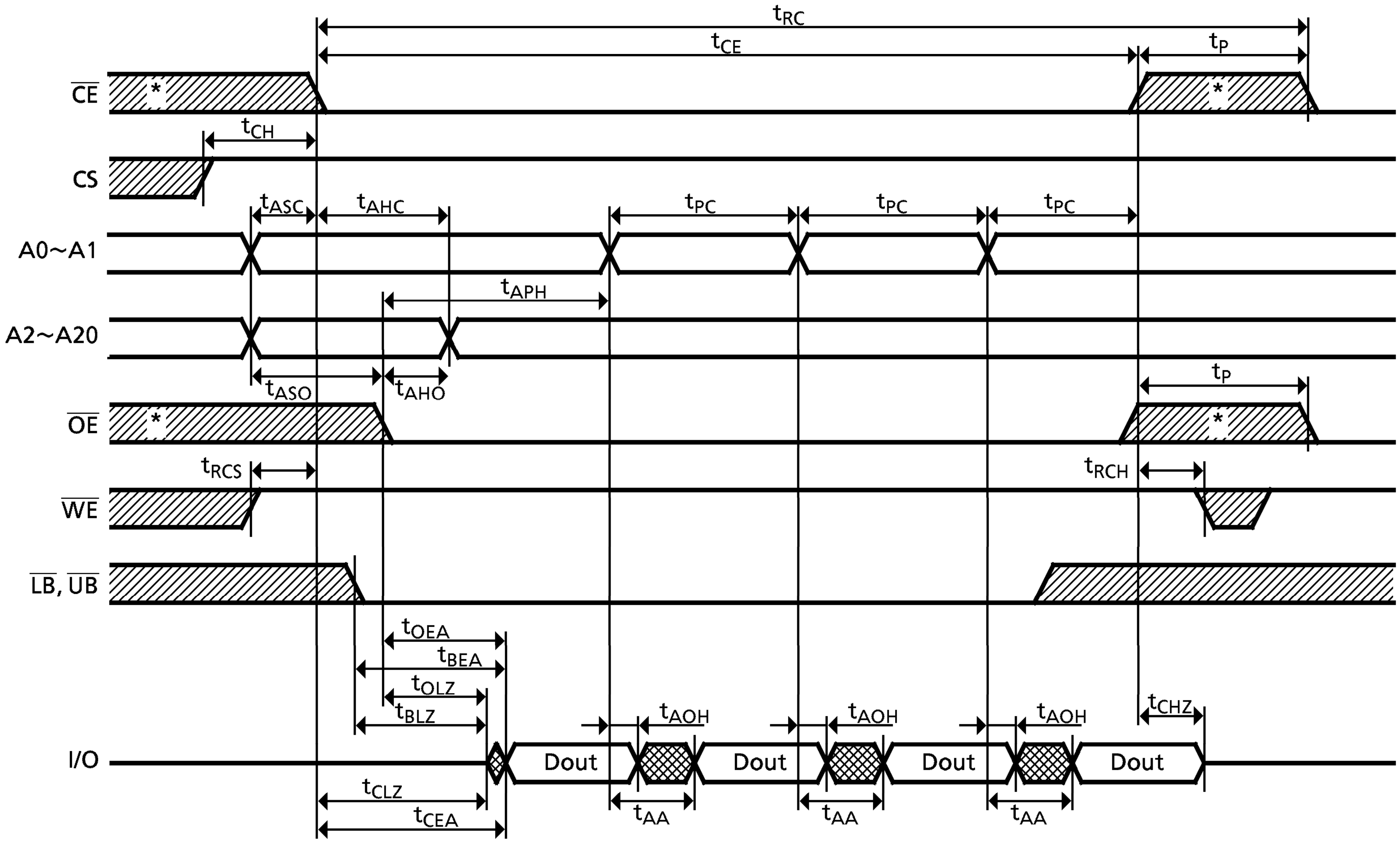
TIMING DIAGRAMS

Read Timing



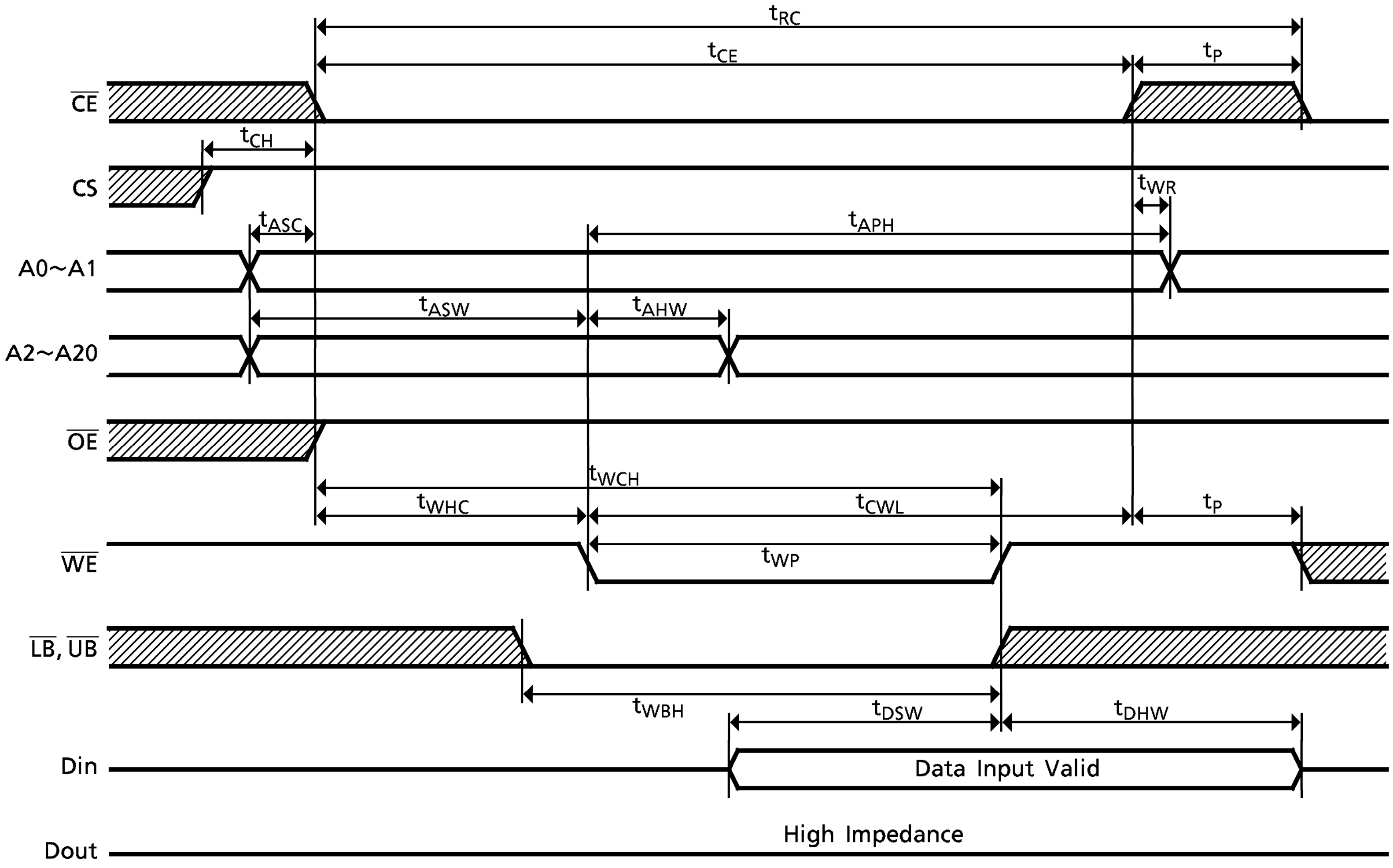
* ▨ In this section, either $\overline{\mathrm{OE}}$ or $\overline{\mathrm{CE}}$ is set to High.

Page Read Timing(4 words access)

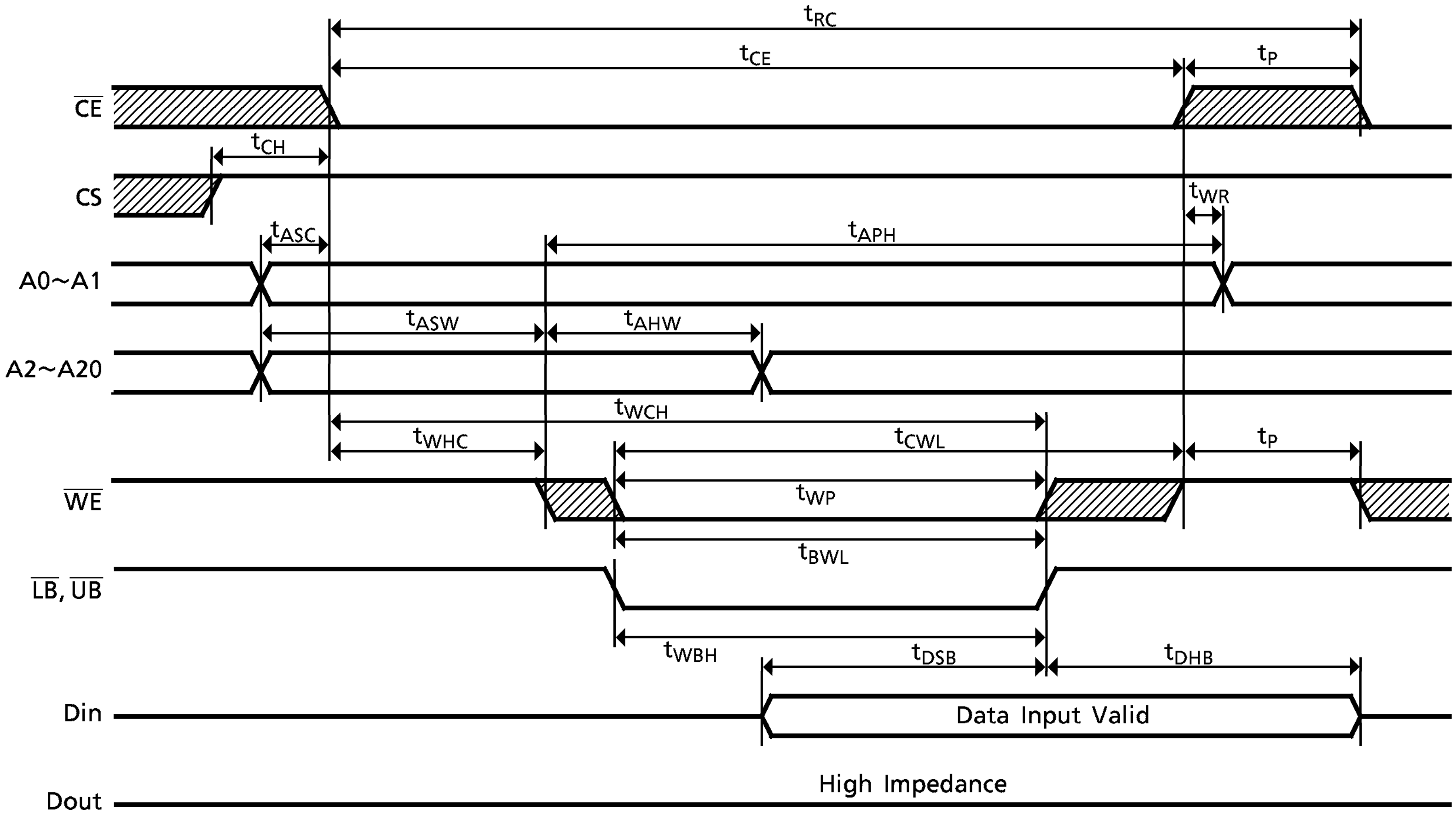


* ▨ In this section, either $\overline{\mathrm{OE}}$ or $\overline{\mathrm{CE}}$ is set to High.

Write Timing($\overline{WE}$ Control Write)

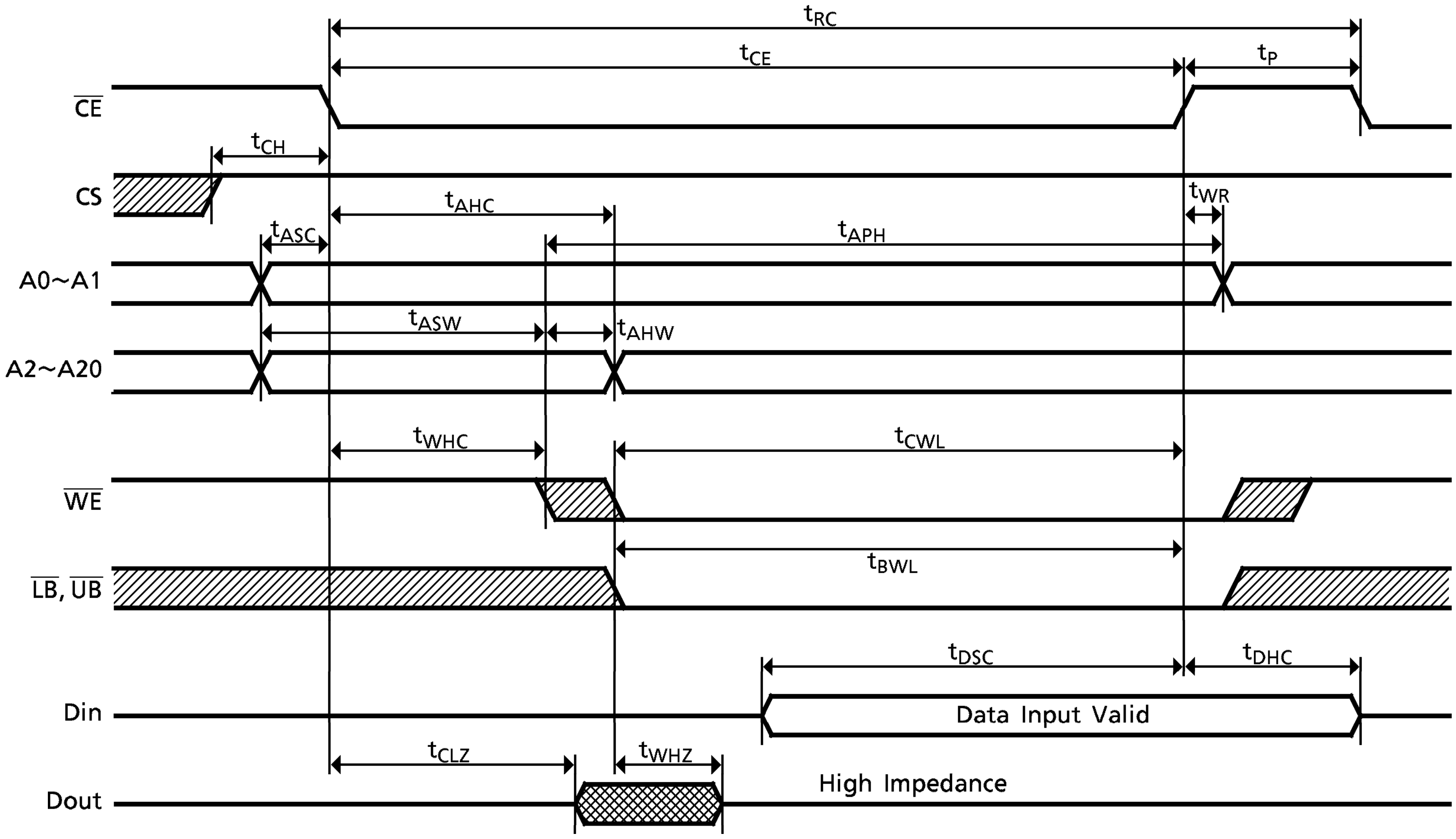


Write Timing($\overline{LB}$ / $\overline{UB}$ Control Write)

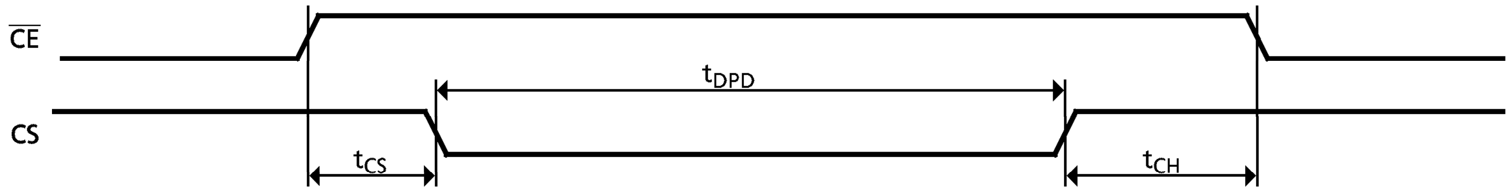


* $\overline{OE}$ ··· "H"

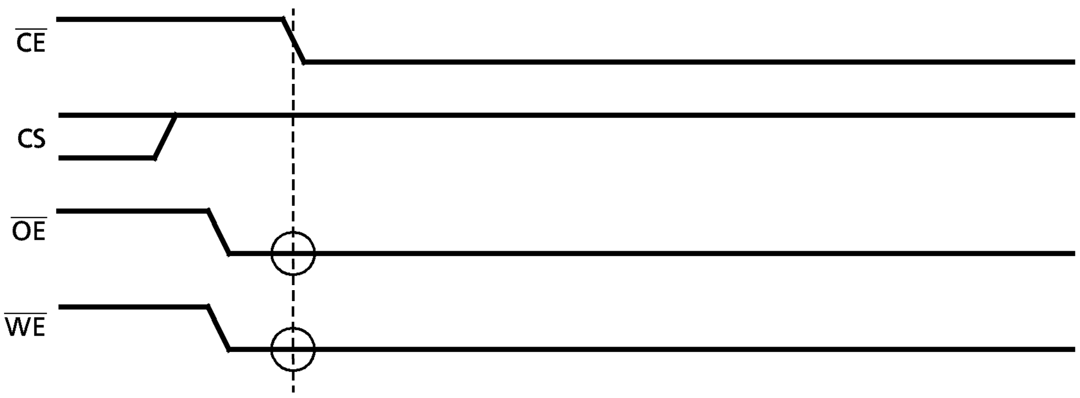
Write Timing($\overline{CE}$ Control Write)



Deep Power-down Timing



Prohibition Timing



The timing shown above is prohibited.
If both $\overline{\text{OE}}$ and $\overline{\text{WE}}$ go Low coincident with or before falling edge of $\overline{\text{CE}}$, a malfunction may occur since devices go into test modes for internal use.

Notes: (1) Stresses greater than listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

(2) All voltages are reference to GND.

(3) I_{DDO} depends on the cycle time.

(4) I_{DDO} depends on output loading. Specified values are defined with the output open condition.

(5) After power-up, an initial pause of 200μs with CS high is required with the output open condition.

(6) AC measurements are assumed $t_T = 5$ns.

(7) Parameters t_{CHZ}, t_{OHZ}, t_{BHZ} and t_{WHZ} define the time at which the output goes the open condition and are not output voltage reference levels.

(8) During write cycles, input data is latched on the earliest of $\overline{\text{WE}}$, $\overline{\text{LB}}/\overline{\text{UB}}$ or $\overline{\text{CE}}$ rising edge. Therefore, input data must be valid during the set-up time(t_{DSC}, t_{DSB} or t_{DSW}) and hold time(t_{DHC}, t_{DHB} or t_{DHW}).

(9) Address(A2 to A20) inputs are latched on the falling edge of $\overline{\text{OE}}$ or $\overline{\text{WE}}$. Therefore, addresses(A2 to A20) input must be valid during the set-up time(t_{ASO} or t_{ASW}) and hold time(t_{AHO} or t_{AHW}).

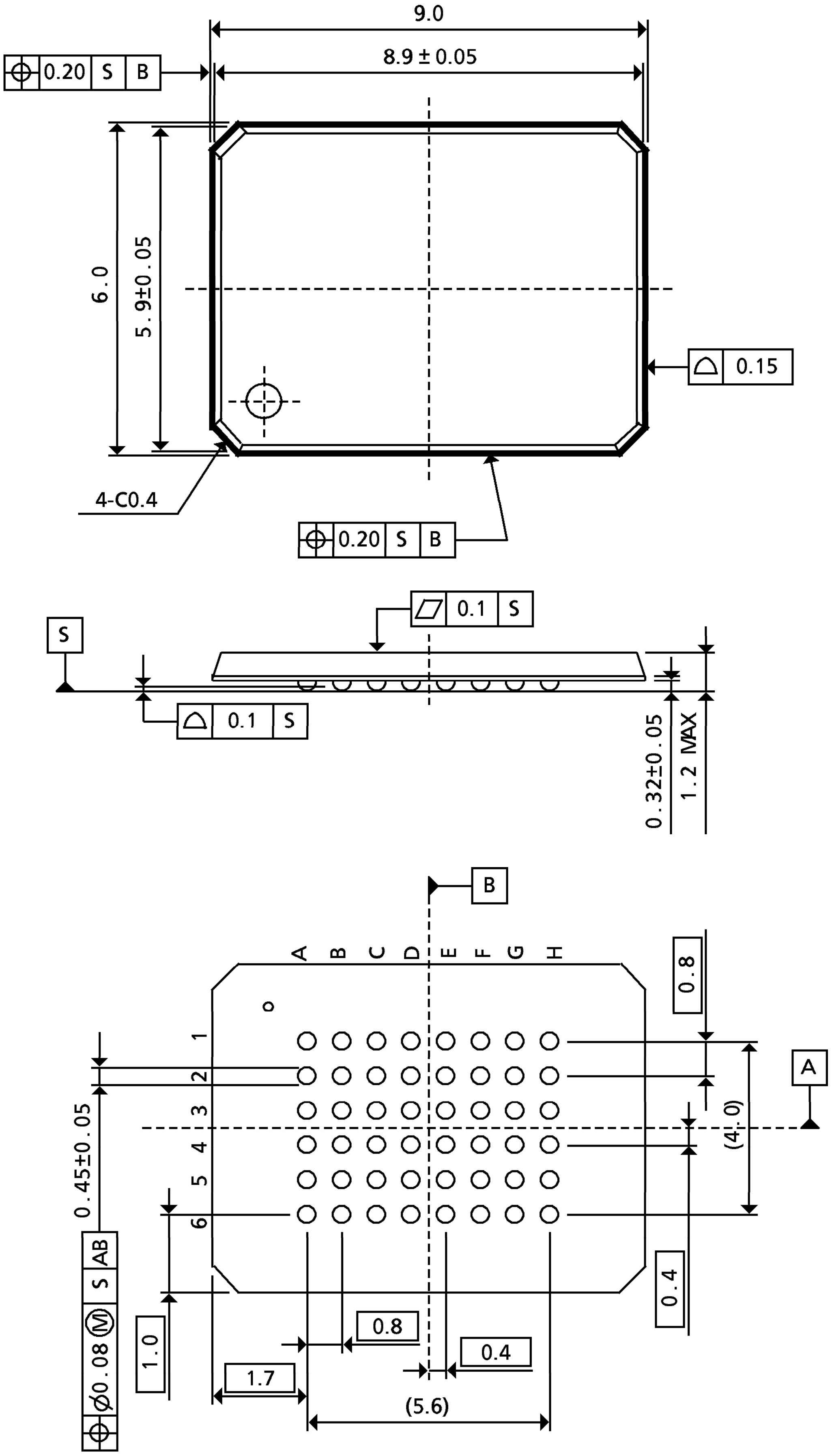
(10) Data cannot be retained at deep power-down stand-by mode.

(11) If $\overline{\text{OE}}$ is high during the write cycle, the outputs will remain at high impedance.

(12) During the output state of I/O signals, input signals of reverse polarity must not be applied.

PACKAGE DIMENSIONS (P-TFBGA48-0609-0.80AZ)

Unit : mm



Weight: g (typ)