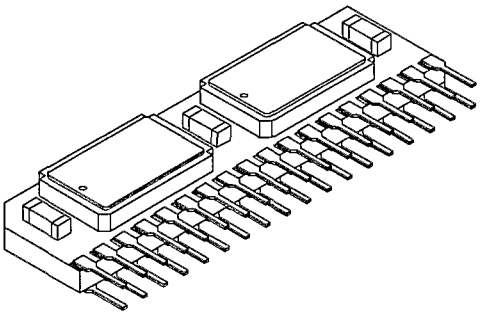
DPS16X17

16K X 16 CMOS SRAM MODULE



DESCRIPTION:

The DPS16X17 is part of a new family of high speed static RAM modules developed by Dense-Pac Microsystems, Inc. The DPS16X17 uses advanced packaging concepts which mount four LCC memory devices on a single multilayer ceramic substrate. The DPS16X17 is intended for use in applications where high speed memories are required and/or board space is of prime concern. It has been designed to the high quality and reliability requirements of the Military and Aerospace industry.

FEATURES:

- Organized as 16,384 by 16 Bits
- Fast Access Times:
  - DPS16X17-25 - 25ns (max)
  - DPS16X17-35 - 35ns (max)
  - DPS16X17-45 - 45ns (max)
  - DPS16X17-55 - 55ns (max)

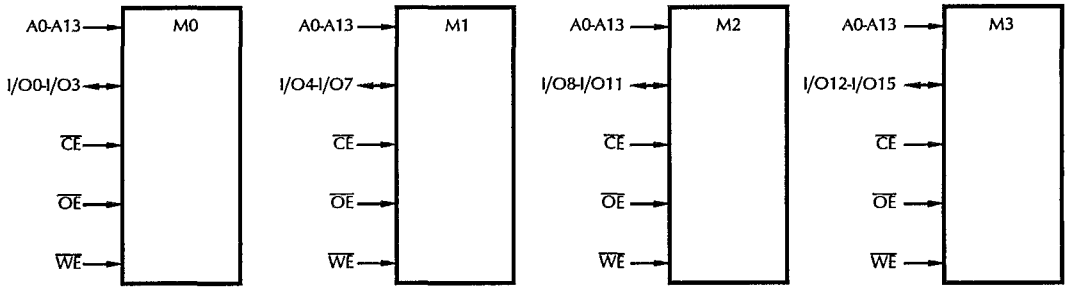
  (Faster Speeds Available Upon Request)
- *Completely Static Operation: No Clock or Refresh Needed*
- Single +5V Supply Voltage, ±10% Tolerance
- Common Data Inputs and Outputs
- $\overline{CE}$ Power-Down Function
- Data Retention Function
- Includes Decoupling Capacitors
- Output Enable Pin for Improved Control
- 36-Pin Dual-Leaded SIP Package

PIN-OUT DIAGRAMS

(TOP VIEW)

I/O0	1	36	V_{DD}
I/O1	2	35	I/O15
I/O2	3	34	I/O14
I/O3	4	33	I/O13
A0	5	32	I/O12
A1	6	31	V_{SS}
A2	7	30	A13
A3	8	29	A12
A4	9	28	A11
A5	10	27	A10
A6	11	26	A9
A7	12	25	A8
I/O4	13	24	I/O11
I/O5	14	23	I/O10
I/O6	15	22	I/O9
I/O7	16	21	I/O8
$\overline{CE}$	17	20	$\overline{WE}$
V_{SS}	18	19	$\overline{OE}$

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0-A13	Address Inputs
I/O0-I/O15	Data Input/Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5 Volts)
V_{SS}	Ground

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.5	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

ABSOLUTE MAXIMUM RATINGS[3]		
Parameter	Value	Unit
Storage Temperature	-65 to + 150	°C
Operating Temperature	-55 to + 125	°C
Supply Voltage[1]	-0.5 to + 7.0	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
$C_{I/O}$	Data Input/Output	20	pF	V_{OUT} = 0V
C_{ADR}	Address Input	45	pF	V_{IN} = 0V
C_{CE}	Chip Enable	45		
C_{WE}	Write Enable	45		
C_{OE}	Output Enable	45		

TRUTH TABLE				
MODE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O
Standby	H	X	X	HIGH-Z
Output Inhibit	L	H	H	HIGH-Z
Read	L	H	L	D_{OUT}
Write	L	L	H	D_{IN}

H = HIGH L = LOW X = Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges									
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current (All Inputs)	V_{DD} = 5.5V V_{IN} = 0V and 5.5V	-20	+20	-20	+20	-40	+40	µA
I_{OUT}	Output Leakage Current (on Data Outputs)	$\overline{CE}$ = V_{IH} V_{OUT} = 0V and 5.5V	-10	+10	-10	+10	-10	+10	µA
I_{CC1}	Operating Power Supply Current	$\overline{CE}$ = V_{IL}, f = max. Outputs Open		540		600		620	mA
I_{SB1}	Standby Power Supply Current (TTL)	$\overline{CE}$ = V_{IH}, f = 0		220		235		240	mA
I_{SB2}	Full Standby Power Supply Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V, V_{IN} ≤ V_{DD} - 0.2V or V_{IN} ≤ 0.2V		80		80		80	mA
V_{OL}	Output Low Voltage	V_{OL} = 8.0mA		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	V_{OH} = -4.0mA	2.4		2.4		2.4		V

NOTE: Dense-Pac has other specialized suppliers that may provide better D.C. Characteristics.

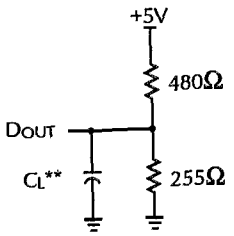
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

AC TEST CONDITIONS		
Load	C_L	Parameters Measured
1	30pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



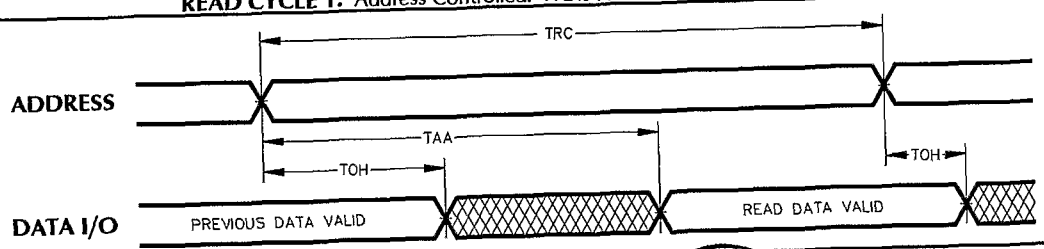
4

AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges										
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	25		35		45		55		ns
2	t_{AA}	Address Access Time		25		35		45		55	ns
3	t_{CO}	Chip Enable to Output Valid		25		35		45		55	ns
4	t_{OV}	Output Enable to Output Valid		15		25		30		35	ns
5	t_{OH}	Output Hold from Address Change	5		5		5		5		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	5		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [4, 5]		10		15		15		20	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		10		15		15		20	ns
10	t_{PU}	Chip Enable to Power Up Time	0		0		0		0		ns
11	t_{PD}	Chip Disable to Power Down Time		25		35		45		55	ns

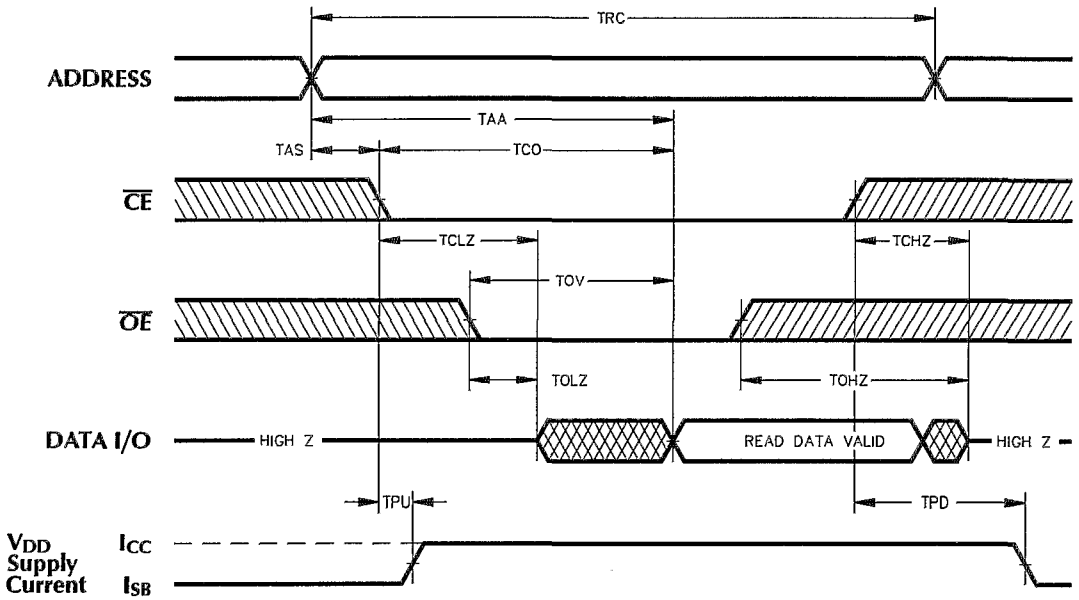
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [8, 9]: Over operating ranges										
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
12	t_{WC}	Write Cycle Time	20		30		40		50		ns
13	t_{AW}	Address Valid to End of Write	20		25		35		50		ns
14	t_{CW}	Chip Enable to End of Write	20		30		35		50		ns
15	t_{DW}	Data Valid to End of Write	13		15		20		25		ns
16	t_{DH}	Data Hold Time	0		5		5		5		ns
17	t_{WP}	Write Pulse Width	20		25		35		50		ns
18	t_{AS}	Address Set-up Time ***	0		0		0		0		ns
19	t_{AH}	Address Hold Time	0		0		0		0		ns
20	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		10		15		20		25	ns
21	t_{WLZ}	Write Enable to Output in LOW-Z [4, 5]	7		10		15		15		ns

*** Valid for both Read and Write Cycles.

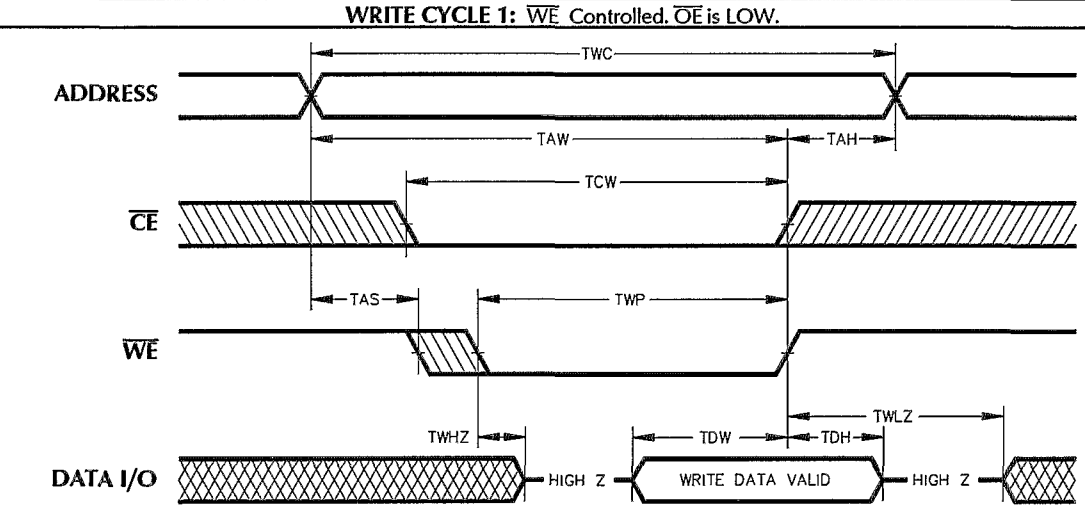
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



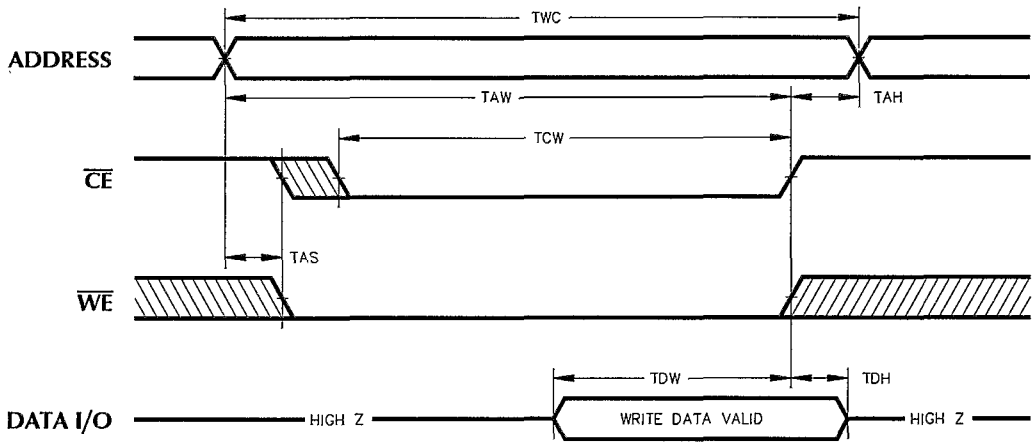
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



4

NOTES:

1. All voltages are with respect to V_{SS}.
2. V_{IL} min.= -3.0V min. for pulse width less than 20ns.
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage, with the load shown in Figure 1.

WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

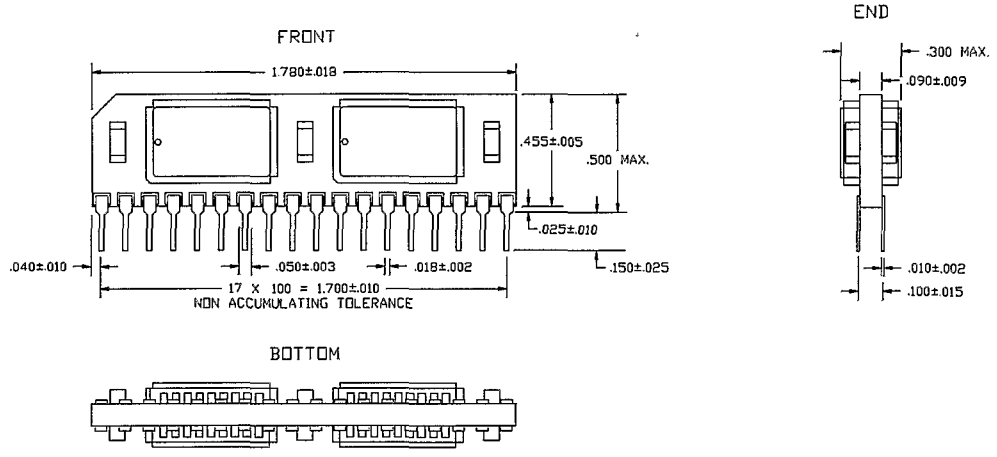
ORDERING INFORMATION

DP	S16X17	– XX	X
PREFIX	DEVICE TYPE	SPEED	GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	–40°C to +85°C
M	MILITARY	–55°C to +125°C
B *	MIL–PROCESSED	–55°C to +125°C
25	25ns	
35	35ns	
45	45ns	
55	55ns	
16K X 16 CMOS SRAM MODULE		

NOTE: B grade modules are constructed with 883 devices.

MECHANICAL DIAGRAMS



Dense-Pac Microsystems, Inc.
7321 Lincoln Way • Garden Grove, California 92641-1428
(714) 898-0007 • (800) 642-4477 (Outside CA) • FAX: (714) 897-1772