National Semiconductor

PRELIMINARY

microCMOS

MA2016 16,384 x 8-Bit CMOS Static RAM Module

General Description

The MA2016 consists of eight 2k x 8-bit CMOS RAMs along with an address decoder capable of decoding up to a 128k x 8-bit low power CMOS RAM. It operates on a single 5V power supply and is able to retain data down to 2V. The MA2016 does not require a refresh and all inputs and outputs are TTL compatible. Multiple MA2016 modules may be stacked in a piggyback fashion or laid out in any manner desired. The low power requirements and versatile layout make the MA2016 very useful for low power hand-held battery powered applications.

Features

- 16k x 8-bits fully decoded
- Outputs directly TTL compatible
- Low power—typical 400 mW
- 250 ns access time
- Static operation—no clocks or refreshing required
- Single 5V supply ± 10%
- 2V minimum for data retention
- TRI-STATE® outputs for bus operation
- Common data I/O pins
- Separate OE pin
- Internal power supply decoupling

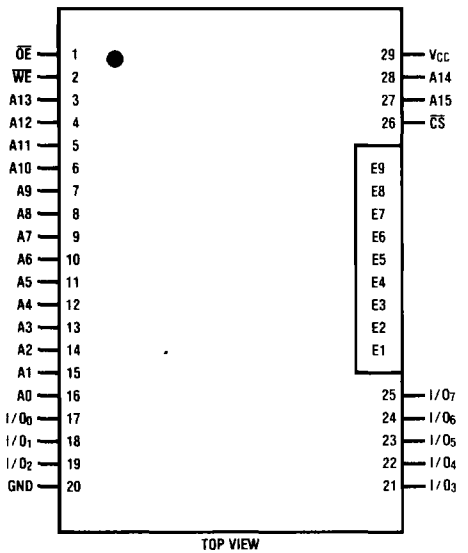
Applications

- Portable terminals
- Hand-held devices
- Pos terminals
- Remote instrumentation
- Process controllers
- *Microcomputer memory*

Ordering Information

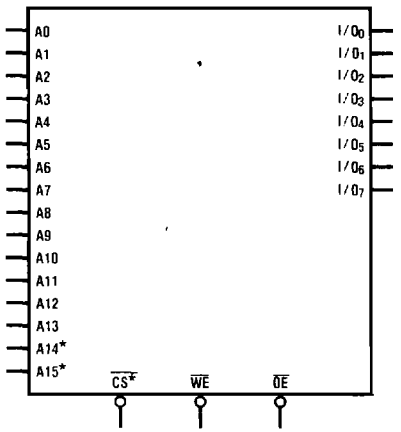
MA2016

Connection Diagram



TOP VIEW

Logic Symbol



* active state user selectable

Pin Names

$\overline{CS}$	Chip Select Input (user programmable)
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
I/O_0-I/O_7	Data Inputs/Outputs
A0-A15	Address Inputs (A14, A15 Block Select, user programmable)
V_{CC}	Power (typical 5V)
GND	Ground

Truth Table

$\overline{CS}$*	$\overline{WE}$	$\overline{OE}$	I/O	Mode
H	X	X	Hi-Z	Standby
L	H	L	D_{OUT}	Read
L	H	H	Hi-Z	Read
L	L	X	D_{IN}	Write

* $\overline{CS}$ state is user selectable. Table shown with jumper E7 to E8 and E4 to E5 installed.

Absolute Maximum Ratings

Voltage at Any Pin with Respect to GND	−0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

AC Test Conditions

Input Pulse Levels:	0.8V to 2.4V
Input Rise and Fall Times:	10 ns
Input and Output Timing Reference Levels:	1.5V
Output Load:	1 TTL gate and $C_L = 100$ pF (including scope and fixturing)

DC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, GND = 0V, $T_A = 0°C$ to 70°C unless otherwise indicated.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\|I_{LI}\|$	Input Leakage Current A0-A10, $\overline{OE}$, $\overline{WE}$	$V_{IN} = 0V$ to V_{CC}			20	μA
$\|I_{LI}\|$	Input Leakage Current A11-A15, $\overline{CS}$	$V_{IN} = 0V$ to V_{CC}			5	μA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ $V_{I/O} = 0V$ to V_{CC}			20	μA
I_{CCOP}	Operating Power Supply Current	$\overline{CS} = V_{IL}$, $I_{I/O} = 0$ mA		55 (Note 1)		mA
I_{CCSB}	Standby Power Supply Current	$\overline{CS} = V_{IH}$		32 (Note 1)		mA
I_{CCDR}	Standby Power Supply Current Data Retention	$V_{CC} = 2.0V$, $\overline{CS} = V_{CC}$ $V_{IN} = 0V$ or V_{CC}		35 (Note 1)		μA
V_{DR}	Data Retention Voltage	$\overline{CS} = V_{CC}$, $V_{IN} = 0V$ or V_{CC}	2			V
V_{OL}	Output Voltage Low	$I_{OL} = 2.1$ mA			0.4	V
V_{OH}	Output Voltage High	$I_{OH} = -1.0$ mA	2.4			V
V_{IL}	Input Voltage Low		−0.3		0.8	V
V_{IH}	Input Voltage High		$V_{CC} - 2.0$		$V_{CC} + 0.3$	V

Capacitance (Note 2) $T_A = 25°C$, f = 1.0 MHz

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{I/O}$	Input/Output Capacitance I/O_0-I/O_7	$V_{I/O} = 0V$		70		pF
C_{IN}	Input Capacitance A0-A10, $\overline{WE}$, $\overline{OE}$	$V_{IN} = 0V$		55		pF
C_{IN}	Input Capacitance A11-A15, $\overline{CS}$			20		pF

Note 1: $V_{CC} = 5V$, $T_A = 25°C$

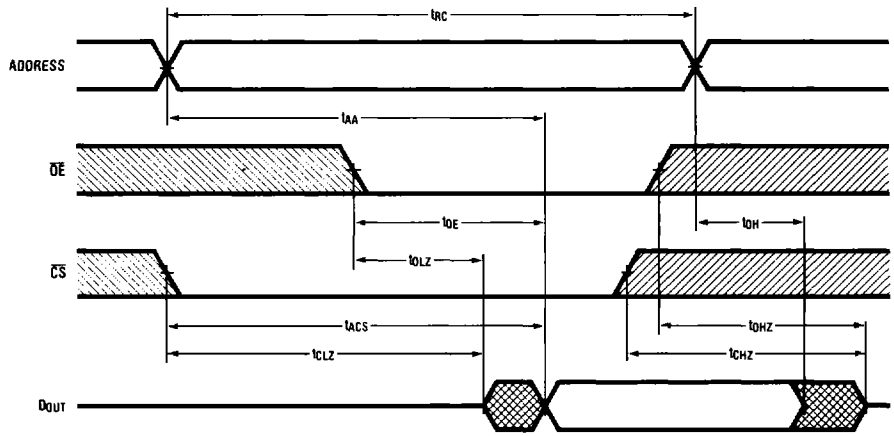
Note 2: This parameter is sampled and not 100% tested.

AC Characteristics-Read Cycle (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

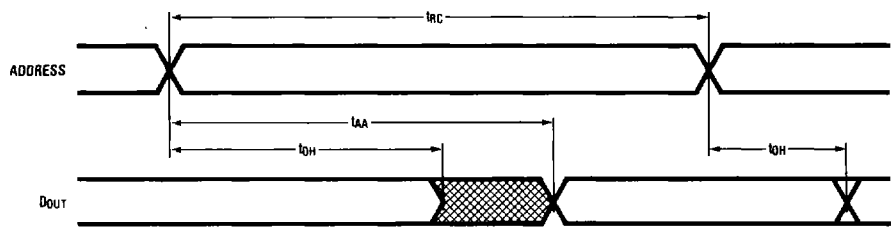
Symbol	Parameter	Min	Typ	Max	Units
t_{RC}	Read Cycle Time	200			ns
t_{AA}	Address Access Time			200	ns
t_{ACS}	Chip Select Access Time			200	ns
t_{CLZ}	Chip Selection to Output in Low Z	65			ns
t_{OE}	Output Enable to Output Valid			150	ns
t_{OLZ}	Output Enable to Output in Low Z	65			ns
t_{CHZ}	Chip Selection to Output in Hi-Z			100	ns
t_{OHZ}	Output Disable to Output in Hi-Z			100	ns
t_{OH}	Output Hold from Address Change	65			ns

Timing Waveforms

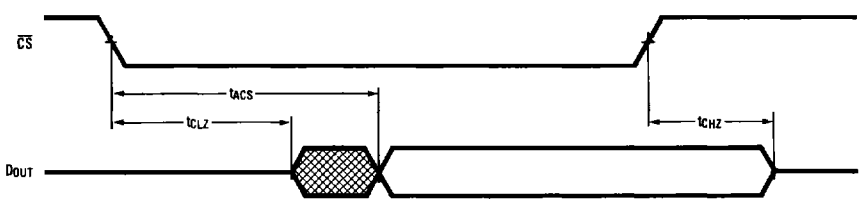
Read Cycle [1] (Notes 1 and 5)



Read Cycle [2] (Notes 1, 2, 4 and 5)



Read Cycle [3] (Notes 1, 3, 4 and 5)



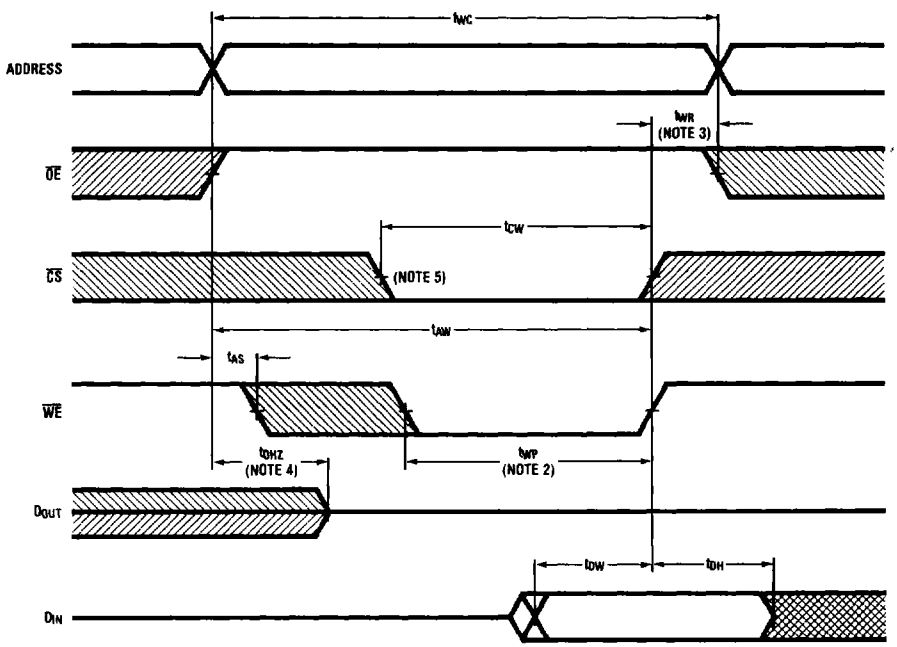
Note 1: $\overline{WE}$ is high for read cycle.
Note 2: Device is continuously selected, $\overline{CS} = V_{IL}$.
Note 3: Address valid prior to or coincident with $\overline{CS}$ transition low.
Note 4: $\overline{OE} = V_{IL}$.
Note 5: When $\overline{CS}$ is low, the address input must not be in the high impedance state.

AC Characteristics-Write Cycle (V_{CC} = 5V ± 10%, T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
t_{WC}	Write Cycle Time	200			ns
t_{CW}	Chip Selection to End of Write	140			ns
t_{AW}	Address Valid to End of Write	160			ns
t_{AS}	Address Set-Up Time	70			ns
t_{WP}	Write Pulse Width	140			ns
t_{WR}	Write Recovery Time	60			ns
t_{OHZ}	Output Disable to Output in Hi-Z			100	ns
t_{WHZ}	Write to Output in Hi-Z			110	ns
t_{DW}	Data to Write Time Overlap	100			ns
t_{DH}	Data Hold from Write Time	60			ns
t_{OW}	Output Active from End of Write	60			ns

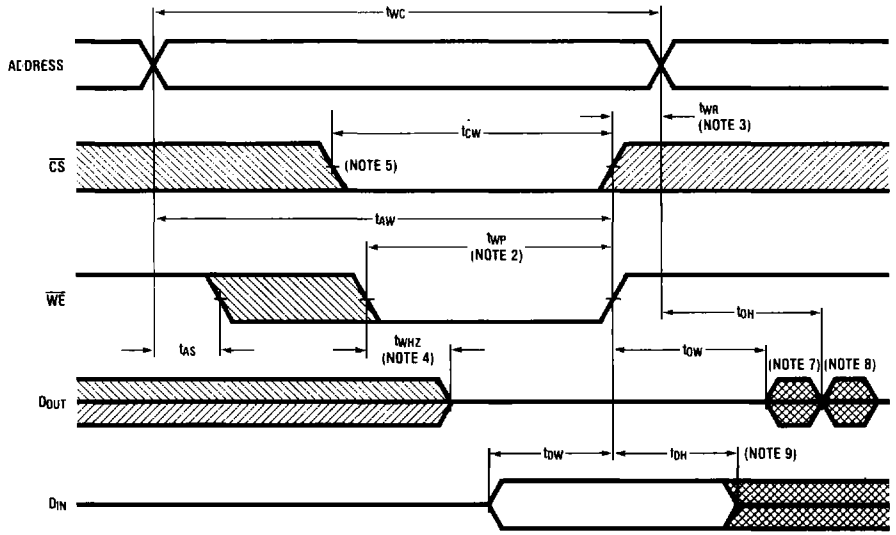
Timing Waveforms (Continued)

Write Cycle [1] (Note 1)



Timing Waveforms (Continued)

Write Cycle [2] (Notes 1 and 6)

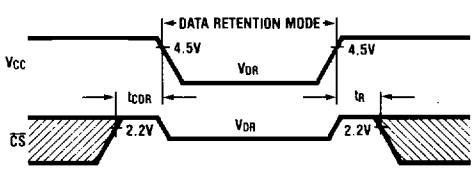


Note 1: $\overline{WE}$ must be high during all address transitions.
Note 2: A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
Note 3: t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
Note 4: During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
Note 5: If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
Note 6: $\overline{OE}$ is continuously low. ($\overline{OE} = V_{IL}$.)
Note 7: D_{OUT} is the the same phase of write data of this write cycle.
Note 8: D_{OUT} is the read data of next address.
Note 9: If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

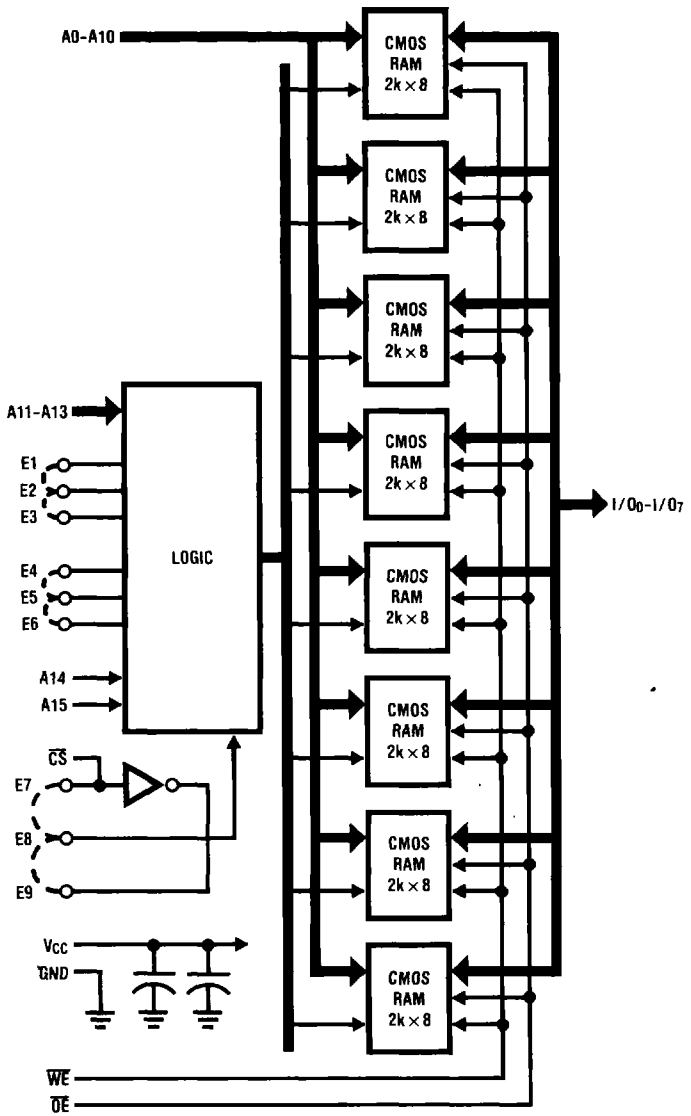
Low V_{CC} Data Retention Characteristics (T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
t_{CDR}	Chip Deselect to Data Retention Time	0			ns
t_R	Operation Recovery Time	200			ns

Low V_{CC} Data Retention Waveform



Block Diagram



Memory Expansion

BLOCK ADDRESS DEDICATION

The user must assign 16k block address boundaries by installing provided jumpers for each module. A summary of jumper connections for contiguous address boundaries from 0k-128k are shown in Table I.

The modules may be stacked up (8 max) or layed out horizontally in any order or combination to fit system profile constraints *(Figure 1)*.

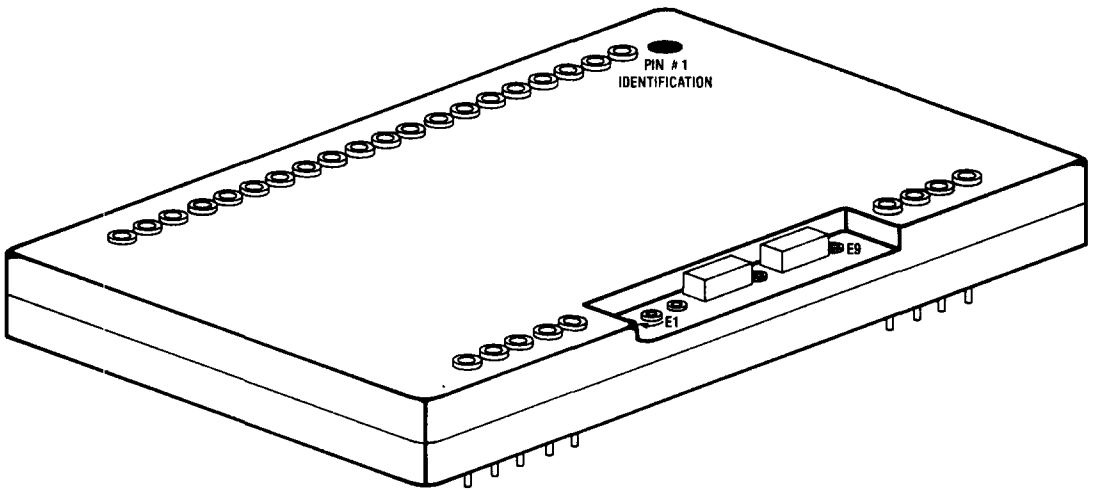
The low voltage data retention feature is usable to a max of four modules when stacked vertically.

Memory Expansion (Continued)

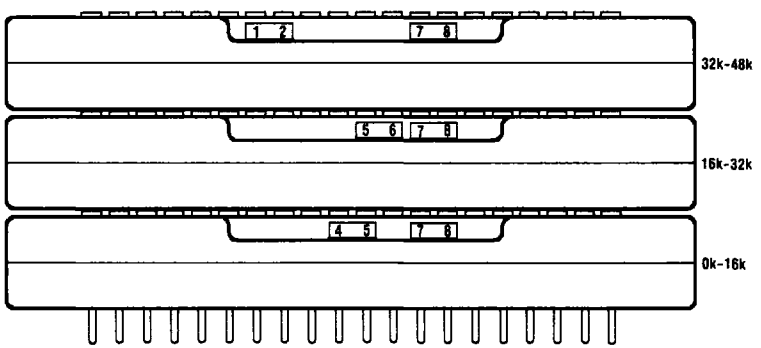
TABLE I

MA2016 #	$\overline{OE}$	$\overline{CS}$	Jumpers* E9 E8 E7 E6 E5 E4 E3 E2 E1	I/O	Address Boundary (Hex)	
1	L	L	● ● ● ● ● ●	0k-16k	0000_{16}	$3FFF_{16}$
2	L	L	● ● ● ● ● ●	16k-32k	4000_{16}	$7FFF_{16}$
3	L	L	● ● ● ● ● ●	32k-48k	8000_{16}	$BFFF_{16}$
4	L	L	● ● ● ● ● ●	48k-64k	$C000_{16}$	$FFFF_{16}$
5	L	H	● ● ● ● ● ●	64k-80k	10000_{16}	$13FFF_{16}$
6	L	H	● ● ● ● ● ●	80k-96k	14000_{16}	$17FFF_{16}$
7	L	H	● ● ● ● ● ●	96k-112k	18000_{16}	$1BFFF_{16}$
8	L	H	● ● ● ● ● ●	112k-128k	$1C000_{16}$	$1FFFF_{16}$
	H	X	X	TRI-STATE		

H = high = logic "1"
L = low = log c "0"
X = don't care
TRI-STATE = HI-Z
* Any configuration must have 2 jumpers per module.



a. 16k Configuration



b. 48k Configuration

FIGURE 1