MC-42256AB8
262,144 x 8-Bit
Dynamic CMOS RAM Module

Description

The MC-42256AB8 is a 262,144-word by 8-bit DRAM module designed to operate from a single +5-volt power supply. The module is a 30-pin socket-mountable Single Inline Memory Module (SIMM™) containing two μPD424256LA DRAMs (256K x 4).

The MC-42256AB8 is functionally equivalent to eight μPD42256 standard 256K x 1 DRAMs. Refreshing is accomplished by $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 - A_8 during a 4-ms period.

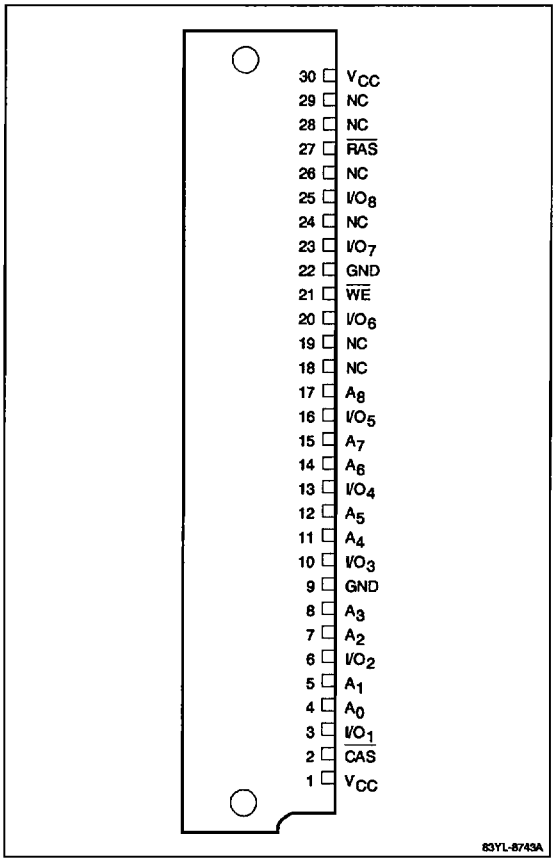
Features

- 262,144-word by 8-bit organization
- Single +5-volt power supply
- Standard 30-pin SIMM packaging
- Two 256K x 4 DRAMs
- Two power supply decoupling capacitors
- Low power dissipation of 16.5 mW max (standby)
- TTL-compatible inputs and outputs
- 256 refresh cycles every 4 ms
- Fast-page mode capability

SIMM is a trademark of Wang Laboratories.

Pin Configurations

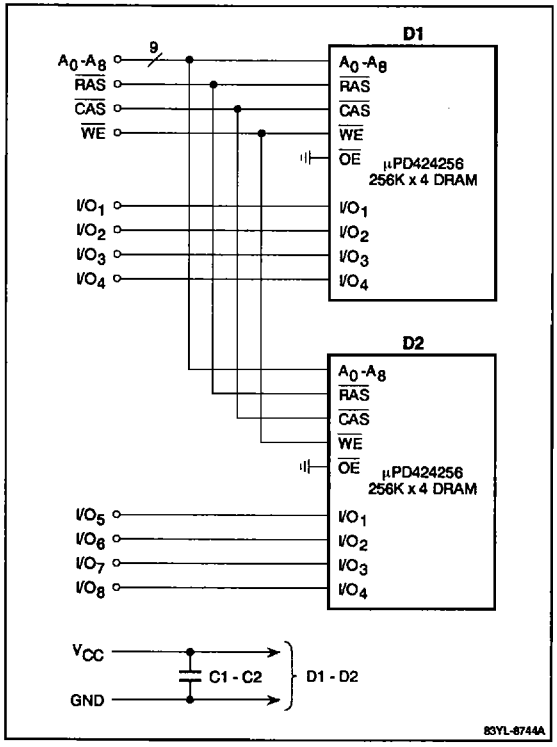
30-Pin Socket-Mountable SIMM



Ordering Information

Part Number	Access Time (max)	Package	Height	Thickness	DRAMs
MC-42256AB8BA-60	60 ns	30-pin socket-mountable SIMM (solder plating)	16.8 mm (0.661 inch)	5.08 mm (0.200 inch)	Two μPD424256LA
BA-70	70 ns				
BA-80	80 ns				
BA-10	100 ns				
MC-42256AB8FA-60	60 ns	30-pin socket-mountable SIMM (gold plating)			
FA-70	70 ns				
FA-80	80 ns				
FA-10	100 ns				

Connection Diagram



Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
I/O_1 - I/O_8	Common data inputs/outputs
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Absolute Maximum Ratings

Voltage on any pin relative to GND	−1.0 to +7.0 V
Operating temperature, T_{OPR}	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	2.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Ambient temperature	T_A	0		70	°C

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	70	pF	A_0 - A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Input/output capacitance	$C_{I/O}$	10	pF	I/O_1 - I/O_8

9a

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%; GND = 0V

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.5	5.0	5.5	V	
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V	
Input voltage, low	V_{IL}	−1.0		0.8	V	
Standby current	I_{CC2}			4	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH}
				2	mA	$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} − 0.2 V
Input leakage current	I_{IL}	−20		20	μA	For A_0 - A_8, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$: V_{IN} = 0 to 5.5 V; other pins = 0 V
Output leakage current	I_{OL}	−10		10	μA	For I/O_1 - I/O_8 and D_{OUT} disabled; V_{OUT} = 0 to 5.5 V
Output voltage, low	V_{OL}	0		0.4	V	I_{OUT} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V_{CC}	V	I_{OUT} = −5 mA

AC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

		−60		−70		−80		−10			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Test Conditions
Operating current, average	I_{CC1}		180		160		140		120	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} min (Note 5)
Operating current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		180		160		140		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = t_{RC} min (Note 5)
Operating current, fast-page cycle, average	I_{CC4}		160		140		120		100	mA	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ cycling; t_{PC} = t_{PC} min (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		180		160		140		120	mA	$\overline{RAS}$ cycling; $\overline{CAS}$ before $\overline{RAS}$; t_{RC} = t_{RC} min (Note 5)
Access time from column address	t_{AA}		30		35		45		50	ns	(Notes 7, 10, 11)
Access time from $\overline{CAS}$ precharge (rising edge)	t_{ACP}		35		40		45		55	ns	(Notes 7, 11)
Column address hold time referenced to $\overline{RAS}$	t_{AR}	N/A		N/A		60		70		ns	
Column address setup time	t_{ASC}	0		0		0	20	0	20	ns	(Note 11)
Row address setup time	t_{ASR}	0		0		0		0		ns	
Column address to $\overline{WE}$ delay time	t_{AWD}	30		35		45		50		ns	(Note 18)
Access time from $\overline{CAS}$ (falling edge)	t_{CAC}		20		20		20		25	ns	(Notes 7, 9, 10, 11)
Column address hold time	t_{CAH}	15		17		20		20		ns	
$\overline{CAS}$ pulse width	t_{CAS}	20	10,000	20	10,000	20	10,000	25	10,000	ns	
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	15		15		15		20		ns	

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
$\overline{CAS}$ precharge time, fast-page cycle	t_{CP}	10		10		10	20	10	25	ns	(Note 11)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		10		ns	(Note 14)
$\overline{CAS}$ hold time	t_{CSH}	60		70		80		100		ns	
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		10		ns	
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	20		20		20		25		ns	(Note 18)
Write command to $\overline{CAS}$ lead time	t_{CWL}	15		15		15		20		ns	
Data-in hold time	t_{DH}	15		15		20		20		ns	(Note 17)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	N/A		N/A		60		70		ns	
Data-in setup time	t_{DS}	0		0		0		0		ns	(Note 17)
Output buffer turnoff delay	t_{OFF}	0	15	0	15	0	20	0	25	ns	(Note 12)
Fast-page cycle time	t_{PC}	40		45		50		60		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		60		70		80		100	ns	(Notes 7, 8)
$\overline{RAS}$ to column address delay time	t_{RAD}	15	30	15	35	17	35	17	50	ns	(Note 10)
Row address hold time	t_{RAH}	10		10		12		12		ns	
Column address lead time referenced to $\overline{RAS}$ (rising edge)	t_{RAL}	30		35		45		50		ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10,000	70	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width, fast-page cycle	t_{RASP}	60	10,000	70	100,000	80	100,000	100	100,000	ns	
Random read or write cycle time	t_{RC}	120		130		160		190		ns	(Note 6)
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	50	25	60	25	75	ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		0		ns	(Note 15)
Read command setup time	t_{RCS}	0		0		0		0		ns	
Refresh period	t_{REF}		4		4		4		4	ms	Addresses A_0 - A_8
$\overline{RAS}$ precharge time	t_{RP}	50		60		70		80		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	10		10		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		10		ns	(Note 15)
$\overline{RAS}$ hold time	t_{RSH}	20		20		20		25		ns	
Read-write cycle time	t_{RWC}	145		155		190		225		ns	(Note 6)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	60		70		80		100		ns	(Note 18)

AC Characteristics (cont)

Parameter	Symbol	-60 Min	-60 Max	-70 Min	-70 Max	-80 Min	-80 Max	-10 Min	-10 Max	Unit	Test Conditions
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		20		25		30		ns	
Rise and fall transition time	t_T	3	50	3	50	3	50	3	50	ns	(Note 4)
Write command hold time	t_{WCH}	15		15		15		20		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	N/A		N/A		55		70		ns	
Write command setup time	t_{WCS}	0		0		0		0		ns	(Note 18)
Write command pulse width	t_{WP}	15		15		15		20		ns	(Note 16)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) Ac measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. I_{CC3} is measured assuming that all column address inputs are held at either a high level or a low level during $\overline{RAS}$-only refresh cycles. I_{CC4} is measured assuming that all column address inputs are switched only once during each fast-page cycle.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Load = 2 TTL (–1 mA, +4 mA) loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value in this table, t_{RAC} increases by the amount that t_{RCD} or t_{RAD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).

(10) If $t_{RAD} \geq t_{RAD}$ (max), then the access time is defined by t_{AA}.

(11) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(12) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than t_{RCD} (max), then access time is controlled exclusively by t_{CAC}.

(13) For fast-page read operation, the definition of access time is as follows:

$\overline{CAS}$ and Column Address Input Conditions	Access Time Definition
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{ACP}
$t_{CP} \leq t_{CP}$ (max), $t_{ASC} \leq t_{CP}$	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \leq t_{ASC}$ (max)	t_{AA}
$t_{CP} \geq t_{CP}$ (max), $t_{ASC} \geq t_{CP}$	t_{CAC}

(14) The t_{CRP} requirement should be applicable for $\overline{RAS}/\overline{CAS}$ cycles preceded by any cycle.

(15) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

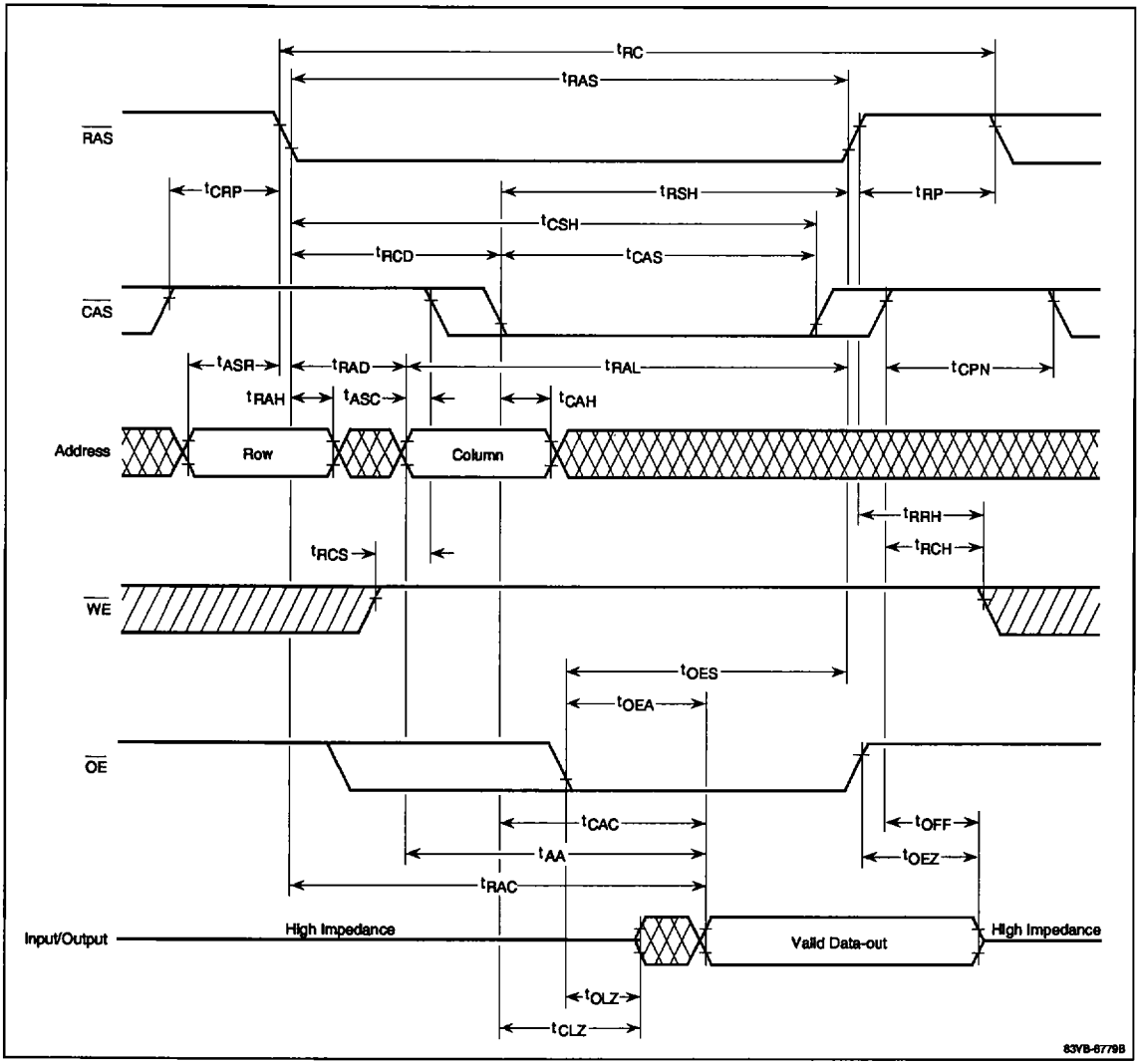
(16) Parameter t_{WP} is applicable for a delayed write cycle such as a read-write/read-modify-write cycle. For early write operation, both t_{WCS} and t_{WCH} must be met.

(17) These parameters are referenced to the falling edge of $\overline{CAS}$ for early write cycles and to the falling edge of $\overline{WE}$ for delayed write or read-modify-write cycles.

(18) For D_{OUT9} parameters t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are restrictive operating parameters in read-write/read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of D_{OUT9} (at access time and until $\overline{CAS_9}$ returns to V_{IH}) is indeterminate.

Timing Waveforms

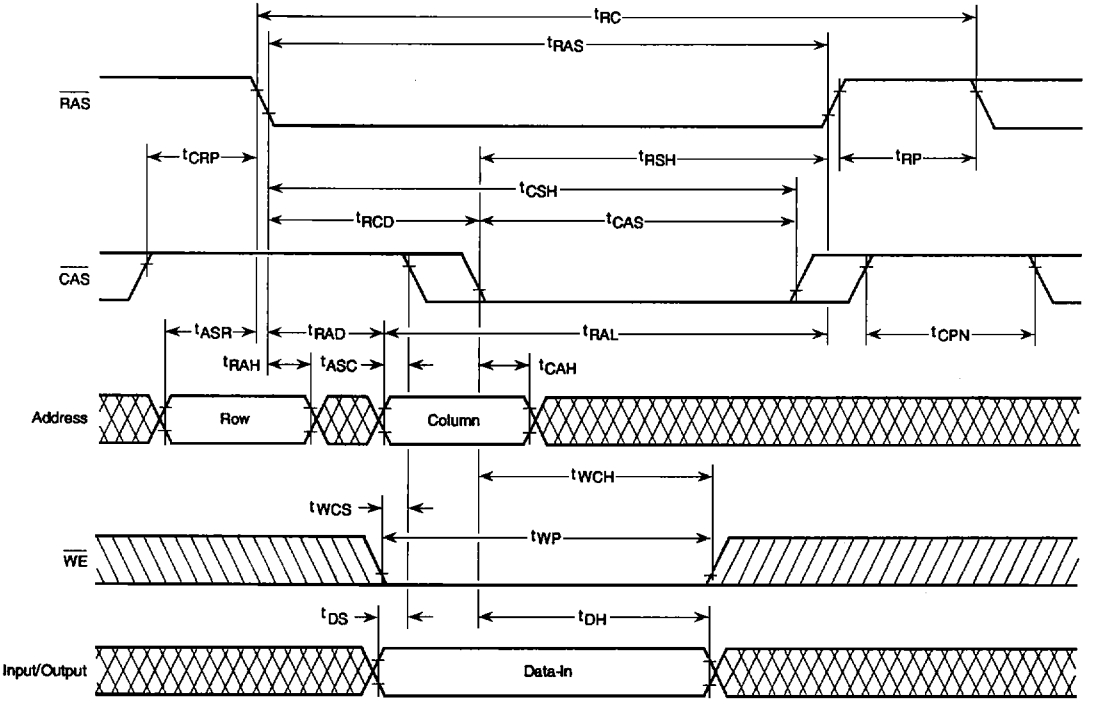
Read Cycle



9a

Timing Waveforms (cont)

Early Write Cycle

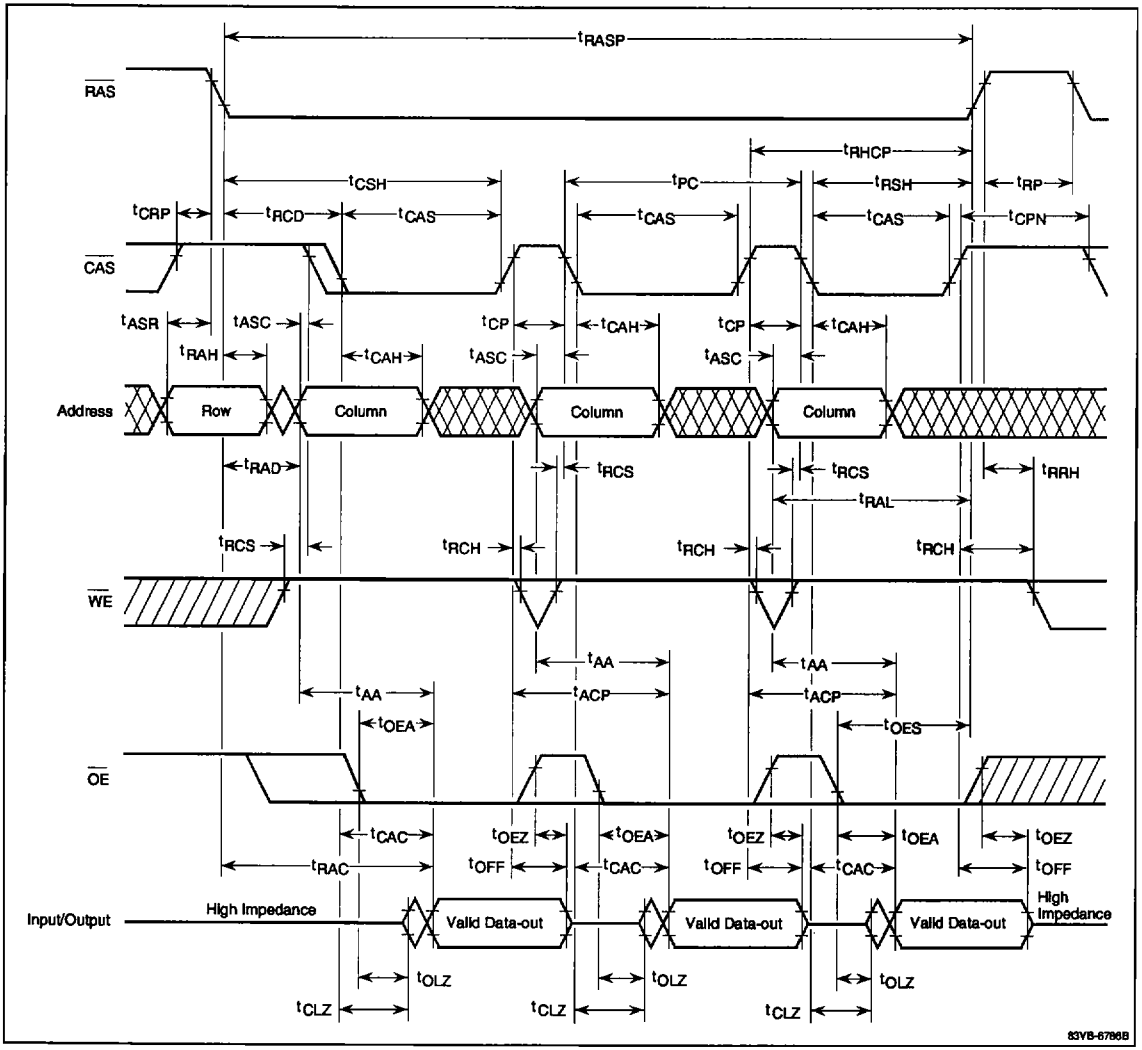


Note:
[1] $\overline{OE}$ = don't care.

83YL-6978B

Timing Waveforms (cont)

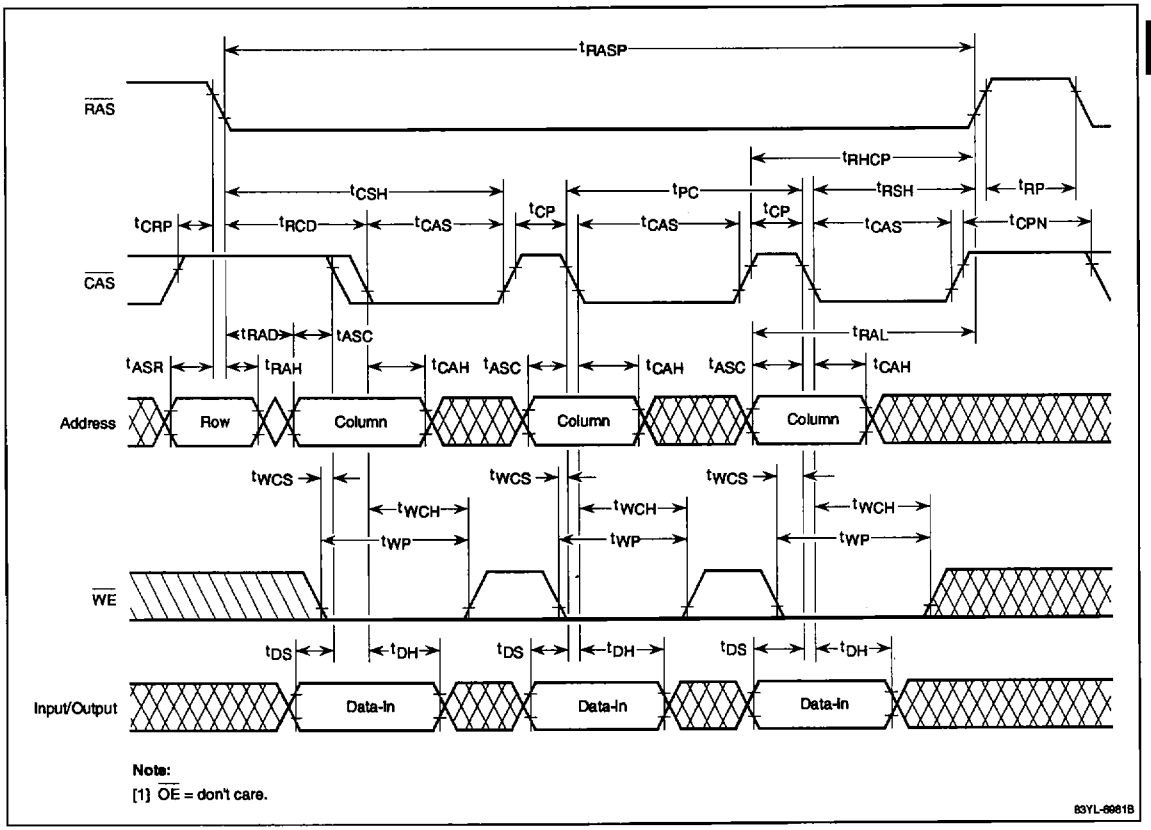
Fast-Page Read Cycle



9a

Timing Waveforms (cont)

Fast-Page Early Write Cycle

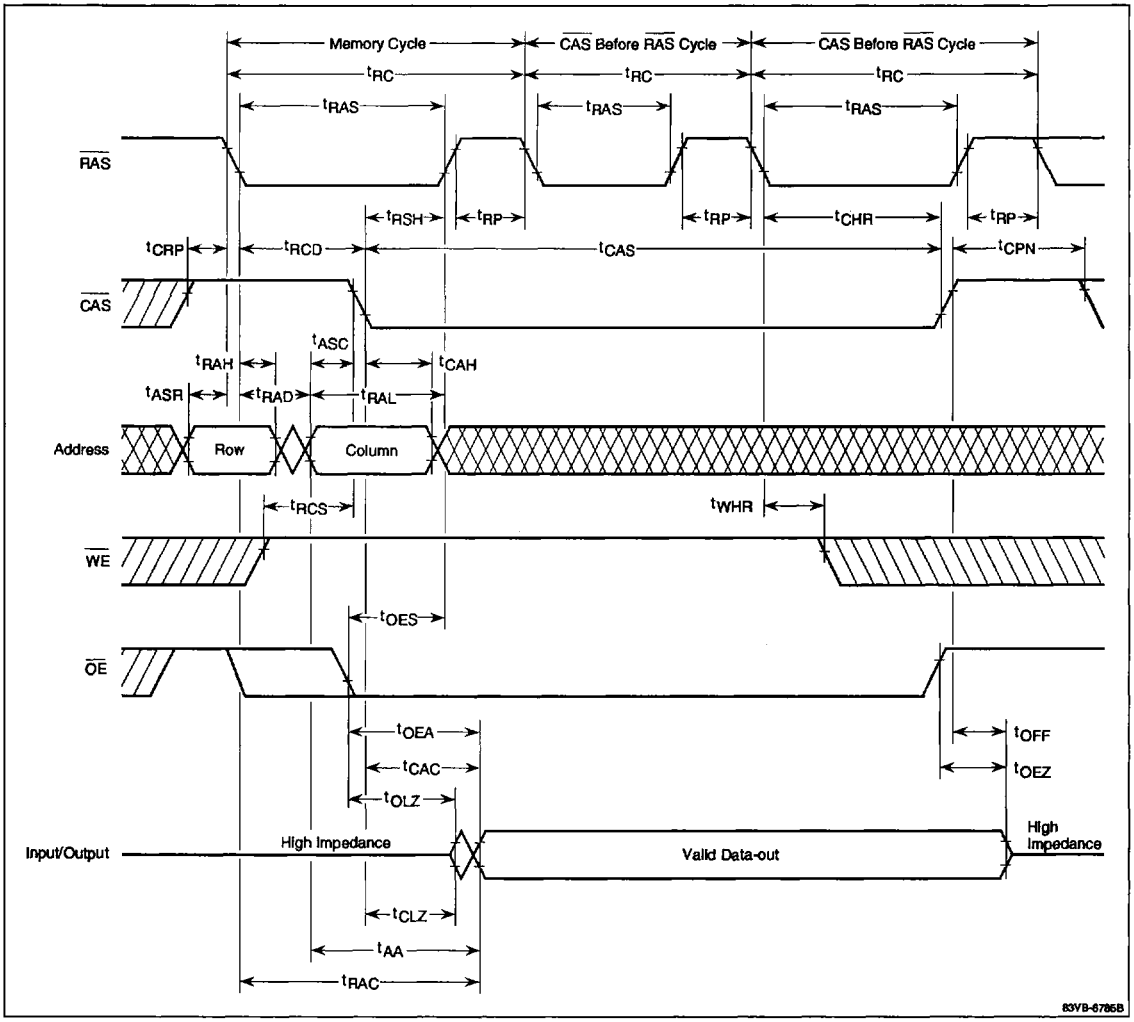


Note:
[1] $\overline{OE}$ = don't care.

83YL-6661B

Timing Waveforms (cont)

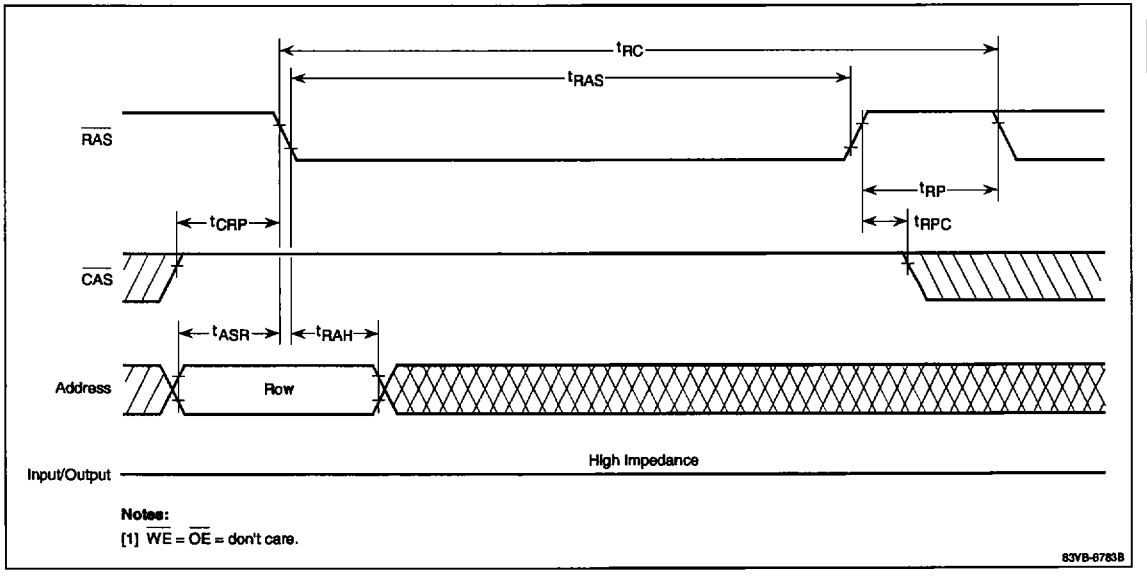
Hidden Refresh Cycle



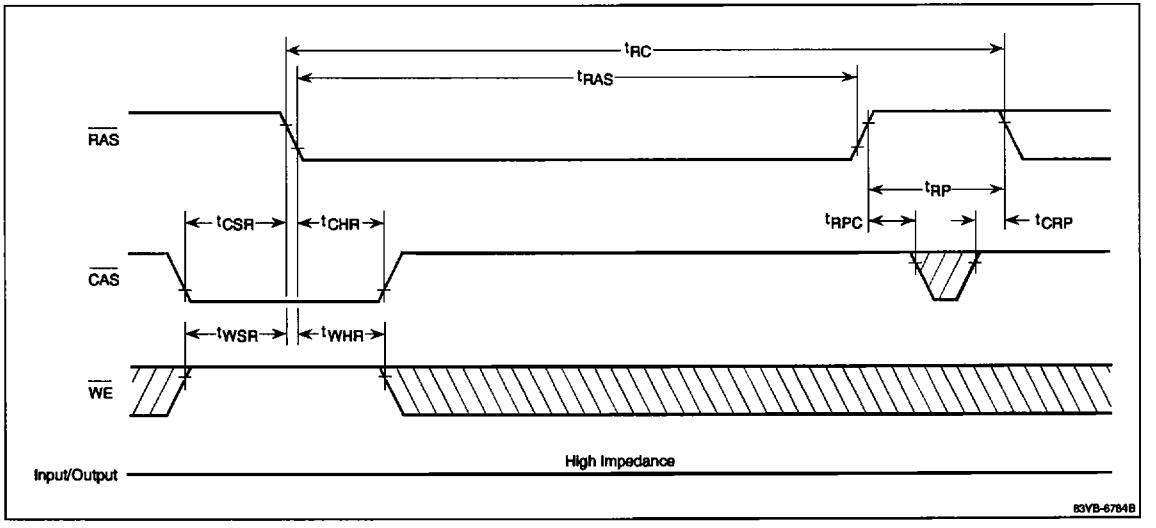
9a

Timing Waveforms (cont)

$\overline{RAS}$-Only Refresh Cycle



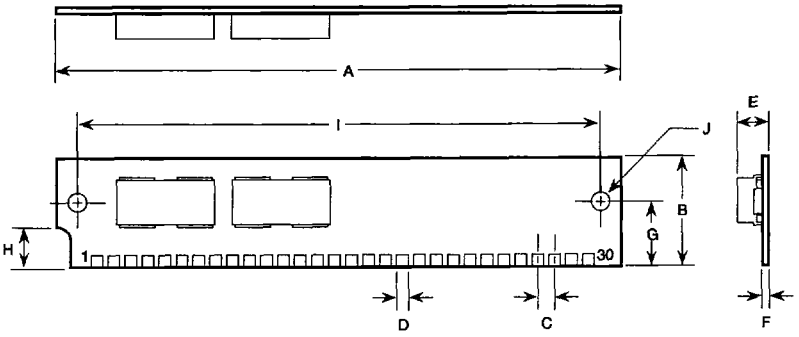
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Package Drawing

30-Pin Socket-Mountable SIMM (MC-42256AB8, Suffix BA or FA)

Item	Millimeters	Inches
A	88.90	3.500
B	16.80 max	.661 max
C	2.54	.100
D	1.78	.070
E	5.08 max	.200 max
F	1.27 ± .08	.050 ± .0032
G	10.16	.400
H	6.35	.250
I	82.10	3.232
J	3.175 dia	.125 dia



MC-42256AB8BA/FA

83YL-67468