No.:	RMNW–K–HTS-0001 /3
Date:	2017. 4. 21

Data sheet

Title: FIXED THICK FILM CHIP RESISTORS; RECTANGULAR TYPE & ANTI-SULFURATION

Style: RMNW10,16,20,32,35

AEC-Q200 qualified

RoHS COMPLIANCE ITEM
Halogen and Antimony Free

Note: ・Stock conditions
Temperature: +5°C ~ +35°C
Relative humidity: 25% ~ 75%
The period of guarantee: Within 2 year from shipmen t by the company.
Solderability shall be satisfied.
・Product specification contained in this data sheet
are subject to change at any time without notice
・If you have any questions or a Purchasing Specification for any quality Agreement is necessary, please contact our sales staff.

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1. Scope

1.1 This data sheet covers the detail requirements for fixed thick film chip resistors; rectangular type & anti-sulfuration, style of RMNW10,16,20,32,35.

1.2 Applicable documents

JIS C 5201−1: 2011, AEC-Q200 Rev.D

2. Classification

Type designation shall be the following form.

(Example) 1)

RMNW	16	K	123	J	TP
1	2	3	4	5	6
Style					

2)

RMNW	16		JP		TP
1	2		4		6
Style					

1 Fixed thick film chip resistors; rectangular type & anti-sulfuration
2 Rated dissipation and / or dimension
3 Temperature coefficient of resistance — Style

K	±100×10^{-6}/ °C
−(Dash)	Standard

4 Rated resistance

123	E24 Series, 3 digit, Ex. 123--> 12kΩ,
1000	E96 Series, 4 digit, Ex. 1000-->100Ω 1022--> 10.2kΩ
JP	Chip jumper

5 Tolerance on rated resistance

D	±0.5%
F	±1%
J	±5%

6 Packaging form

B	Bulk (loose package)
TH	Paper taping
TP	
TE	Embossed taping

3. Rating

3.1 The ratings shall be in accordance with Table–1.

Table–1

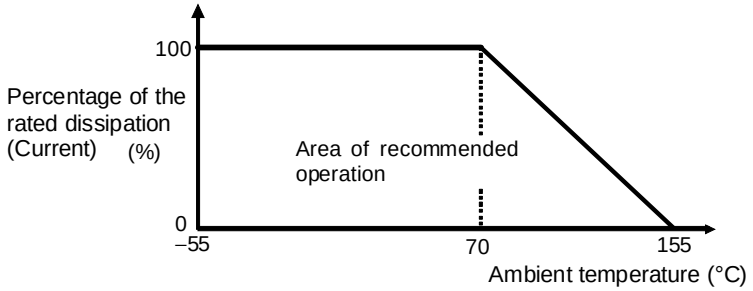
Style	Rated dissipation (W)	Temperature coefficient of resistance (10^{-6} / °C)		Rated resistance range (Ω)	Preferred number series for resistors	Tolerance on rated resistance
RMNW10	0.1	K	±100	10.2~1M	E24, 96	F(±1%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
		K	±100	10.2~1M	E24	J(±5%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
RMNW16	0.1	K	±100	10~1M	E24, 96	D(±0.5%)
		K	±100	10.2~1M	E24, 96	F(±1%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
		K	±100	10.2~1M	E24	J(±5%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
RMNW20	0.125	K	±100	10.2~1M	E24, 96	F(±1%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
		K	±100	10.2~1M	E24	J(±5%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
RMNW32	0.25	K	±100	10.2~1M	E24, 96	F(±1%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
		K	±100	10.2~1M	E24	J(±5%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
RMNW35	0.5	K	±100	10.2~1M	E24, 96	F(±1%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		
		K	±100	10.2~1M	E24	J(±5%)
		Standard	±200	1.02M~10M		
			+400~–200	1.0~10		

Style	Limiting element voltage (V)	Max. Overload voltage(V)	Category temperature range (°C)
RMNW10	50	100	–55~+155
RMNW16	50	100	
RMNW20	150	300	
RMNW32	200	400	
RMNW35	200	400	

Style	Resistance value of chip jumper	Rated current of chip jumper (A)	Peak current of chip jumper (A)
RMNW10	50mΩ max.	1	1.5
RMNW16		1	3
RMNW20		1.5	3.5
RMNW32		2	5
RMNW35		3	6

3.2 Derating

The derated values of dissipation (or current rating in case of chip jumper) at temperature in excess of 70 °C shall be as indicated by the following curve.



Figure–1 Derating curve

3.3 Rated voltage

d. c. or a. c. r. m. s. voltage calculated from the square root of the product of the rated resistance and the rated dissipation.

$$E = \sqrt{P \cdot R}$$

E : Rated voltage (V)
P : Rated dissipation (W)
R : Rated resistance (Ω)

Limiting element voltage can only be applied to resistors when the resistance value is equal to or higher than the critical resistance value.

At high value of resistance, the rated voltage may not be applicable.

4. Packaging form

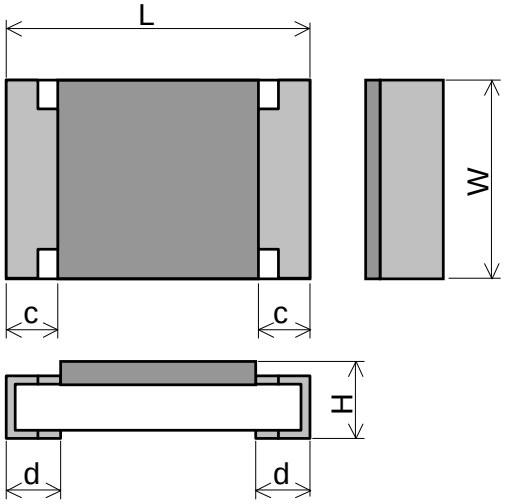
The standard packaging form shall be in accordance with Table–2.

Table–2

Symbol	Packaging form		Standard packaging quantity / units	Application
B	Bulk (loose package)		10,000 pcs.	RMNW10
			5,000 pcs.	RMNW16,20,32,35
TH	Paper taping	8mm width, 2mm pitches	10,000 pcs.	RMNW10
TP	Paper taping	8mm width, 4mm pitches	5,000 pcs.	RMNW16,20,32,35

5. Dimensions

5.1 The resistor shall be of the design and physical dimensions in accordance with Figure−2 and Table−3.



Figure−2

Table−3 Unit : mm

Style	L	W	H	c	d
RMNW10	1.0±0.05	0.5±0.05	0.35±0.1	0.2±0.2	0.25±0.10
RMNW16	1.6±0.2	0.8±0.1	0.45±0.15	0.3±0.1	0.3±0.15
RMNW20	2.0±0.1	1.25±0.1	0.5±0.15	0.4±0.2	0.4±0.2
RMNW32	3.1±0.1	1.6±0.1	0.6±0.15	0.5±0.2	0.45±0.20
RMNW35	3.1±0.1	2.6±0.1	0.55±0.10	0.5±0.2	0.5±0.2

6. Marking

The Rated resistance of RMNW10 should not be marked.

6.1 RMNW20,32,35

The nominal resistance shall be marked in 3 digits or 4 digits and marked on over coat side.

- J(±5%): 3 digits, F(±1%): 4 digits

Marking example	Contents	Application
123	12×10^{3} [Ω] → 12 [kΩ]	E24
2R2	2. 2 [Ω]	E24, Less than 10Ω
5623	562×10^{3} [Ω] → 562[kΩ]	E24, E96
12R7	12.7 [Ω]	E24, E96

6.2 RMNW16

The nominal resistance shall be marked in 3 digits (E24 and/or E96) and marked on over coat side.

In case of the resistance value that E96 overlaps with E24, there is a case to mark in E96.

Marking example	Contents	Application
123	12×10^{3} [Ω] → 12 [kΩ]	E24
2R2	2. 2 [Ω]	E24
02C	102×10^{2} [Ω] → 10.2 [kΩ]	E96
51X	332×10^{-1} [Ω] → 33.2 [Ω]	E96

6.2.1 Symbol for E96 series of resistance value

E96	Symbol	E96	Symbol	E96	Symbol	E96	Symbol	E96	Symbol
100	01	162	21	261	41	422	61	681	81
102	02	165	22	267	42	432	62	698	82
105	03	169	23	274	43	442	63	715	83
107	04	174	24	280	44	453	64	732	84
110	05	178	25	287	45	464	65	750	85
113	06	182	26	294	46	475	66	768	86
115	07	187	27	301	47	487	67	787	87
118	08	191	28	309	48	499	68	806	88
121	09	196	29	316	49	511	69	825	89
124	10	200	30	324	50	523	70	845	90
127	11	205	31	332	51	536	71	866	91
130	12	210	32	340	52	549	72	887	92
133	13	215	33	348	53	562	73	909	93
137	14	221	34	357	54	576	74	931	94
140	15	226	35	365	55	590	75	953	95
143	16	232	36	374	56	604	76	976	96
147	17	237	37	388	57	619	77		
150	18	243	38	392	58	634	78		
154	19	249	39	402	59	649	79		
158	20	255	40	412	60	665	80		

6.2.2 Symbol of multipliers

Symbol	Y	X	A	B	C	D	E	F
Multipliers	10^{-2}	10^{-1}	10^{0}	10^{1}	10^{2}	10^{3}	10^{4}	10^{5}

6.3 Marking example of Jumper Chip

Marking example	Contents	Application
000	JP	RMNW10, 16,20,32,35

7. Performance

7.1 The standard condition for tests shall be in accordance with Sub–clause 4.2, JIS C 5201–1: 2011.

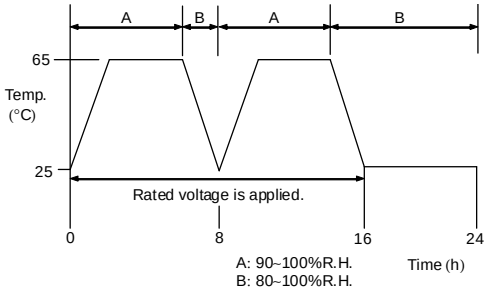
7.2 The performance shall be satisfied in Table–4.

Table–4(1)

No.	Test items	Condition of test (JIS C 5201–1)	Performance requirements
1	Resistance	Sub–clause 4.5	As in 4.5.2 The resistance value shall correspond with the rated resistance taking into account the specified tolerance. Chip jumper: 50mΩ max.
2	Temperature characteristic of resistance	4.8 Natural resistance change per change in degree centigrade. $TCR(10^{-6}/\Omega)= \frac{R2-R1}{R1(t2-t1)} \times 10^{6}$ t1 : 20°C $^{+5}_{-1}$ °C, t2: 155°C $^{+5}_{-1}$ °C R1 : Resistance at t1 temperature R2 : Resistance at t2 temperature	See Table–1.
3	Short time overload	4.13 The applied voltage: 2.5 times the rated voltage Test period: 5s Test potential should not exceed max. overload voltage as shown in Table–1.	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
4	Resistance to soldering heat	MIL-STD-202 Method 210 Test by a piece. Temp. of solder bath: 270±5°C Immersion time: 10±1s After immersion into solder, leaving at the room temp. for 1h or more and then measure the resistance.	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
5	Solderability	J-STD-002 • Pre-condition: 155°C, 4h Temp. of solder bath: 235°C Immersion time: 5s • Pre-condition: Steam aging, 1h Temp. of solder bath: 260°C Immersion time: 7s	The surface of terminal immersed shall be min. of 95% covered with a new coating of solder.
6	Temperature cycling	JESD22 Method JA-104 Test cycle: 1000 cycles for duty cycle as specified below.	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.

Step	Temperature(°C)	Time(min)
1	–55	5~10
2	+155	5~10

Table−4(2)

No	Test items	Condition of test (JIS C 5201−1)	Performance requirements
7	Moisture Resistance	MIL-STD-202 Method 106 Test condition: 10cycles for duty cycle as shown as below.  	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
8	Operational life	MIL-STD-202 Method 108 Test temp.: 125±2°C Test power: 35% of rated power shall be applied for continuously. Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
9	Bias humidity	MIL-STD-202 Method 103 Test condition: 85°C & 85% R.H. Test power: 10% of rated power shall be applied for continuously. Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
10	High Temperature exposure	MIL-STD-202 Method 108 Test condition: 155±2°C Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
11	Substrate bending test	AEC-Q200-005 Bent value: 2 mm(Among the fulcrums: 90mm) Duration: 10s	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
12	Adhesion	AEC-Q200-006 Force: 10.2 N Duration: 60 s±1 s	No remarkable damage or removal of the terminations
13	Thermal shock	MIL-STD-202 Method 107 Test cycle: 300 cycles for duty cycle as specified below.	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
		Step / Temperature(°C) / Time(min) 1 / −55 / 15 2 / +155 / 15	
		Max transfer time: 20s	
14	ESD test	AEC-Q200-200 Test condition: 1000V RMNW10: 500V	Resistor: ΔR/R: Within ±(1.0%+0.05Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.

Table–4(3)

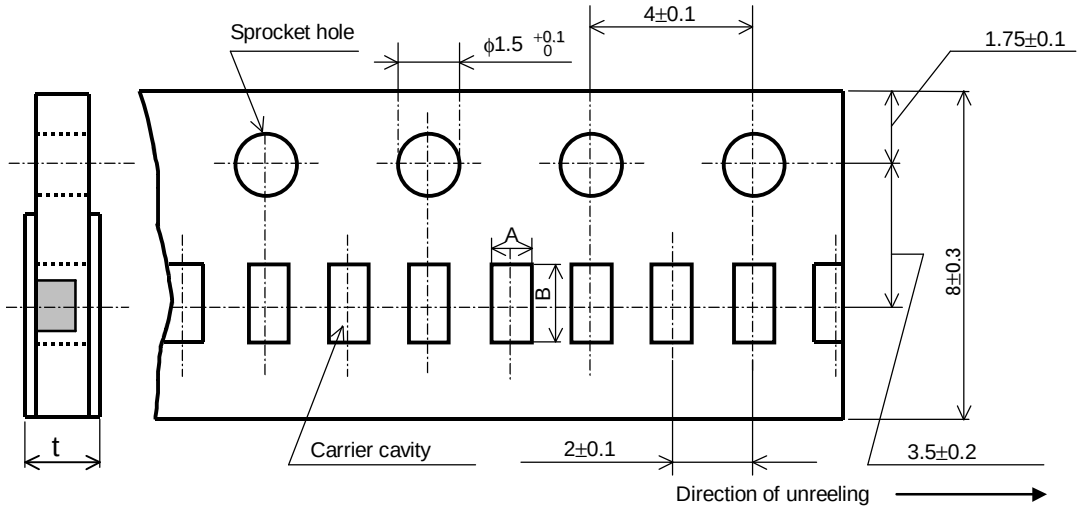
No	Test items	Condition of test (JIS C 5201–1)	Performance requirements
15	Load life in humidity	4.24 Test temp. & relative humidity : 40±2°C & 90~95% R.H. Test voltage: Cycle of 1h 30min "ON" and 30min "OFF" at dc rated voltage. Test period:1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
16	Load life	4.25 Test temp.: 70±2°C Test voltage: Cycle of 1h 30min "ON" and 30min "OFF" at dc rated voltage. Test period: 1,000 $^{+48}_{0}$ h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.
17	Humid sulfur vapor test	ASTM B-809 Test temp.: 60°C Test period: 480h	Resistor: ΔR/R: Within ±(2.0%+0.1Ω) Chip jumper: 50mΩ max. No evidence of appearance damage.

8. Taping

8.1 Paper taping (8mm width, 2mm pitches)

Taping dimensions shall be in accordance with Figure–3 and Table–5.

Unit: mm



Figure–3

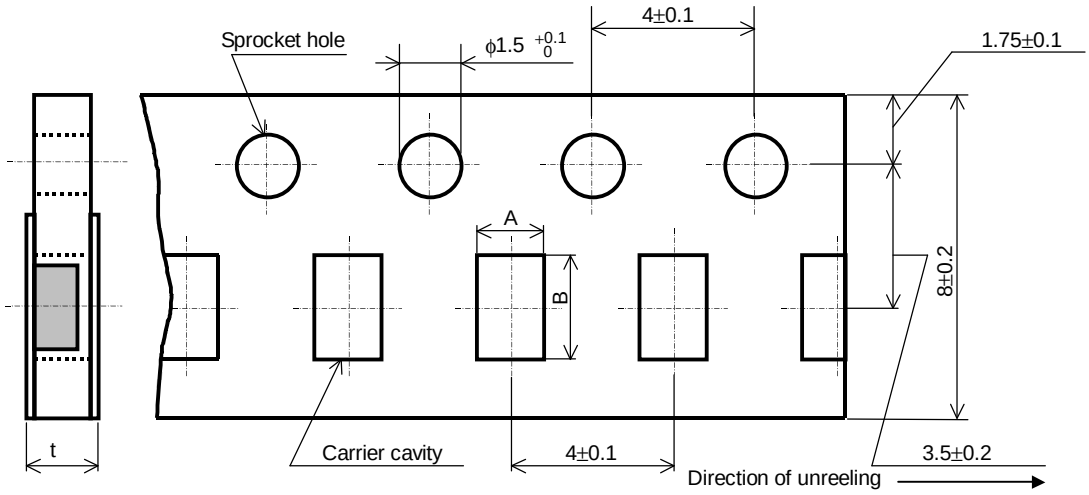
Table–5 Unit: mm

Style	A	B	t
RMNW10	0.7±0.1	1.2±0.1	0.4±0.05

8.2 Paper taping (8mm width, 4mm pitches)

Taping dimensions shall be in accordance with Figure–4 and Table–6.

Unit: mm



Figure–4

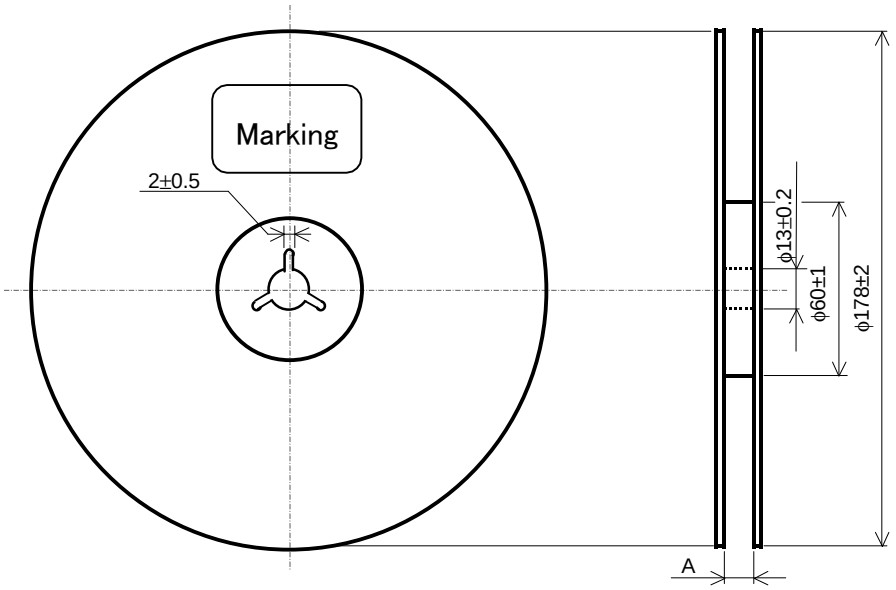
Table–6 Unit: mm

Style	A	B	t
RMNW16	1.1±0.2	1.9±0.2	0.65±0.05
RMNW20	1.65±0.20	2.4±0.2	1.0 Max.
RMNW32	2.0±0.2	3.6±0.2	1.0 max.
RMNW35	3.0±0.2	3.6±0.2	1.0 max.

8.3 Reel dimension

Reel dimensions shall be in accordance with the following Figure–5 and Table–7.

Unit: mm



Figure–5

Table–7 Unit: mm

Style	A
RMNW10, 16, 20, 32, 35	9±0.5

9. Marking on package

The label of a minimum package shall be legibly marked with follows.

(1) Classification (Style, Temperature coefficient of resistance, Rated resistance, Tolerance on rated resistance, Packaging form)

(2) Quantity (3) Lot number (4) Manufacturer's name or trade mark (5) Others