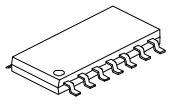
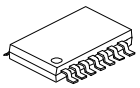
# U74ACT02

***CMOS IC***

## QUADRUPLE 2-INPUT POSITIVE-NOR GATES



SOP-14



TSSOP-14

## ■ DESCRIPTION

The UTC **U74ACT02** contains four independent 2-input positive-nor gates. Each Gate Performs the Boolean function $Y=\overline{A+B}$ or $Y=\overline{A}\cdot\overline{B}$

## ■ FEATURES

* Operation Voltage Range: 4.5~5.5V
* Low Power Dissipation: $I_{CC}$=2μA (Max.)
* High Noise Immunity
* Compatible With TTL Output

## ■ ORDERING INFORMATION

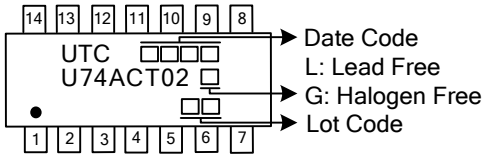
| Ordering Number | | Package | Packing |
|---|---|---|---|
| Lead Free | Halogen Free | | |
| U74ACT02L-S14-R | U74ACT02G-S14-R | SOP-14 | Tape Reel |
| U74ACT02L-P14-R | U74ACT02G-P14-R | TSSOP-14 | Tape Reel |

U74ACT02G-S14-R

(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S14: SOP-14, P14: TSSOP-14
(3) G: Halogen Free and Lead Free, L: Lead Free

## ■ MARKING





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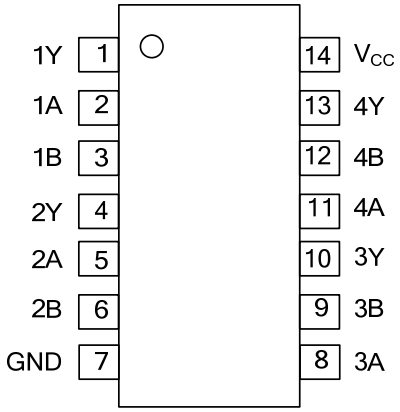
## ■ PIN CONFIGURATION

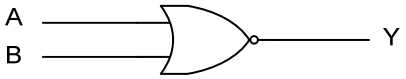



## ■ FUNCTION TABLE

| INPUT(A) | INPUT(B) | OUTPUT(Y) |
|---|---|---|
| H | X | L |
| X | H | L |
| L | L | H |

H = High voltage level；L = Low voltage level；X = Don't care

## ■ LOGIC DIAGRAM (positive gate)



## ■ ABSOLUTE MAXIMUM RATING ($T_A$=25°C, unless otherwise specified) (Note 2)

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | -0.5 ~ 7.0 | V |
| Input Voltage | $V_{IN}$ | -0.5 ~ $V_{CC}$ +0.5 | V |
| Output Voltage | $V_{OUT}$ | -0.5 ~ $V_{CC}$ +0.5 | V |
| Input Clamp Current ($V_{IN}$ < 0 or $V_{IN}$ > $V_{CC}$) | $I_{IK}$ | ±20 | mA |
| Output Clamp Current ($V_{OUT}$ < 0 or $V_{OUT}$ > $V_{CC}$) | $I_{OK}$ | ±20 | mA |
| Output Current ($V_{OUT}$=0V ~ $V_{CC}$) | $I_{OUT}$ | ±50 | mA |
| $V_{CC}$ or GND Current | $I_{CC}$ | ±200 | mA |
| Storage Temperature | $T_{STG}$ | -65 ~ +150 | °C |

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

## ■ RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.5 ~ 5.5 | V |
| Input Voltage | $V_{IN}$ | 0 ~ $V_{CC}$ | V |
| Output Voltage | $V_{OUT}$ | 0 ~ $V_{CC}$ | V |
| Input Transition Rise or Fall Rate | Δt/Δv | 10 | ns/V |
| Operating Temperature | $T_A$ | -40 ~ +125 | °C |

## ■ ELECTRICAL CHARACTERISTICS ($T_A$ =25°C , unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| High Level Input Voltage | $V_{IH}$ | $V_{CC}$=4.5~5.5V | | 2 | | | V |
| Low Level Input Voltage | $V_{IL}$ | $V_{CC}$=4.5~5.5V | | | | 0.8 | V |
| High-Level Output Voltage | $V_{OH}$ | $V_{CC}$=4.5V | $I_{OH}$=-24mA | 3.86 | | | V |
| | | | $I_{OH}$=-50μA | 4.4 | 4.49 | | V |
| | | $V_{CC}$=5.5V | $I_{OH}$=-24mA | 4.86 | | | V |
| | | | $I_{OH}$=-50μA | 5.4 | 5.49 | | V |
| Low-Level Output Voltage | $V_{OL}$ | $V_{CC}$=4.5V | $I_{OL}$=24mA | | | 0.36 | V |
| | | | $I_{OL}$=50μA | | 0.001 | 0.1 | V |
| | | $V_{CC}$=5.5V | $I_{OL}$=24mA | | | 0.36 | V |
| | | | $I_{OL}$=50μA | | 0.001 | 0.1 | V |
| Input Leakage Current | $I_{I(LEAK)}$ | $V_{CC}$=5.5V, $V_{IN}$=$V_{CC}$ or GND | | | | ±0.1 | μA |
| Quiescent Supply Current | $I_Q$ | $V_{CC}$=5.5V, $V_{IN}$=$V_{CC}$ or GND, $I_{OUT}$=0A | | | | 2 | μA |
| Additional Quiescent Supply Current Per Input Pin | $\Delta I_Q$ | $V_{CC}$=5.5V, One input at 3.4V, Other inputs at $V_{CC}$ or GND | | | 0.6 | | mA |
| Input Capacitance | $C_I$ | $V_{CC}$= 5V, $V_{IN}$= $V_{CC}$ or GND | | | 2.6 | | pF |

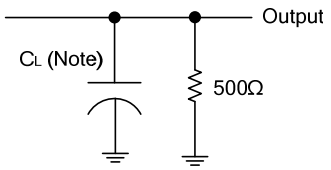
## ■ SWITCHING CHARACTERISTICS ($T_A$ =25°C , unless otherwise specified)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Propagation delay from input (A or B) to output(Y) | $t_{PLH}$ / $t_{PHL}$ | $V_{CC}$=5V±0.5V, $C_L$=50pF, $R_L$=500Ω | 1.0 | 6.5 | 9.0 | ns |

## ■ OPERATING CHARACTERISTICS ($T_A$ =25°C , unless otherwise specified)

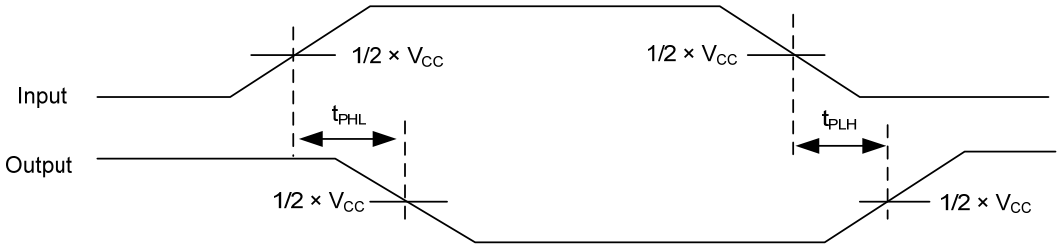
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Dissipation Capacitance | $C_{PD}$ | $V_{CC}$=5.0V, $C_L$=50pF, f=10MHz | | 40 | | pF |

## ■ TEST CIRCUIT AND WAVEFORMS




TEST CIRCUIT

Note : $C_L$ includes probe and jig capacitance.




**PROPAGATION DELAY FROM INPUT(A) TO OUTPUT(Y).**

Notes: 1. $C_L$ includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: PRR ≤1MHz, $Z_O$ = 50Ω.

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