

TS1M3660G

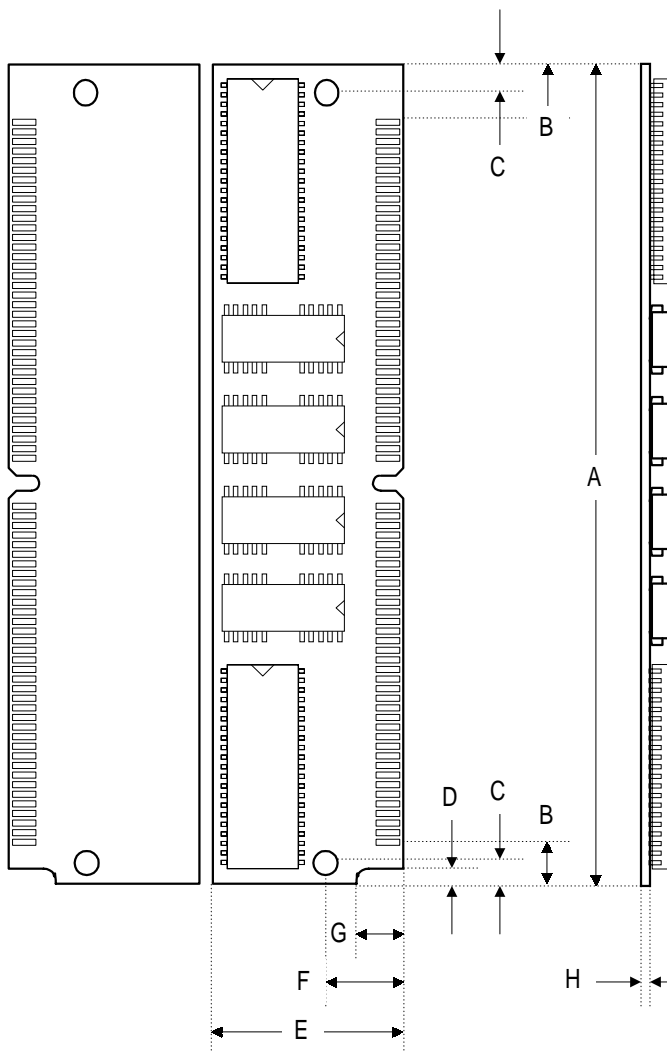
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DRAM SIMM With 1Mx16 5VOLT

Description

The TS1M3660G is a 1M by 36-bit dynamic RAM module with 2 pcs of 1Mx16 and 4 pcs 1Mx1 DRAMs assembled on the printed circuit board.

The TS1M3660G is optimized for application to systems which require high density and large capacity along with compact sizing.

Placement



PCB : 09 - 5215G

Features

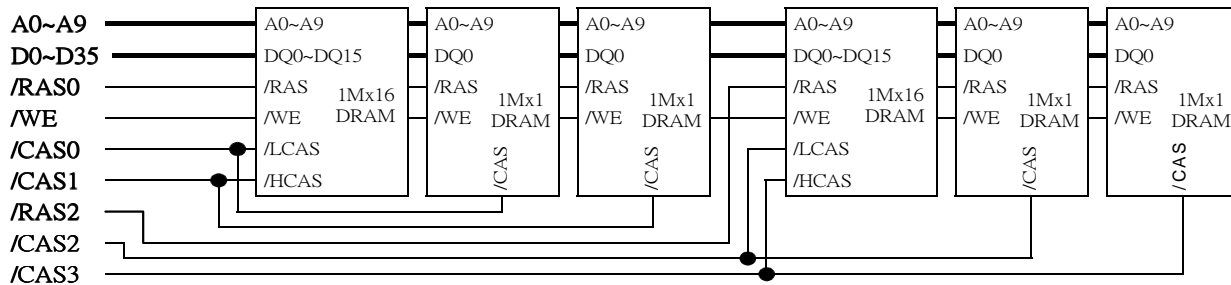
- Fast Page Mode Operation.
- Single +5.0V \pm 10% power supply.
- 1,024 cycles refresh.
- Lower power consumption.
- CAS before RAS refresh, RAS only refresh, Hidden refresh, Fast Page Mode, Read_Modify_Write capability.

| TS4M3260 | |
|---|-------|
| Access time from /RAS t _{RAC} | 60ns |
| Access time from /CAS t _{CAC} | 15ns |
| Random read/write cycle time t _{RC} | 110ns |
| Page mode cycle time t _{PC} | 40ns |

Dimensions

| Side | Millimeters | Inches |
|------|-------------------|-------------------|
| A | 107.95 \pm 0.20 | 4.520 \pm 0.008 |
| B | 6.35 | 0.250 |
| C | 3.38 | 0.133 |
| D | 2.03 | 0.080 |
| E | 25.40 \pm 0.20 | 0.850 \pm 0.008 |
| F | 10.16 | 0.400 |
| G | 6.35 | 0.250 |
| H | 1.27 \pm 0.10 | 0.050 \pm 0.004 |

TS1M3660G -- Block Diagram



Pinouts

| Pin No | Pin Name | Pin No | Pin Name | Pin No | Pin Name |
|--------|----------|--------|----------|--------|----------|
| 01 | Vss | 25 | D22 | 49 | D8 |
| 02 | D0 | 26 | D7 | 50 | D24 |
| 03 | D16 | 27 | D23 | 51 | D9 |
| 04 | D1 | 28 | A7 | 52 | D25 |
| 05 | D17 | 29 | NC | 53 | D10 |
| 06 | D2 | 30 | Vcc | 54 | D26 |
| 07 | D18 | 31 | A8 | 55 | D11 |
| 08 | D3 | 32 | A9 | 56 | D27 |
| 09 | D19 | 33 | NC | 57 | D12 |
| 10 | Vcc | 34 | /RAS2 | 58 | D28 |
| 11 | NC | 35 | NC | 59 | Vcc |
| 12 | A0 | 36 | NC | 60 | D29 |
| 13 | A1 | 37 | NC | 61 | D13 |
| 14 | A2 | 38 | NC | 62 | D30 |
| 15 | A3 | 39 | Vss | 63 | D14 |
| 16 | A4 | 40 | /CAS0 | 64 | D31 |
| 17 | A5 | 41 | /CAS2 | 65 | D15 |
| 18 | A6 | 42 | /CAS3 | 66 | NC |
| 19 | A10 | 43 | /CAS1 | 67 | PD1 |
| 21 | D20 | 45 | NC | 69 | PD3 |
| 22 | D5 | 46 | NC | 70 | PD4 |
| 23 | D21 | 47 | /WE | 71 | NC |
| 24 | D6 | 48 | NC | 72 | Vss |

Pin Identification

| Symbol | Function |
|---------------|----------------------------|
| A0 ~ A9 | Address inputs |
| D0 ~ D35 | Common data inputs/outputs |
| /RAS0, /RAS2 | Row address strobes |
| /CAS0 ~ /CAS3 | Column address strobes |
| /WE | Write enable |
| Vcc | +5.0 Volt power supply |
| Vss | Ground |
| NC | No connection |
| PD1 ~ PD4 | Presence detection pin |

| | PD1 | PD2 | PD3 | PD4 |
|------|-----|-----|-----|-----|
| 60ns | Vss | Vss | NC | NC |

This technical information is based on industry standard data and tests believed to be reliable. However, Transcend makes no warranties, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.

ABSOLUTE MAXIMUM RATINGS*

| Item | Symbol | Rating | Unit |
|---|------------------------------------|-------------|------|
| Voltage on any pin relative to V _{ss} | V _{IN} , V _{OUT} | -1 to +7.0 | V |
| Voltage on V _{cc} supply relative to V _{ss} | V _{cc} | -1 to +7.0 | V |
| Storage temperature | T _{stg} | -55 to +150 | °C |
| Power dissipation | P _D | 5 | W |
| Short circuit output current | I _{os} | 50 | mA |

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATION CONDITIONS (Voltage referenced to V_{ss}, T_A = 0 to 70°C)

| Item | Symbol | Min | Typ | Max | Unit |
|--------------------|-----------------|--------------------|-----|-------------------------------|------|
| Supply Voltage | V _{cc} | 4.5 | 5.0 | 5.5 | V |
| Ground | V _{ss} | 0 | 0 | 0 | V |
| Input High Voltage | V _{IH} | 2.4 | - | V _{cc} ^{*1} | V |
| Input Low Voltage | V _{IL} | -1.0 ^{*2} | - | 0.8 | V |

Note: *1: V_{cc} +2.0V at pulse width ≤ 20s, witch is measured at V_{cc}.

*2: -2.0V at pulse width ≤ 20ns, witch is measured at V_{ss}.

DC AND OPERATION CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

| Symbol | Min | Max | Unit |
|-------------------|-----|-----|------|
| I _{CC1} | - | 640 | mA |
| I _{CC2} | - | 12 | mA |
| I _{CC3} | - | 640 | mA |
| I _{CC4} | - | 460 | mA |
| I _{CC5} | - | 6 | mA |
| I _{CC6} | - | 640 | mA |
| I _{I(L)} | -10 | 30 | uA |
| I _{O(L)} | -5 | 5 | uA |
| V _{OH} | 2.4 | - | V |
| V _{OL} | - | 0.4 | V |

I_{CC1}: Operation Current* (/RAS, /CAS, Address cycling @t_{RC}=min)

I_{CC2}: Standby Current (/RAS=/CAS=/W=V_{IH})

I_{CC3}: /RAS Only Refresh Current* (/CAS=V_{IH}, /RAS cycling @t_{RC}=min)

I_{CC4}: Fast Page Mode Current* (/RAS=V_{IL}, /CAS cycling: t_{PC}=min)

I_{CC5}: Standby Current (/RAS=/CAS=/W=V_{CC}-0.2V)

I_{CC6}: /CAS-Before-/RAS Refresh Current* (/RAS and /CAS cycling @t_{RC}=min)

I_{I(L)}: Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.5V$, all other pins not under test=0 V)

I_{O(L)}: Output Leakage Current (Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

V_{OH}: Output High Voltage Level (I_{OH} = -5mA)

V_{OL}: Output Low Voltage Level (I_{OL} = 4.2mA)

***Note:** I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once within one Fast page mode cycle time, t_{PC}.

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CAPACITANCE (TA = 25°C, Vcc = 5V, f = 1MHz)

| Item | Symbol | Min | Max | Unit |
|--|------------------|-----|-----|------|
| Input capacitance (A0~A11) | C _{IN1} | - | 50 | pF |
| Input capacitance (/WE) | C _{IN2} | - | 60 | pF |
| Input capacitance (/RAS0, /RAS2) | C _{IN3} | - | 40 | pF |
| Input capacitance (/CAS0~/CAS3) | C _{IN4} | - | 34 | pF |
| Data input/output capacitance (D0~D31) | C _{DQ} | - | 20 | pF |

AC CHARACTERISTICS (0°C ≤ TA ≤ 70°C, Vcc=5.0V ± 10%, See notes 1, 2)

Test condition: Vih/Vil=2.4/0.8V, Voh/Vol=2.4/0.4V, output loading CL=100pF

| Parameter | Symbol | Min | Max | Unit | Note |
|---------------------------------|------------------|-----|-----|------|-------|
| Random read or write cycle time | t _{RC} | 110 | | ns | |
| Access time from /RAS | t _{RAC} | | 60 | ns | 3,4 |
| Access time from /CAS | t _{CAC} | | 15 | ns | 3,4,5 |
| Access time from column address | t _{AA} | | 30 | ns | 3,10 |
| /CAS to output in Low-Z | t _{CLZ} | 0 | | ns | 3 |
| Output buffer turn-off delay | t _{OFF} | 0 | 15 | ns | 6 |
| Transition time(rise and fall) | t _T | 3 | 50 | ns | 2 |
| /RAS precharge time | t _{RP} | 40 | | ns | |
| /RAS pulse width | t _{RAS} | 60 | 10K | ns | |
| /RAS hold time | t _{RSH} | 15 | | ns | |

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AC CHARACTERISTICS ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$, $V_{CC}=5.0\text{V} \pm 10\%$, See notes 1, 2)

Test condition: $V_{ih}/V_{il}=2.4/0.8\text{V}$, $V_{oh}/V_{ol}=2.4/0.4\text{V}$, output loading $CL=100\text{pF}$

| Parameter | Symbol | Min | Max | Unit | Note |
|---|-------------------|-----|------|------|------|
| /CAS hold time | t _{CSH} | 60 | | ns | |
| /CAS pulse width | t _{CAS} | 15 | 10K | ns | |
| /RAS to /CAS delay time | t _{RCD} | 20 | 45 | ns | 4 |
| /RAS to column address delay time | t _{RAD} | 15 | 30 | ns | 10 |
| /CAS to /RAS precharge time | t _{CRP} | 5 | | ns | |
| Row address set-up time | t _{ASR} | 0 | | ns | |
| Row address hold time | t _{RAH} | 10 | | ns | |
| Column address set-up time | t _{ASC} | 0 | | ns | |
| Column address hold time | t _{CAH} | 10 | | ns | |
| Column address to /RAS lead time | t _{RAL} | 30 | | ns | |
| Read command set-up time | t _{RCS} | 0 | | ns | |
| Read command hold referenced to /CAS | t _{RCH} | 0 | | ns | 8 |
| Read command hold referenced to /RAS | t _{RRH} | 0 | | ns | 8 |
| Write command hold time | t _{WCH} | 10 | | ns | |
| Write command pulse width | t _{WP} | 10 | | ns | |
| Write command to /RAS lead time | t _{RWL} | 15 | | ns | |
| Write command to /CAS lead time | t _{CWL} | 15 | | ns | |
| Date set-up time | t _{DS} | 0 | | ns | 9 |
| Date hold time | t _{DH} | 10 | | ns | 9 |
| Refresh period | t _{REF} | | 16 | ms | |
| Write command set-up time | t _{WCS} | 0 | | ns | 7 |
| /CAS setup time(/CAS-before-/RAS refresh) | t _{CSR} | 5 | | ns | |
| /CAS hold time (/CAS-before-/RAS refresh) | t _{CHR} | 10 | | ns | |
| /RAS to /CAS precharge time | t _{RPC} | 5 | | ns | |
| Access time from /CAS precharge | t _{CPA} | | 35 | ns | 3 |
| Fast page mode cycle time | t _{PC} | 40 | | ns | |
| /CAS precharge time (Fast page cycle) | t _{CP} | 10 | | ns | |
| /RAS pulse width (Fast page cycle) | t _{RASP} | 60 | 200K | ns | |
| /W to /RAS precharge time (C-B-R refresh) | t _{WRP} | 10 | | ns | |
| /W to /RAS hold time (C-B-R refresh) | t _{WRH} | 10 | | ns | |

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 /RAS-only or /CAS-before-/RAS refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{IH}/V_{IL} . $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 2 TTL loads and 100pF.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} is non-restrictive operating parameter. It is included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the /CAS leading edge in early write cycle.
10. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .