SONET/SDH/ATM MULTI-RATE 16 BIT TRANSCEIVER WITH CDR S3065

FEATURES

- CMOS 0.18 micron technology
- Complies with Bellcore and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
  - OC-48 (2488.32 Mbps)
  - OC-48 with FEC (2.67 Gbps)
  - OC-24 (1244.16 Mbps)
  - OC-24 with FEC (1.34 Gbps)
  - OC-12 (622.08 Mbps)
  - OC-12 with FEC (666.51 Mbps)
  - OC-3 (155.52 Mbps)
  - OC-3 with FEC (166.63 Mbps)
  - HDTV (1.485 Gbps)
  - D1 (1.38 Gbps)
  - Fibre Channel (1062 Mbps)
  - 2 x Fibre Channel (2.124 Gbps)
  - Gigabit Ethernet (1.25 Gbps)
  - DTV (143.18 Mbps)
- Reference frequency of 155.52 MHz
- Interface to LVPECL and LVTTL logic
- 16-bit differential LVPECL data path
- 324 FC-PBGA
- Diagnostic loopback mode
- Supports line timing
- Lock detect
- Signal detect input
- Low jitter LVPECL interface
- Internal FIFO to decouple transmit clocks
- Dual 1.8 V/ 3.3 V supply
- Typical power 1.25 Watts
- Available in die form

APPLICATIONS

- Wavelength Division Multiplexing (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

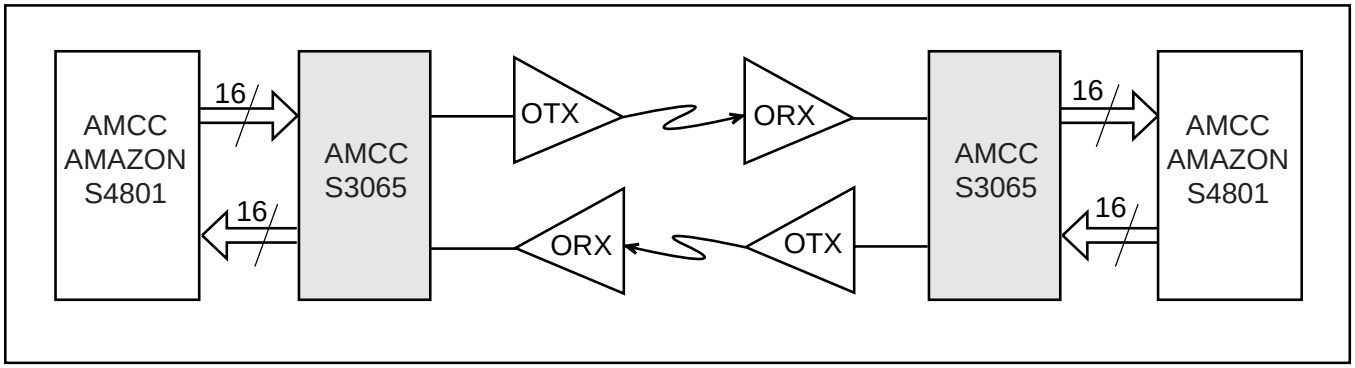
GENERAL DESCRIPTION

The S3065 SONET/SDH transceiver chip is a fully integrated serialization/deserialization multirate interface device. The S3065 receives a scrambled Non-Return to Zero (NRZ) signal and recovers the clock from the data. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency Phase-Locked Loop (PLL) on the S3065 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock (for SONET OC-48) in support of existing system clocking schemes.

The low jitter LVPECL interface is compliant with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3065 is packaged in a 324 FC-PBGA, offering designers a small package outline. The S3065 is also available in die form.

Figure 1. System Block Diagram



S3065 OVERVIEW

The S3065 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. The block diagram in Figure 2 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end. Table 1 shows the suggested interface devices for the S3065.

The S3065 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 16-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

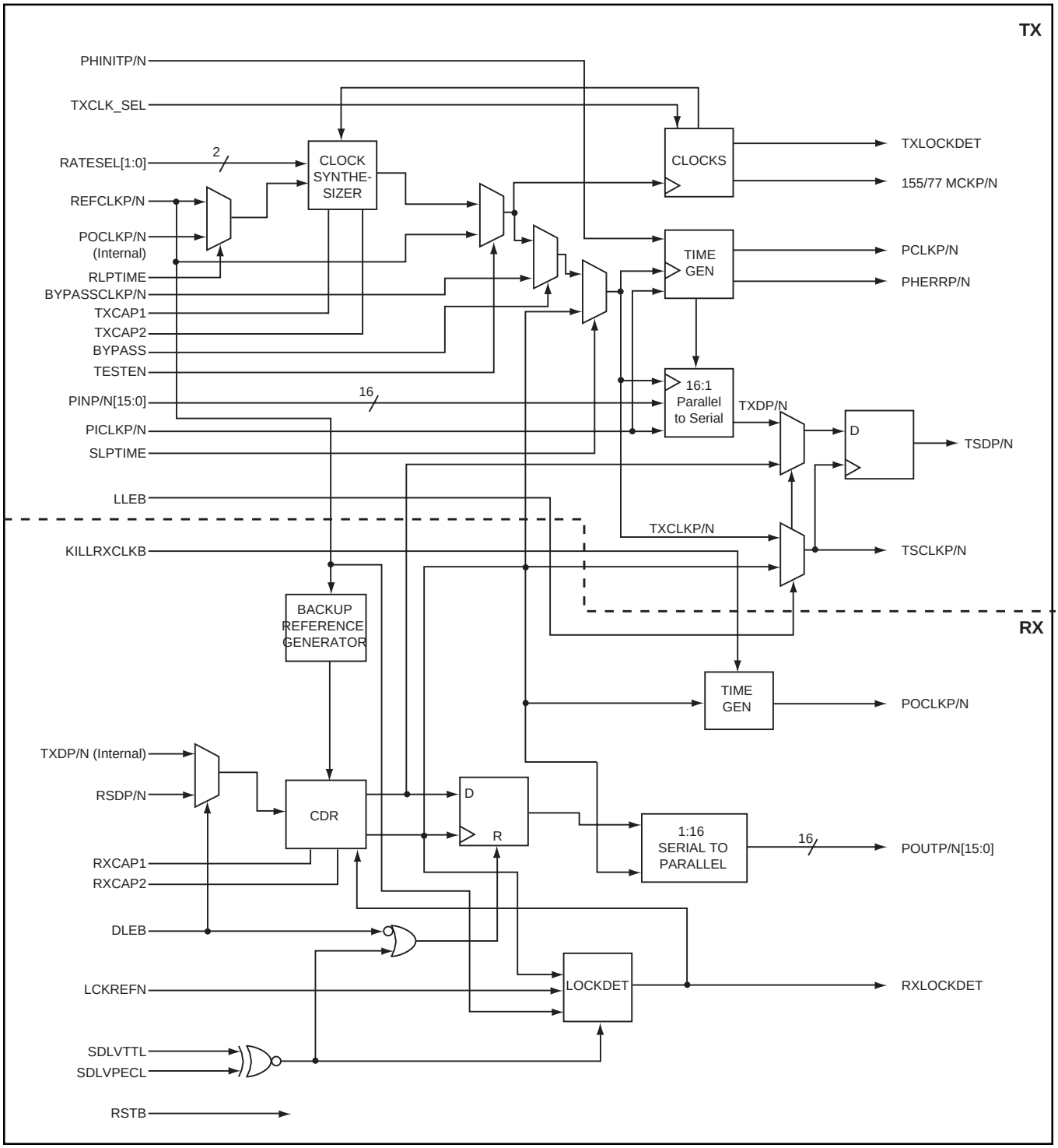
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. 16-bit parallel output

Internal clocking and control functions are transparent to the user.

Table 1. Sugggested Interface Devices

AMCC	S4801	STS-48C POS/ATM SONET Mapper
AMCC	S4802	SONET/SDH STS-48/STM-16 Framer/Pointer Processor
AMCC	S4804	STS-48 POS/ATM SONET Mapper
AMCC	S4805	SONET/SDH STS-48/STM-16 Framer/Pointer Processor
AMCC	S19201	STS-192 SONET/SDM Interleaver/Disinterleaver

Figure 2. S3065 Transceiver Functional Block Diagram



S3065 TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3065 transceiver chip performs the serialization stage in the processing of a transmit data stream. It converts 16-bit parallel data to bit serial format.

A high-frequency bit clock can be generated from a 155.52 MHz (for SONET rates) frequency reference by using an integral frequency synthesizer consisting of a Phase-Locked Loop (PLL) circuit with a divider in the loop.

Diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) is provided. See Other Operating Modes.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 2, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (REFCLKP/N).

The REFCLKP/N input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 10, the frequency spectrum in Figure 12. In order for the Transmit Serial Clock (TSCLK) frequency to have the same accuracy required for operation in a SONET system. The REFCLK must meet the phase noise requirements shown in Figure 12 to meet the jitter generation specifications given in Table 10. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the VCO output and the REFCLKP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Timing Generator

The timing generation function, seen in Figure 2, provides a divide-by-16 rate version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PINP/N[15:0] data from the FIFO to the serial shift register.

The PCLK output is a divide-by-16 rate version of the transmit serial clock. PCLK is intended for use as a divide-by-16 clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3065 device.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the REFCLK. The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the REFCLK.

Table 2. Reference Jitter Limits

Operating Mode	Band Width	RMS Jitter
STS-48	12 kHz to 20 MHz	-61 dBc
STS-24	12 kHz to 20 MHz	-61 dBc
STS-12	12 kHz to 20 MHz	-61 dBc
STS-3	12 kHz to 20 MHz	-61 dBc

Table 3. Rate Select and REFCLK Options

RATESEL0	RATESEL1	Mode	REFCLK
0	0	OC-3	155.52 MHz
0	1	OC-12	155.52 MHz
1	0	OC-24	155.52 MHz
1	1	OC-48	155.52 MHz
0	0	OC-3 with FEC	166.63 MHz
0	1	OC-12 with FEC	166.63 MHz
1	0	OC-24 with FEC	166.63 MHz
1	1	OC-48 with FEC	166.63 MHz
1	0	Fibre Channel	132.75 MHz
1	1	2 x Fibre Channel	132.75 MHz
1	0	HDTV	185.625 MHz
1	0	D1	172.5 MHz
1	0	Gigabit Ethernet	156.25 MHz
0	0	DTV	143.18 MHz

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 2 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PINP/N[15:0] bus on the rising edge of PICLK. The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide-by-16 clock, which is phase aligned to the transmit serial clock as described in the Timing Generator description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

FIFO

A FIFO is added to decouple the internal and external (PICLK) clocks. The internally generated divide-by-16 clock is used to clock out data from the FIFO. Phase Initialization (PHINIT) and Lock Detect (LOCKDET) are used to center or reset the FIFO. The PHINIT and LOCKDET signals will center the FIFO after the third PICLK pulse. This is in order to insure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK to PICLK delay can have a maximum drift as specified by Table 21.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKDET will go active and initialize the FIFO.
2. When RSTB goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held in reset when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During normal operation, the incoming data is passed from the PICLK timing domain to the internally generated divide-by-16 clock domain. Although the frequency of PICLK and the internally generated clock are the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, the phase error becomes active. When Phase Error (PHERR) conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs, up to ten bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete.

RECEIVER OPERATION

The S3065 transceiver chip provides the first stage of the digital processing of a receive bit-serial stream. It converts the bit-serial data stream into a 16-bit parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A line loopback (receiver to transmitter) is also provided.

Clock Recovery

The S3065 clock recovery device performs the clock recovery function for serial data links. The chip extracts the clock from the serial data inputs and provides retimed clock and data outputs. A 155.52 MHz reference clock (for SONET rates) is used for phase locked loop start up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference to the nominal bit rate.

The clock recovery generates a clock that is at the same frequency as the incoming data bit rate at the serial data input. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock.

Frequency stability without incoming data is guaranteed by an alternate reference input (REFCLK) that the PLL locks onto when data is lost. If the frequency of the incoming signal varies by a value greater than that stated in Table 10, with respect to REFCLKP/N, the PLL will be declared out of lock, and the PLL will lock to the reference clock. The assertion of LVTTL Signal Detect (SDLVTTL) or LVPECL Signal Detect (SDLVPECL) will also cause an out of lock condition.

The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET data signal.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for SONET equipment by the Bellcore TA-NWT-000253 standard, shown in Figure 3.

Lock Detect

The S3065 contains a lock detect circuit which monitors the integrity of the serial data inputs. If the received serial data fails the frequency test, the PLL will be forced to lock to the local reference clock. This will maintain the correct frequency of the recovered clock output under loss of signal or loss of lock conditions. If the recovered clock frequency deviates from the local reference clock frequency by a value greater than that stated in Table 10, the PLL will be declared out of lock. The lock detect circuit will poll the input data stream in an attempt to reacquire lock to data. If the recovered clock frequency is determined to be within the values stated in Table 10, the PLL will be declared in lock and the lock detect output will go active. When SDLVTTL XOR SDLVPECL = 0, it causes an out of lock condition.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of two 16-bit registers. The first is a serial-in, parallel-out shift register, which performs the serial-to-parallel conversion clocked by the clock recovery block. On the falling edge of the Parallel Output Clock (POCLK), the data in the parallel register is transferred to an output parallel register which drives POUTP/N[15:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data from the transmitter is routed to the serial-to-parallel block in place of the Receiver Serial Data (RSD). Transmit Serial Data/Transmit Serial Clock (TSD/TSCLK) outputs are active. DLEB takes precedence over SDLVPECL and SDLVTTL.

Line Loopback

The line loopback circuitry selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects the data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select the data and clock from the RSD and Receive Serial Clock (RSCLK) inputs, and a receive-to-transmit loopback can be established at the serial data rate.

Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3065 is bypassed, and the timing of the entire transmitter section is controlled by the Receive Serial Clock, RSCLKP/N. This mode is entered by setting the SLPTIME input to a TTL high level.

In this mode, the REFCLKP/N input is not used to generate TSCLKP/N. It should be carefully noted that the internal PLL and CDR PLL continue to operate in this mode, and continue as the source for the 155/77MCK and RSD/RSCLK, and if these signals are being used, the REFCLKP/N input must be properly driven.

In Reference Loop Timing (RLPTIME) mode, the Parallel Output Clock (POCLK) from the receiver is used as the reference clock to the transmitter. The 155/77MCK are generated from the POCLK in this operating mode.

CDR CHARACTERISTICS

Performance

The S3065 CDR PLL complies with the jitter specifications proposed for SONET/SDH equipment defined by the Bellcore Specifications: GR-253-CORE, Issue 2, December 1995 and ITU-T Recommendations: G.958 document, when used as specified.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. SONET input jitter tolerance requirements are shown in Figure 3.

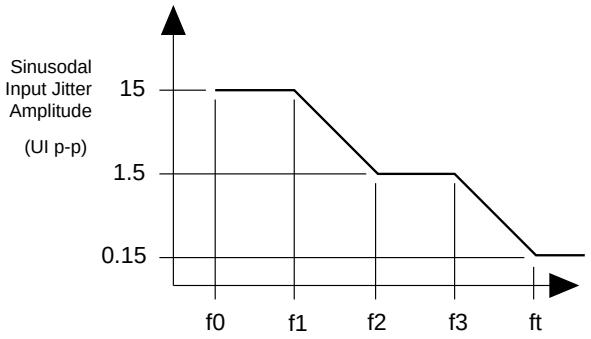
Jitter Transfer

The jitter transfer function is defined as the ratio of jitter on the output OC-N/STS-N signal to the jitter applied on the input OC-N/STS-N signal versus frequency. Jitter transfer requirements are shown in Figure 4. The measurement condition is that input sinusoidal jitter up to the mask level in Figure 3 be applied. The jitter transfer is only specified for the OC-48 rates. The S3065 does not meet the jitter transfer specification for the OC-12 and OC-3 rates.

Jitter Generation

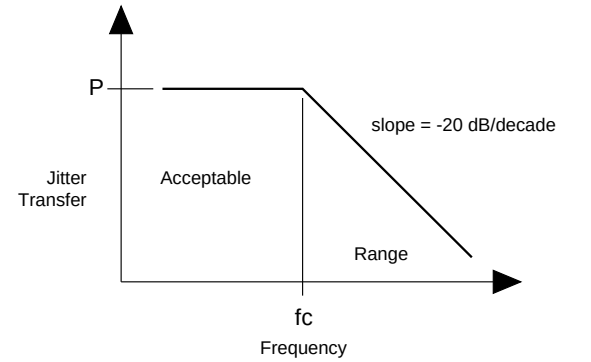
The jitter generation of the serial clock and serial data outputs shall not exceed the value specified in Table 10 when a serial data input with no jitter is presented to the serial data inputs. The REFCLK input must meet the phase noise requirements shown in Figure 12 to meet the jitter generation value specified in Table 10.

Figure 3. Input Jitter Tolerance Specification



OC/STS Level	f0 (Hz)	f1 (Hz)	f2 (Hz)	f3 (kHz)	ft (kHz)
48	10	600	6000	100	1000
24					
12	10	30	300	25	250
3	10	30	300	6.5	65

Figure 4. Jitter Transfer Specification



OC/STS Level[1,2]	fc (kHz)	P (dB)
48	2000	0.1

1. Bellcore Specifications: GR-253- CORE, Issue 2, December 1995.
2. ITU-T Recommendations: G.958.

FIBRE CHANNEL JITTER CHARACTERISTICS

Performance

The S3065 PLL complies with the jitter specifications proposed for Fibre Channel equipment defined by the fibre channel methodology for Jitter specification.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. Fibre Channel input jitter tolerance requirements are shown in Table 4.

Jitter Generation

The jitter of the serial clock and serial data outputs shall not exceed the value specified in Table 5 when a serial data input with no jitter is presented to the serial data inputs.

Table 4. Input Jitter Tolerance Specification at node α_R

Parameters	Description	Min	Max	Units
t_{FDJ}	Frequency Dependent Jitter Tolerance (637 kHz to ≥ 5 MHz)	0.10	–	UI p-p
t_{DJ}	Deterministic Jitter Tolerance (637 kHz – 531 MHz)	0.38	–	UI p-p
t_{RJ}	Random Jitter (637 kHz – 531 MHz)	0.22	–	UI p-p
t_{TJ}	Total Jitter	0.70	–	UI p-p

Table 5. Total Jitter Generation Specification at node α_T

Parameters	Description	Min	Max	Units
DJ	Deterministic Jitter		0.08	UI p-p
TJ	Total Jitter		0.23	UI p-p

Figure 5. Fibre Channel System Node Definition

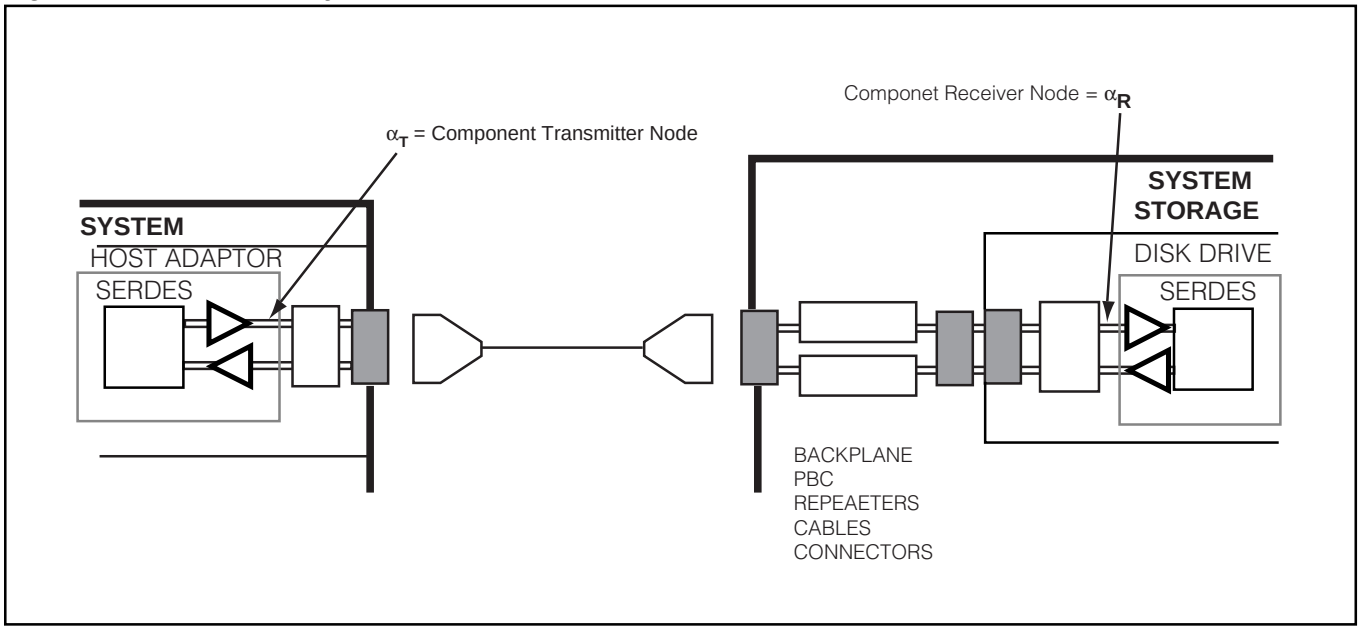


Table 6. S3065 Transmitter Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PINP0 PINN0 PINP1 PINN1 PINP2 PINN2 PINP3 PINN3 PINP4 PINN4 PINP5 PINN5 PINP6 PINN6 PINP7 PINN7 PINP8 PINN8 PINP9 PINN9 PINP10 PINN10 PINP11 PINN11 PINP12 PINN12 PINP13 PINN13 PINP14 PINN14 PINP15 PINN15	Internally Biased Diff. LVPECL	I	V12 U12 P13 N13 U13 T13 R14 P14 V14 U14 U15 T15 V16 U16 T18 T17 R17 R16 P18 P17 N17 N16 M15 M14 M18 M17 L17 L16 K18 K17 K15 K14	Parallel Input Data, aligned to the PICLK parallel input clock. PINP/N[15] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 16 of each PCM word, the last bit transmitted). PINP/N[15:0] is sampled on the rising edge of PICLK.
PICLKP PICLKN	Internally Biased Diff. LVPECL	I	R12 P12	Parallel Input Clock. A divide-by-16, nominally 50% duty cycle input clock, to which PINP/N[15:0] is aligned. PICLK is used to transfer the data on the PINP/N inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PINP/N[15:0].
TXCAP1 TXCAP2	Analog	I	E18 F18	Transmit Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 22.
PHINITP PHINITN	Internally Biased Diff. LVPECL	I	U11 T11	Phase Initialization. Rising edge will realign internal timing.
TXCLK_SEL	LVTTL	I	E12	Transmit Clock Select. Used to select between the 155.52 MHz and the 77.76 MHz clock (for SONET rates only) on the 155/77 MCKP/N output. A low on TXCLK_SEL selects 155.52 output clock, and a high on TXCLK_SEL selects 77.76 MHz output clock.

Table 6. S3065 Transmitter Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
TSDP TSDN	Diff. CML	O	A11 A10	Transmit Serial Data. Differential CML serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Diff. CML	O	A15 A14	Transmit Serial Clock that can be used to retime the TSD signal.
PCLKP PCLKN	Diff. LVPECL	O	V9 U9	Parallel Clock. A reference clock generated by dividing the internal bit clock by 16. It is normally used to coordinate 16-bit wide transfers between upstream logic and the S3065 device.
PHERRP PHERRN	Diff. LVPECL	O	T10 R10	Phase Error. Active high. Pulses high during each PCLK cycle for which there is a potential setup/hold timing violation between the internal byte clock and PICLK timing domains.
TXLOCKDET	LVTTL	O	H2	Transmit PLL Lock Detect. Goes High after the PLL has locked to the clock provided on the REFCLK pins. TXLOCKDET is an asynchronous output.

Table 7. S3065 Receiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Internally biased and terminated Diff. CML	I	A4 A5	Receive Serial Data stream signals normally connected to an optical receiver module.
SDLVPECL	Single Ended LVPECL	I	A7	LVPECL Signal Detect. LVPECL with internal pull-down. Active high when SDLVTTL is held at a logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Receive Serial Data In (RSDP/N) pins will be internally forced to a constant state (one or zero), and any transition on RSDP/N will be squelched. When SDLVPECL is active, data on the RSDP/N pins will be processed normally. When SDLVTTL is to be connected to the optical receiver module instead of SDLVPECL, then SDLVPECL should be tied high to implement an active low signal detect, or left unconnected to implement an active high signal detect.
SDLVTTL	LVTTL	I	B6	LVTTL Signal Detect. Active high when SDLVPECL is unconnected (logic 0). Active low when SDLVPECL is held at a logic 1. A single-ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant state (one or zero), and any transition on RSDP/N will be squelched. When SDLVTTL is active, data on the RSDP/N pins will be processed normally.
RXCAP1 RXCAP2	Analog	I	D1 E1	Receive Loop FIlter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 22.
LCKREFN	LVTTL	I	B7	Lock to Reference. Active low. When active, the serial clock output will be forced to lock to the local reference clock input [REFCLK].

Table 7. S3065 Receiver Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3 POUTP4 POUTN4 POUTP5 POUTN5 POUTP6 POUTN6 POUTP7 POUTN7 POUTP8 POUTN8 POUTP9 POUTN9 POUTP10 POUTN10 POUTP11 POUTN11 POUTP12 POUTN12 POUTP13 POUTN13 POUTP14 POUTN14 POUTP15 POUTN15	Diff. LVPECL	O	K1 K2 L2 L3 M1 M2 N2 N3 P1 P2 R2 R3 T1 T2 V3 U3 U4 T4 R5 P5 V5 U5 P6 N6 U6 T6 R7 P7 V7 U7 U8 T8	Parallel Data Output bus, aligned to the Parallel Output Clock (POCLK). POUTP/N[15] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUTP/N[0] is the least significant bit. POUTP/N[15:0] is updated on the falling edge of POCLK.
POCLKP POCLKN	Diff. LVPECL	O	P8 N8	Parallel Output Clock. A divide-by-16, nominally 50% duty cycle, parallel output clock that is aligned to POUTP/N[15:0] 16-bit parallel output data. POUTP/N[15:0] is updated on the falling edge of POCLK.
RXLOCKDET	LVTTL	O	H1	Receive PLL Lock Detect. Clock recovery indicator that is set high when the internal clock recovery has locked onto the incoming data stream. RXLOCKDET is an asynchronous output.

Table 8. S3065 Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	H18 H17	Reference Clock. Used as the reference for the internal bit clock frequency synthesizer. Internally biased.
DLEB	LVTTL	I	C8	Diagnostic Loopback Enable. Active low. Selects diagnostic loopback. When DLEB is inactive, the S3065 device uses the primary data (RSD) input. When active, the S3065 device uses the diagnostic loopback data from the transmitter. TSD/TSCLK is active in DLEB.
RATESEL0 RATESEL1	LVTTL	I	A2 B1	Selects the operating mode, see Table 3.
LLEB	LVTTL	I	C5	Line Loopback Enable. Active low. Selects line loopback. When LLEB is active, the S3065 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs.
KILLRXCLKB	LVTTL	I	D5	Kill Receive Clock Input. Active low. For normal operation, KILLRXCLKB is high. When this input is low, it will force the POCLK output to a logic "0" state.
SLPTIME	LVTTL	I	B8	Serial Clock Loop Time Select input. Active high. When active, SLPTIME enables the recovered clock from the receive section to be used in place of the synthesized transmit clock.
RLPTIME	LVTTL	I	A8	Reference Clock Loop Time Select input. Active high. When active, RLPTIME enables POCLK from the receiver to be used as the reference clock input to the transmitter.
RSTB	LVTTL	I	C9	Master Reset. Reset input for the device. Active low for a duration of 5 REFCLK cycles. During reset, all clocks are disabled.
TESTEN	LVTTL	I	C10	Test Enable. Used for production testing. Low for normal operation.
155/77MCKP 155/77MCKN	Diff. LVPECL	O	H3 H4	TSCLK/16 or TSCLK/32 clock output from the clock synthesizer.
BYPASSCLKP BYPASSCLKN	Internally biased and terminated Diff. CML	I	B18 C18	Bypass Clock. Provides an alternative serial clock bypassing the internal VCO.
BYPASS	LVTTL	I	C14	Active high. Selects between BYPASS clock and the VCO clock.

Table 8. S3065 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
AVSS	GND		C1, C2, C3, D2, D4, E2, E4, E17, F1, F2, G1, C15, D15, D17, D18, F15, F17, G14, G16, G17, G18, H16	Analog Ground (0 V).
VSS_RSD	GND		A3, B4, B3	RSD Ground (0 V).
VSS_TTL	GND		A1, B2	TTL Ground (0 V).
VSS_TSD	GND		B10, B11, B12	TSD Ground (0 V).
VSS_TSCLK	GND		B14, B15, B16	TSCLK Ground (0 V).
VSS_BYPASS	GND		B17, C17	BYPASS Ground (0 V).
VSS_LVPECL	GND		J1, L1, M4, N1, K4, N4, N9, P10, R1, R4, R6, R8, T3, T9, U2, V1, V4, V6, V8	LVPECL Ground (0 V).
VSS	GND		C6, C11, D7, D8, D14, E5, E8, H14, J14, V10	Ground (0 V).
VSS_RX	GND		F7, F8, F9, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9, K7, K8, K9, L7, L8, L9, M6	Receive Core Ground (0 V).
VSS_TX	GND		F10, F11, F12, G10,G11, G12, H10, H11, H12, J10, J11, J12, K10, K11, K12, L10, L11, L12, M11	Transmit Core Ground (0 V).
VSS_REF	GND		J17	Reference clock Ground (0 V).
VSS_CMOS	GND		K16, L15, L18, M13, N12, N18, P11, P15, P16, R18, T12, T14, T16, U17, V11, V13, V15, V18	CMOS Ground (0 V).
VDD_3V	3.3 V		C7, D6, D10, E6, E7, M16, N14, R11, R15, U18	Power Supply.
VDD_TTL	3.3 V		E14, F14	TTL Power Supply
VDD_LVPECL	3.3 V		K3, L4, M3, M8, N5, N7, N10, P3, P4, P9, R9, T5, T7, U1, U10, V2	LVPECL Power Supply.

Table 8. S3065 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
AVDD_RX	1.8 V		C4, D3, E3, F3, F4, G2, G3, G4	Receive Analog Power Supply.
VDD_RSD	1.8 V		A6, B5	RSD Power Supply.
VDD_RX_ CORE	1.8 V		E9, F5, F6, G5, G6, H5, J5, K6, L5, L6, M5, M7, M9	Receive Core Power Supply.
VDD_TSD	1.8 V		A9, B9, A12	TSD Power Supply.
VDD_TX_ CORE	1.8 V		E13, F13, G13, H13, J13, K13, L13, M12, M10, E10, E11	Transmit Core Power Supply.
VDD_1V	1.8 V		N11, R13, L14, V17, N15 D9, D11	Power Supply.
VDD_TSCLK	1.8 V		A13, B13, A16	TSCLK Power Supply.
VDD_1V_REF	1.8 V		J16	Reference Clock Power Supply.
AVDD_TX	1.8 V		C16, D16, E15, E16, F16, G15, H15, J15	Transmit Analog Power Supply.
VDD_BYPASS	1.8 V		A17, A18	Bypass Power Supply.
VDD_3V_REF	3.3 V		J18	Reference Clock Power Supply.
NC			J4, D12, D13, J2, J3, C12, C13, K5	No Connect. Do not connect these pins to power or ground.

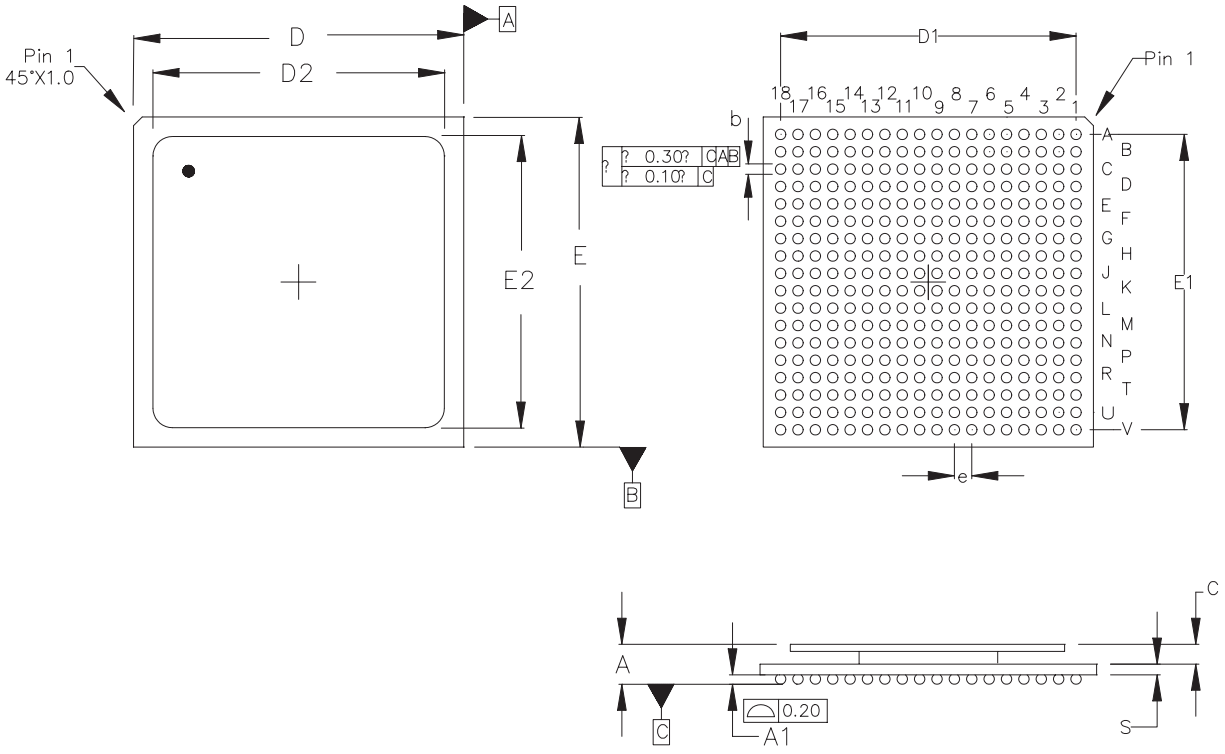
Figure 6. S3065 Pinout BottomView

	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	VDD_ BYPASS	VDD_ BYPASS	VDD_TSCLK	TSCLKP	TSCLKN	VDD_TSCLK	VDD_TSD	TSDP	TSDN	VDD_TSD	RLPTIME	SDLVPECL	VDD_RSD	RSDN	RSDP	VSS_RSD	RATESEL0	VSS_TTL
B	BYPASSCLKP	VSS_BYPASS	VSS_TSCLK	VSS_TSCLK	VSS_TSCLK	VDD_TSCLK	VSS_TSD	VSS_TSD	VSS_TSD	VDD_TSD	SLPTIME	LCKREFN	SDLVTTL	VDD_RSD	VSS_RSD	VSS_RSD	VSS_TTL	RATESEL1
C	BYPASSCLKN	VSS_BYPASS	AVDD_TX	AVSS	BYPASS	NC	NC	VSS	TESTEN	RSTB	DLEB	VDD_3V	VSS	LLEB	AVDD_RX	AVSS	AVSS	AVSS
D	AVSS	AVSS	AVDD_TX	AVSS	VSS	NC	NC	VDD_1V	VDD_3V	VDD_1V	VSS	VSS	VDD_3V	KILLRXCLKB	AVSS	AVDD_RX	AVSS	RXCAP1
E	TXCAP1	AVSS	AVDD_TX	AVDD_TX	VDD_TLL	VDD_TX_ CORE	TXCLK_SEL	VDD_TX_ CORE	VDD_TX_ CORE	VDD_RX_ CORE	VSS	VDD_3V	VDD_3V	VSS	AVSS	AVDD_RX	AVSS	RXCAP2
F	TXCAP2	AVSS	AVDD_TX	AVSS	VDD_TLL	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	VDD_RX_ CORE	AVDD_RX	AVDD_RX	AVSS	AVSS
G	AVSS	AVSS	AVSS	AVDD_TX	AVSS	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	VDD_RX_ CORE	AVDD_RX	AVDD_RX	AVDD_RX	AVSS
H	REFCLKP	REFCLKN	AVSS	AVDD_TX	VSS	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	155/77MCKN	155/77MCKP	TXLOCKDET	RXLOCKDET
J	VDD_3V_REF	VSS_REF	VDD_1V_REF	AVDD_TX	VSS	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	NC	NC	NC	VSS_LVPECL
K	PINP14	PINN14	VSS_CMOS	PINP15	PINN15	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	NC	VSS_LVPECL	VDD_LVPECL	POUTN0	POUTP0
L	VSS_CMOS	PINP13	PINN13	VSS_CMOS	VDD_1V	VDD_TX_ CORE	VSS_TX	VSS_TX	VSS_TX	VSS_RX	VSS_RX	VSS_RX	VDD_RX_ CORE	VDD_RX_ CORE	VDD_LVPECL	POUTN1	POUTP1	VSS_LVPECL
M	PINP12	PINN12	VDD_3V	PINP11	PINN11	VSS_CMOS	VDD_TX_ CORE	VSS_TX	VDD_TX_ CORE	VDD_RX_ CORE	VDD_LVPECL	VDD_RX_CO-RE	VSS_RX	VDD_RX_ CORE	VSS_LVPECL	VDD_LVPECL	POUTN2	POUTP2
N	VSS_CMOS	PINP10	PINN10	VDD_1V	VDD_3V	PINN1	VSS_CMOS	VDD_1V	VDD_LVPECL	VSS-LVPECL	POCLKN	VDD_LVPECL	POUTN11	VDD_LVPECL	VSS_LVPECL	POUTN3	POUTP3	VSS_LVPECL
P	PINP9	PINN9	VSS_CMOS	VSS_CMOS	PINN3	PINP1	PICLKN	VSS_CMOS	VSS_LVPECL	VDD_LVPECL	POCLKP	POUTN13	POUTP11	POUTN9	VDD_LVPECL	VDD_LVPECL	POUTN4	POUTP4
R	VSS_CMOS	PINP8	PINN8	VDD_3V	PINP3	VDD-1V	PICLKP	VDD_3V	PHERRN	VDD-LVPECL	VSS_LVPECL	POUTP13	VSS_LVPECL	POUTP9	VSS_LVPECL	POUTN5	POUTP5	VSS_LVPECL
T	PINP7	PINN7	VSS_CMOS	PINN5	VSS_CMOS	PINN2	VSS_CMOS	PHINITN	PHERRP	VSS-LVPECL	POUTN15	VDD_LVPECL	POUTN12	VDD_LVPECL	POUTN8	VSS_LVPECL	POUTN6	POUTP6
U	VDD_3V	VSS_CMOS	PINN6	PINP5	PINN4	PINP2	PINN0	PHINITP	VDD_LVPECL	PCLKN	POUTP15	POUTN14	POUTP12	POUTN10	POUTP8	POUTN7	VSS_LVPECL	VDD_LVPECL
V	VSS_CMOS	VDD_1V	PINP6	VSS_CMOS	PINP4	VSS_CMOS	PINP0	VSS_CMOS	VSS	PCLKP	VSS_LVPECL	POUTP14	VSS_LVPECL	POUTP10	VSS_LVPECL	POUTP7	VDD-LVPECL	VSS_LVPECL

Figure 7. S3065 Pinout Top View

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
A	VSS_TTL	RATESEL0	VSS_RSD	RSDP	RSDN	VDD_RSD	SDLVPECL	RLPTIME	VDD_TSD	TSDN	TSDP	VDD_TSD	VDD_TSCLK	TSCLKN	TSCLKP	VDD_TSCLK	VDD_ BYPASS	VDD_ BYPASS
B	RATESEL1	VSS_TTL	VSS_RSD	VSS_RSD	VDD_RSD	SDLVTTL	LCKREFN	SLPTIME	VDD_TSD	VSS_TSD	VSS_TSD	VSS_TSD	VDD_TSCLK	VSS_TSCLK	VSS_TSCLK	VSS_TSCLK	VSS_BYPASS	BYPASSCLKP
C	AVSS	AVSS	AVSS	AVDD_RX	LLEB	VSS	VDD_3V	DLEB	RSTB	TESTEN	VSS	NC	NC	BYPASS	AVSS	AVDD_TX	VSS_BYPASS	BYPASSCLKN
D	RXCAP1	AVSS	AVDD_RX	AVSS	KILLRXCLKB	VDD_3V	VSS	VSS	VDD_1V	VDD_3V	VDD_1V	NC	NC	VSS	AVSS	AVDD_TX	AVSS	AVSS
E	RXCAP2	AVSS	AVDD_RX	AVSS	VSS	VDD_3V	VDD_3V	VSS	VDD_RX_ CORE	VDD_TX_ CORE	VDD_TX_ CORE	TXCLK_SEL	VDD_TX_ CORE	VDD_TTL	AVDD_TX	AVDD_TX	AVSS	TXCAP1
F	AVSS	AVSS	AVDD_RX	AVDD_RX	VDD_RX_ CORE	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	VDD_TTL	AVSS	AVDD_TX	AVSS	TXCAP2
G	AVSS	AVDD_RX	AVDD_RX	AVDD_RX	VDD_RX_ CORE	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	AVSS	AVDD_TX	AVSS	AVSS	AVSS
H	RXLOCKDET	TXLOCKDET	155/77MCKP	155/77MCKN	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	VSS	AVDD_TX	AVSS	REFCLKN	REFCLKP
J	VSS_LVPECL	NC	NC	NC	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	VSS	AVDD_TX	VDD_1V_REF	VSS_REF	VDD_3V_REF
K	POUTP0	POUTN0	VDD_LVPECL	VSS_LVPECL	NC	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	PINN15	PINP15	VSS_CMOS	PINN14	PINP14
L	VSS_LVPECL	POUTP1	POUTN1	VDD_LVPECL	VDD_RX_ CORE	VDD_RX_ CORE	VSS_RX	VSS_RX	VSS_RX	VSS_TX	VSS_TX	VSS_TX	VDD_TX_ CORE	VDD_1V	VSS_CMOS	PINN13	PINP13	VSS_CMOS
M	POUTP2	POUTN2	VDD_LVPECL	VSS_LVPECL	VDD_RX_ CORE	VSS_RX	VDD_RX_CO- RE	VDD_LVPECL	VDD_RX_ CORE	VDD_TX_ CORE	VSS_TX	VDD_TX_ CORE	VSS_CMOS	PINN11	PINP11	VDD_3V	PINN12	PINP12
N	VSS_LVPECL	POUTP3	POUTN3	VSS_LVPECL	VDD_LVPECL	POUTN11	VDD_LVPECL	POCLKN	VSS-LVPECL	VDD_LVPECL	VDD_1V	VSS_CMOS	PINN1	VDD_3V	VDD_1V	PINN10	PINP10	VSS_CMOS
P	POUTP4	POUTN4	VDD_LVPECL	VDD_LVPECL	POUTN9	POUTP11	POUTN13	POCLKP	VDD_LVPECL	VSS_LVPECL	VSS_CMOS	PICLKN	PINP1	PINN3	VSS_CMOS	VSS_CMOS	PINN9	PINP9
R	VSS_LVPECL	POUTP5	POUTN5	VSS_LVPECL	POUTP9	VSS_LVPECL	POUTP13	VSS_LVPECL	VDD-LVPECL	PHERRN	VDD_3V	PICLKP	VDD-1V	PINP3	VDD_3V	PINN8	PINP8	VSS_CMOS
T	POUTP6	POUTN6	VSS_LVPECL	POUTN8	VDD_LVPECL	POUTN12	VDD_LVPECL	POUTN15	VSS-LVPECL	PHERRP	PHINITN	VSS_CMOS	PINN2	VSS_CMOS	PINN5	VSS_CMOS	PINN7	PINP7
U	VDD_LVPECL	VSS_LVPECL	POUTN7	POUTP8	POUTN10	POUTP12	POUTN14	POUTP15	PCLKN	VDD_LVPECL	PHINITP	PINN0	PINP2	PINN4	PINP5	PINN6	VSS_CMOS	VDD_3V
V	VSS_LVPECL	VDD-LVPECL	POUTP7	VSS_LVPECL	POUTP10	VSS_LVPECL	POUTP14	VSS_LVPECL	PCLKP	VSS	VSS_CMOS	PINP0	VSS_CMOS	PINP4	VSS_CMOS	PINP6	VDD_1V	VSS_CMOS

Figure 8. Package Drawing 324 PBGA



DIMENSIONS (are in millimeters)

UNIT	A_1	S	C	A	E	E_1	E_2	D	D_1	D_2	b	e
MIN	0.40	0.87	1.22		18.80	16.90	16.80	18.80	16.90	16.80	0.50	1.00 BASIC
NOM	0.50	0.95	1.42		19.00	17.00	17.00	19.00	17.00	17.00	0.60	
MAX	0.60	1.03	1.62	2.97	19.20	17.10	17.20	19.20	17.10	17.20	0.70	

Table 9. Thermal Management

Device	Max Package Power	Θja (Still Air)	Θjc
S3065	1.9 W	27.4˚ C/W	1.9˚ C/W

Note: The S3065 requires an airflow of 300 LFMP for industrial operating range of 85°C/W.

Table 10. Performance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Nominal VCO Center Frequency CSU and CDR	2.0	2.488	3.0	GHz	
Jitter Generation (CSU) OC-48 OC-12 OC-3			 0.007 0.005 0.005	UI (rms)	Note: Output jitter measured at SONET operating rate using appropriate filter, rms jitter, in lock.
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 is required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise and Fall Times			1.5	ns	10% to 90% of amplitude.
Acquisition Time (CDR) 155.52 MHz REFCLK			500	µsec	Minimum transition density of 20%. Guaranteed but not tested. With device already powered up and valid ref. clk.
Frequency difference at which the PLL goes out of lock (REFCLK compared to the divided down VCO clock)–CDR	450	600	770	ppm	Guaranteed but not tested.
Frequency difference at which the receive PLL goes into lock (REFCLK compared to the divided down VCO clock) - CDR	220	300	390	ppm	Guaranteed but not tested.
Jitter Generation (CDR) with VCO locked to SERDATIP/N			0.01	UI (rms)	Note: This mode is valid in the SLPTIME, RLPTIME, and LLEB mode only.
REFCLK to PCLK Delay	0		6.43	ns	Guaranteed but not tested.
RSTB to TXLOCKDET Delay			500	µs	Guaranteed but not tested.
Bit Latency - Number of clock cycles after PINP/N[X] appears at TSDP/N			20	REFCLK Cycles	Guaranteed but not tested.

Table 11. SONET Jitter Tolerance Specifications

Parameter	Min	Typ	Max	Units	Conditions
Jitter Tolerance STS-48	0.4	0.5		UI	1 MHz < f < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-24					
Jitter Tolerance STS-12	0.4	0.6		UI	250 kHz < f < 5 MHz Data Pattern = 2^7-1 PRBS
Jitter Tolerance STS-3	0.4	0.8		UI	65 kHz < f < 1 MHz Data Pattern = 2^7-1 PRBS

Table 12. Gigabit Ethernet Jitter Specifications

Parameter	Min	Typ	Max	Units	Conditions
t_J Total Input Jitter Tolerance	599			ps	As specified in IEEE 802.3z.
t_{DJ} Deterministic Input Jitter Tolerance	370			ps	As specified in IEEE 802.3z.

Table 13. Absolute Maximum Ratings

The following are the absolute maximum stress ratings for S3065 device. Stresses beyond those listed may cause permanent damage to the device. Absolute maximum ratings are stress ratings only and operation of the device at the maximums stated or any other conditions beyond those indicated in the “Recomended Operating Conditions” of the document are not inferred.

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	°C
Voltage on 3.3 Volts Power pins with respect to GND	-0.5		+3.6	V
Voltage on 1.8 Volts Power pins with respect to GND	-0.2		+1.98	V
Voltage on any LVPECL Input Pin	0		VDD_LVPECL	V

ESD Ratings

The S3065 is rated to the following voltages based on the human body model:

1. All pins are rated at 500 volts except TXCAP1, TXCAP2 and TSDP. TXCAP1, TXCAP2 and TSDP are rated at 100 volts.

Table 14. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias[1]	0		70	°C
Voltage on 1.8 Volts Power Planes with respect to GND	1.71	1.8	1.89	V
Voltage on 3.3 Volts Power Planes with respect to GND	3.135	3.3	3.465	V
Voltage on any LVPECL Input Pin	0		VDD_LVPECL	V
Voltage on any LVTTL Input Pin	0		VDD_TTL	V
1.8 Volts Supply Current[2]			620	mA
3.3 Volts Supply Current[2]			150	mA

1. 300 LFPM airflow is required for industrial temperature range of 85 °C.
2. Outputs unloaded.

Table 15. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0		VDD_TTL	V	VDD_TTL = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	VDD_TTL = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.4			V	V_{CC} = min I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{CC} = min I_{OL} = 1 mA

Table 16. Internally Biased Differential LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	LVPECL Input Low	VDD_LVPECL -2.0		VDD_LVPECL -1.4	V	Funtional Test Only.
V_{IH}	LVPECL Input High	VDD_LVPECL -1.25		VDD_LVPECL -0.55	V	Funtional Test Only.
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	200		1200	mV	See Figure 13.
ΔV_{INDIFF}	Diff. Input Voltage Swing	400		2400	mV	See Figure 13.

Table 17. Differential LVPECL Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	500		900	mV	270 Ω to GND. 100 Ω Line to Line. See Figure 13.
$\Delta V_{OUTDIFF}$	Diff. Output Voltage Swing	1000		1800	mV	270 Ω to GND. 100 Ω Line to Line. See Figure 13.
V_{OH}	Output High Voltage	VDD_ LVPECL -1.09		VDD_ LVPECL -0.83	V	270 Ω to GND. 100 Ω Line to Line.
V_{OL}	Output Low Voltage	VDD_ LVPECL -1.93		VDD_ LVPECL -1.44	V	270 Ω to GND. 100 Ω Line to Line.

Table 18. Single-Ended LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	VDD_LVPECL -2.0		VDD_LVPECL -1.4	V	
V_{IH}	PECL Input High Voltage	VDD_LVPECL -1.25		VDD_LVPECL -0.55	V	

Table 19. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{OH} (CLOCK)	CML Output High Voltage.	VDD_TSCLK -0.45		VDD_TSCLK -0.25	V	
V_{OL} (CLOCK)	CML Output Low Voltage.	VDD_TSCLK -1.15		VDD_TSCLK -0.73	V	
$\Delta V_{OUTDIFF}$ (CLOCK)	CML Serial Output Differential Voltage Swing	800		1400	mV	100 Ω line-to-line. See Figure 13.
$\Delta V_{OUTSINGLE}$ (CLOCK)	CML Serial Output Single-Ended Voltage Swing	400		700	mV	100 Ω line-to-line. See Figure 13.
V_{OH} (DATA)	CML Output High Voltage.	VDD_TSD -0.45		VDD_TSD -0.25	V	
V_{OL} (DATA)	CML Output Low Voltage.	VDD_TSD -1.15		VDD_TSD -0.73	V	
$\Delta V_{OUTDIFF}$ (DATA)	CML Serial Output Differential Voltage Swing	800		1400	mV	
$\Delta V_{OUTSINGLE}$ (DATA)	CML Serial Output Single-Ended Voltage Swing	400		700	mV	

Table 20. CML Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
ΔV_{INDIFF}	Differential Input Voltage Swing	300		1600	mV	See Figure 13.
$\Delta V_{INSINGLE}$	Single-Ended Input Voltage Swing	150		800	mV	See Figure 13.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 21. Transmitter AC Timing Characteristics

Parameter	Description	Min	Max	Units
	TSCLK Frequency	2.0	3.0	GHz
	TSCLK Duty Cycle	45	55	%
	TSCLK Duty Cycle Distortion w.r.t. RSCLK (internal) or BYPASSCLK (In SLPTIME, LLEB or BYPASS modes)		5.0	%
	PICLK Duty Cycle	35	65	%
tS_{PIN}	PINP/N[15:0] Setup Time w.r.t. PICLK	1.5		ns
tH_{PIN}	PINP/N[15:0] Hold Time w.r.t. PICLK	0.75		ns
tS_{TSD}	TSD Setup Time w.r.t. TSCLK Rising	120		ps
tH_{TSD}	TSD Hold Time w.r.t. TSCLK Rising	100		ps
	PCLK to PICLK drift after FIFO is centered		5.2	ns
	PCLK Duty Cycle	45	55	%
	TSCLK Rise and Fall Time		120	ps
	TSD Rise and Fall Time		150	ps

Figure 9. Transmitter Input Timing[1]

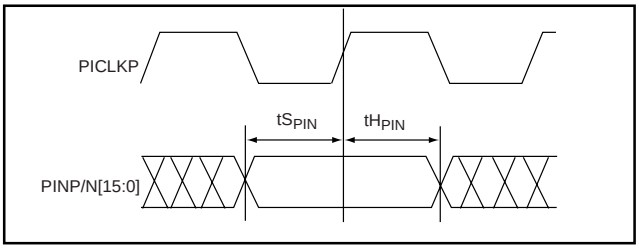
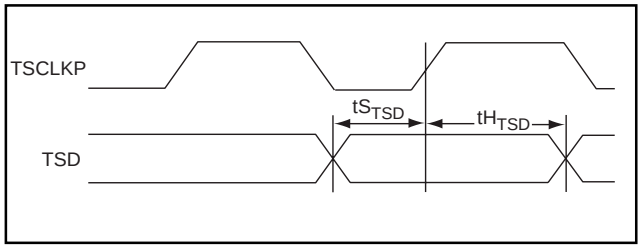


Figure 10. Transmitter Output Timing[1]

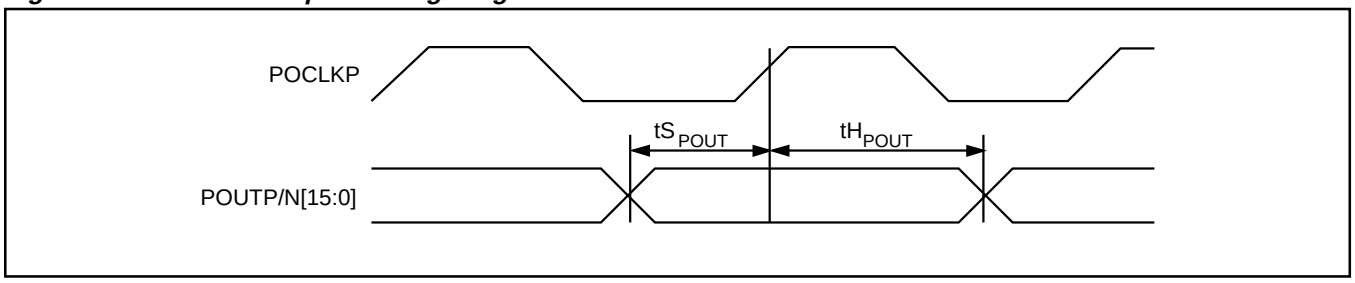


Notes on Timing:
1. Timing is measured from the crossover point of the clock to the crossover point of the data.

Table 22. AC Receiver Timing Characteristics

Parameter	Description	Min	Max	Units
	POCLK Duty Cycle	45	55	%
tS_{POUT}	POUTP/N[15:0] Setup Time w.r.t. POCLK	2.25		ns
tH_{POUT}	POUTP/N[15:0] Hold Time w.r.t. POCLK	2		ns

Figure 11. Receiver Output Timing Diagram[1]



Notes on Timing:

1. Timing is measured from the crossover point of the clock to the crossover point of the data.

Figure 12. S3065 155.52 MHz REFCLK Phase Noise Limit (for SONET rates)

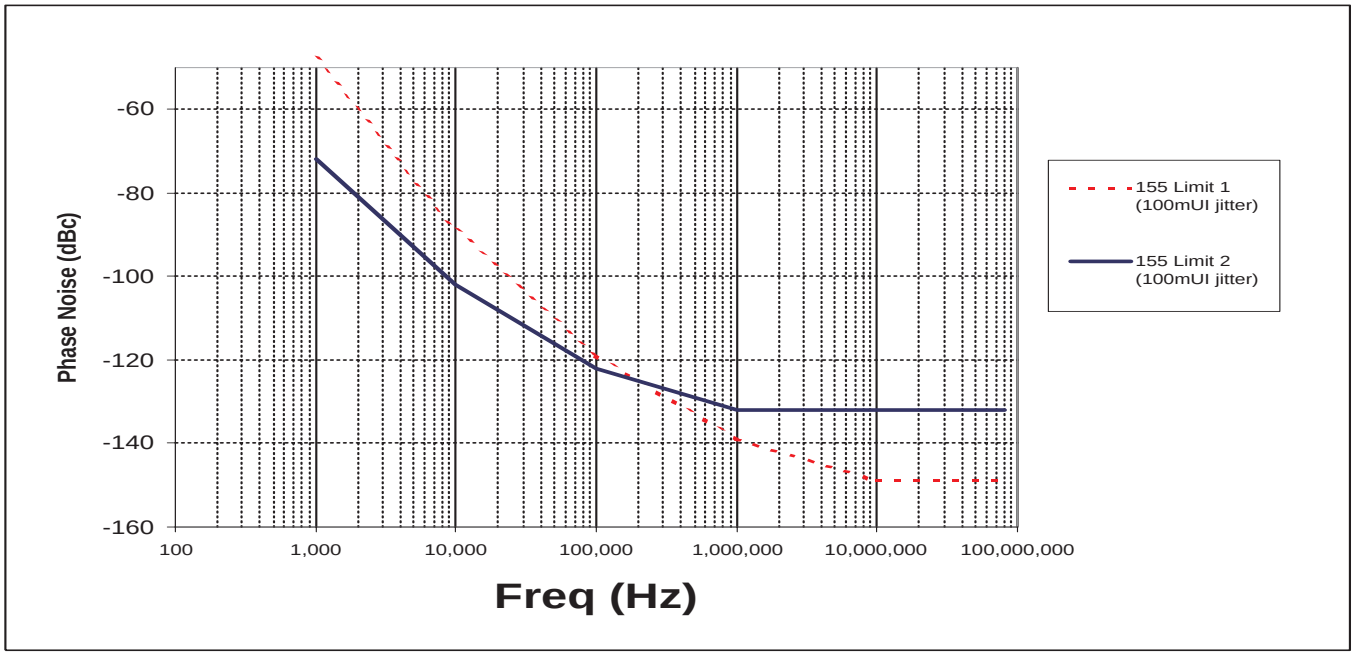
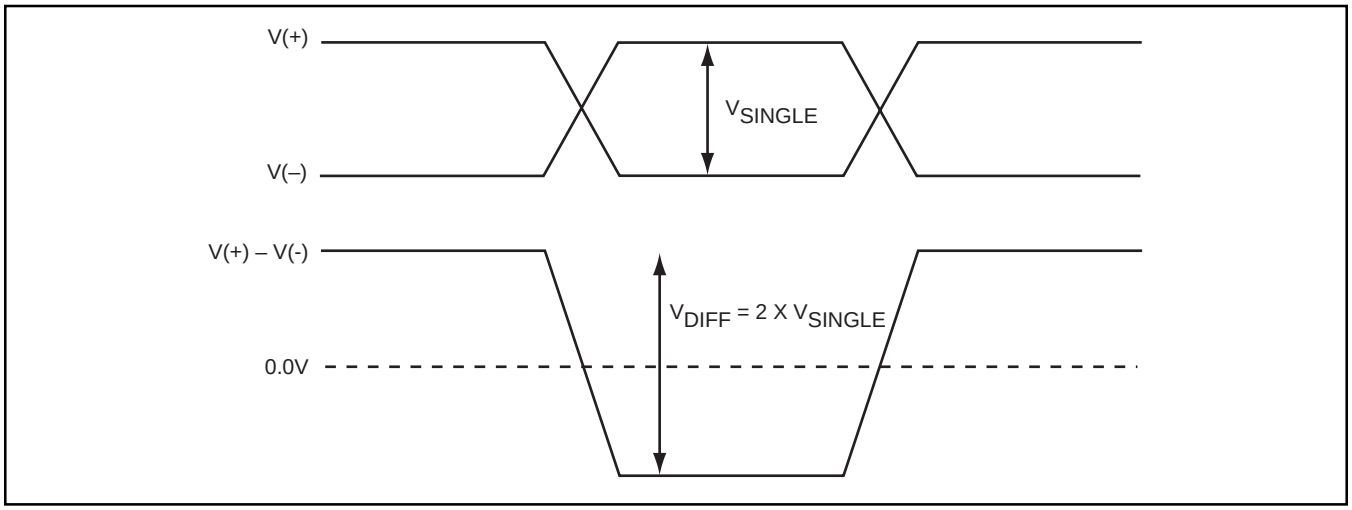
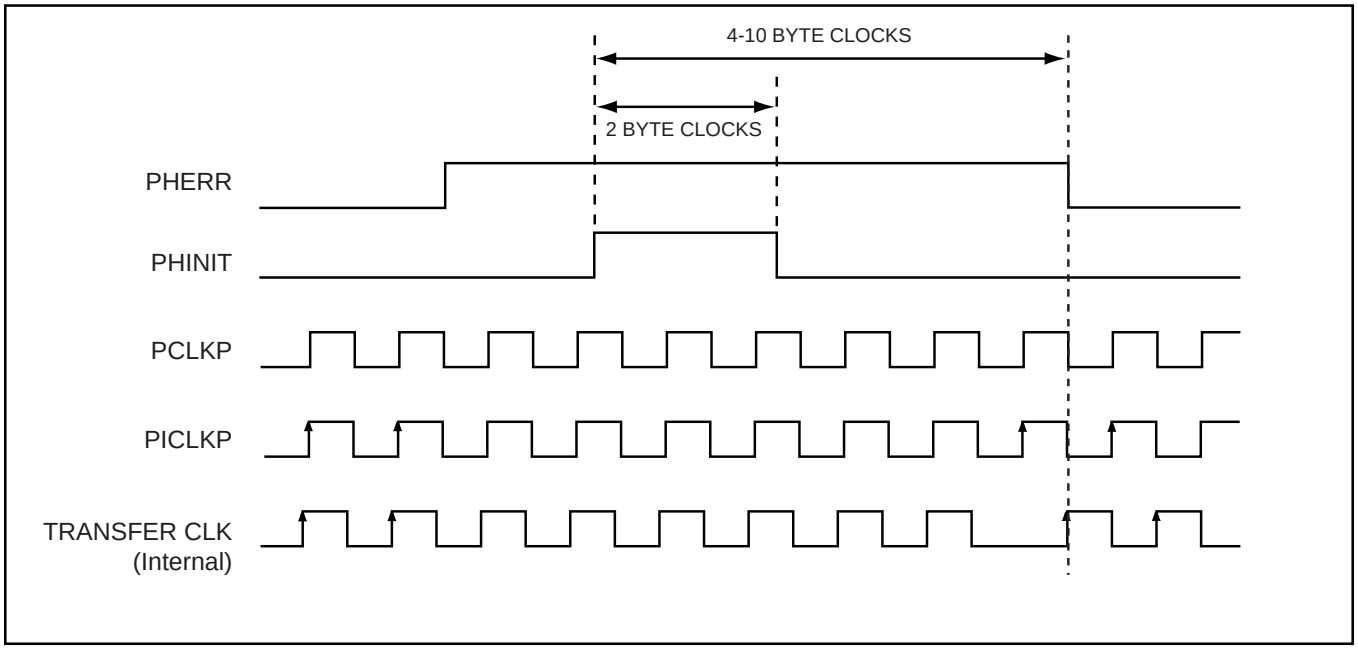


Figure 13. Differential Voltage Measurement



Note: V(+) – V(-) is the algebraic difference of the input signals.

Figure 14. Phase Adjust Timing[1]



1. The byte clock = 155.52 MHz (for OC-48 SONET rate).

Figure 15. Differential CML Output to +5V/+3.3V PECL Input AC Coupled Termination

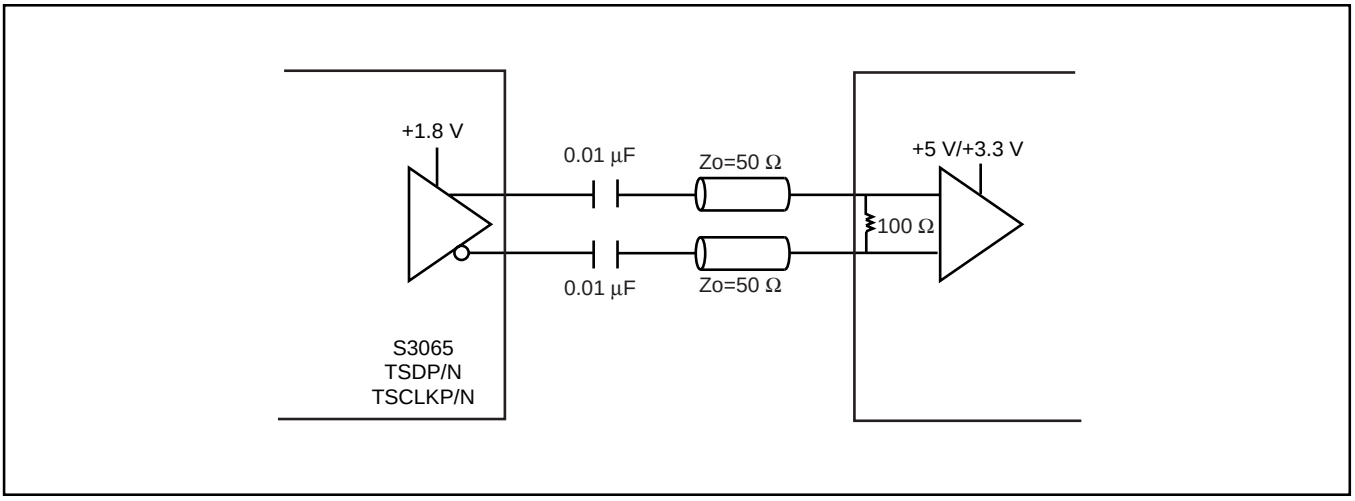


Figure 16. Differential LVPECL Driver to LVPECL Input Termination

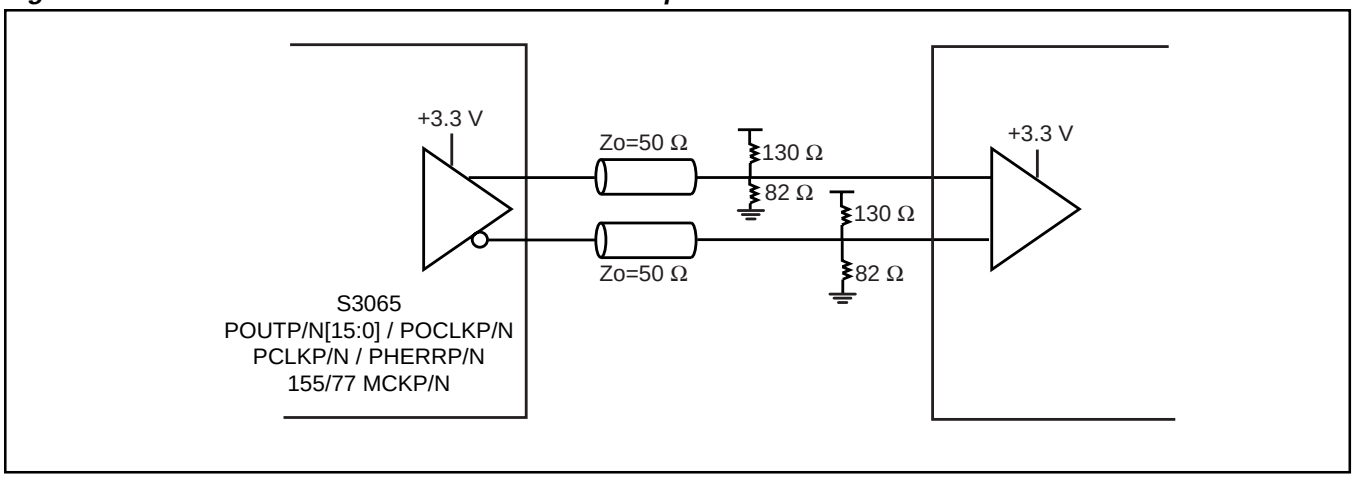


Figure 17. Differential LVPECL Driver to Differential LVPECL Input Termination

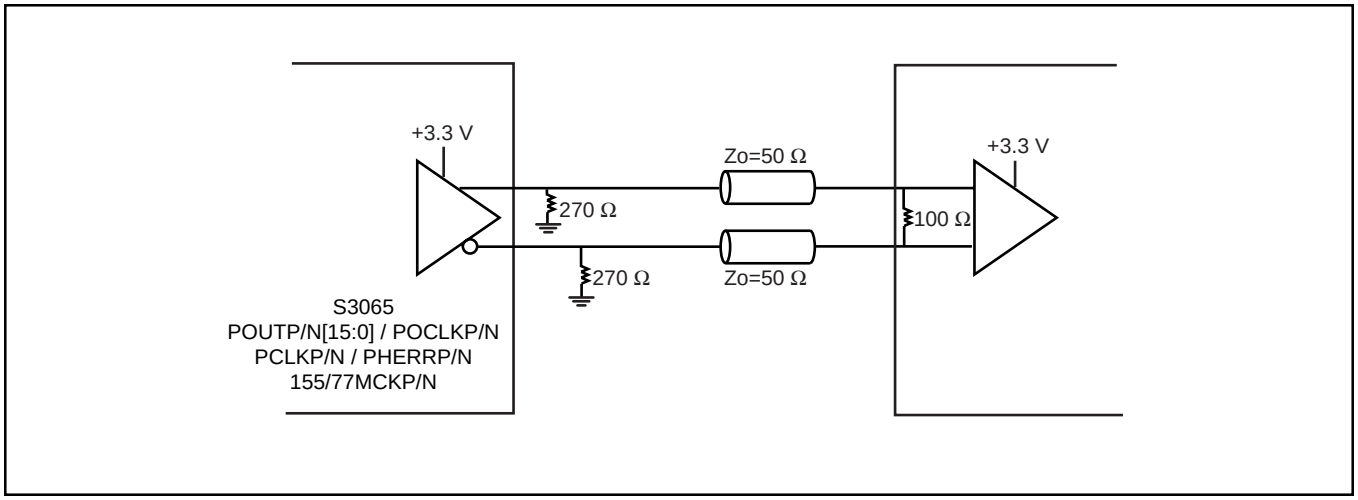


Figure 18. +5V Differential PECL Driver to S3065 Differential CML Input AC Coupled Termination

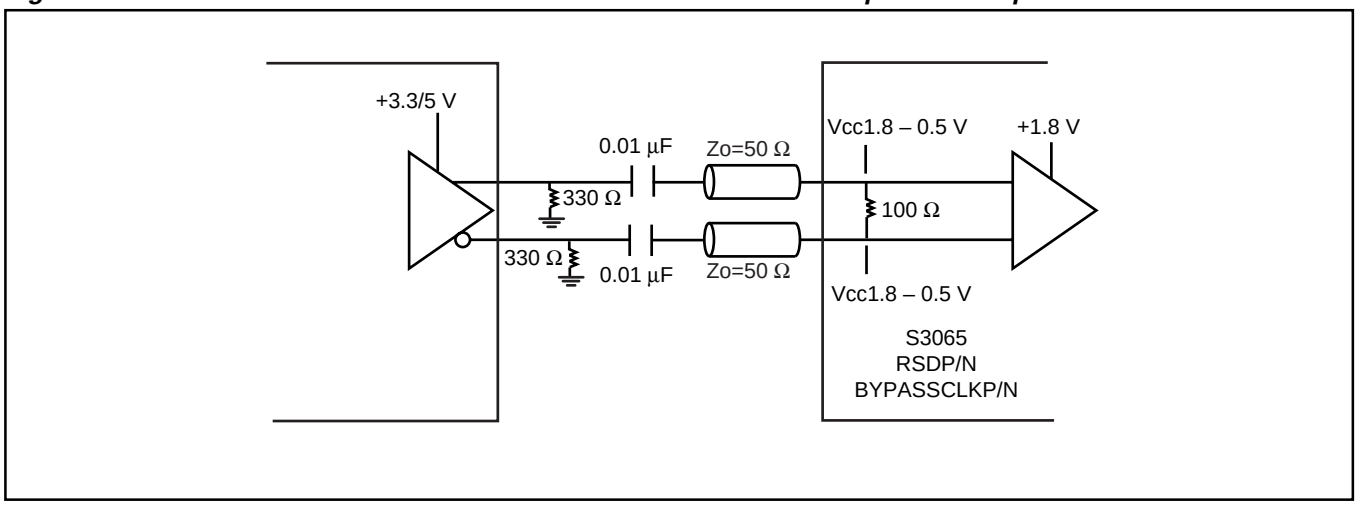


Figure 19. +5V Differential PECL Driver to S3065 Differential LVPECL Reference Clock Input AC Coupled Termination

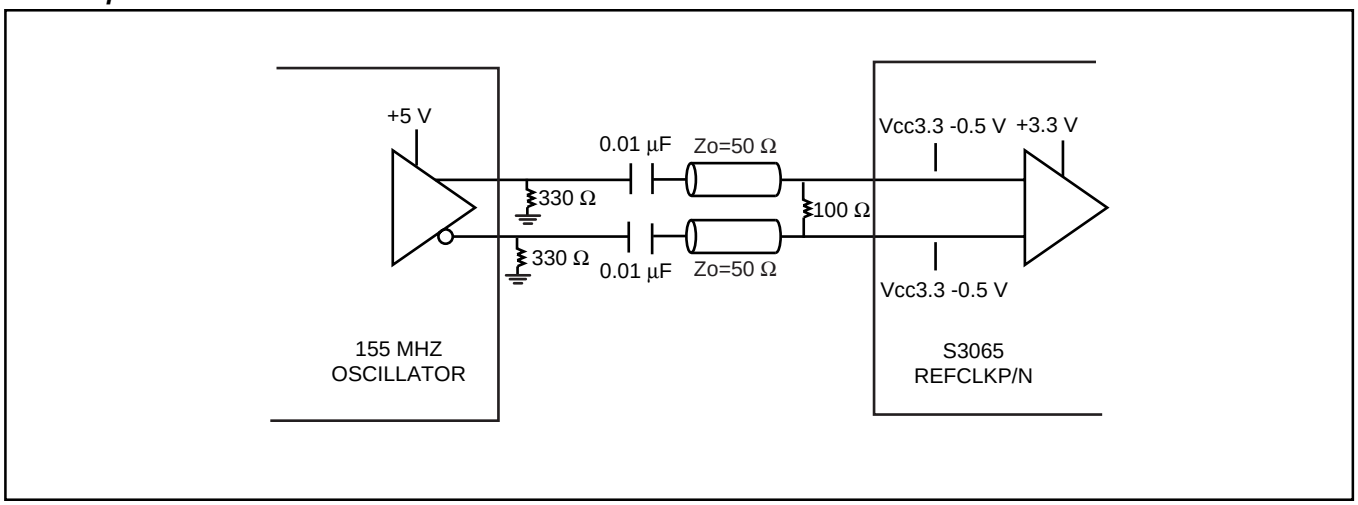


Figure 20. +3V Differential LVPECL Driver to S3065 Differential LVPECL Reference Clock Input DC Coupled Termination

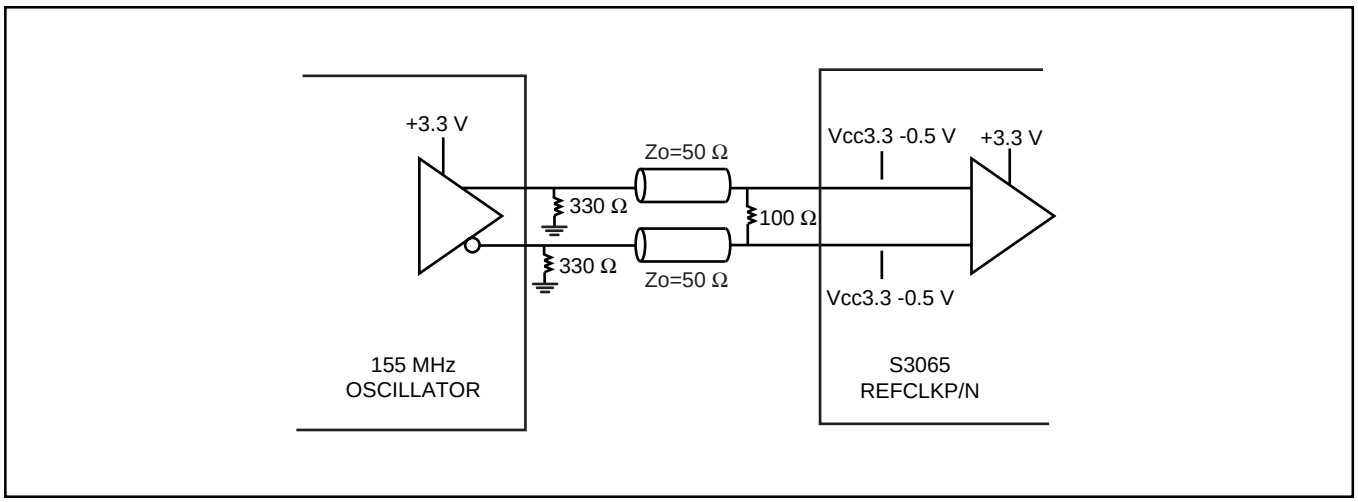


Figure 21. Differential LVPECL Driver to S3065 Internally Biased Differential LVPECL Inputs

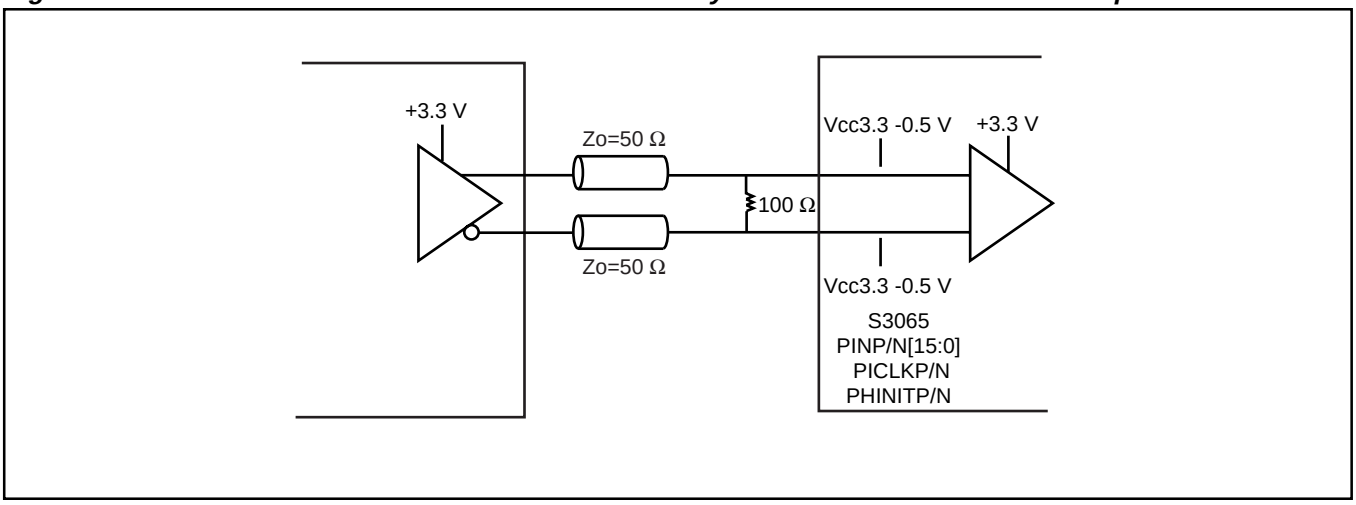
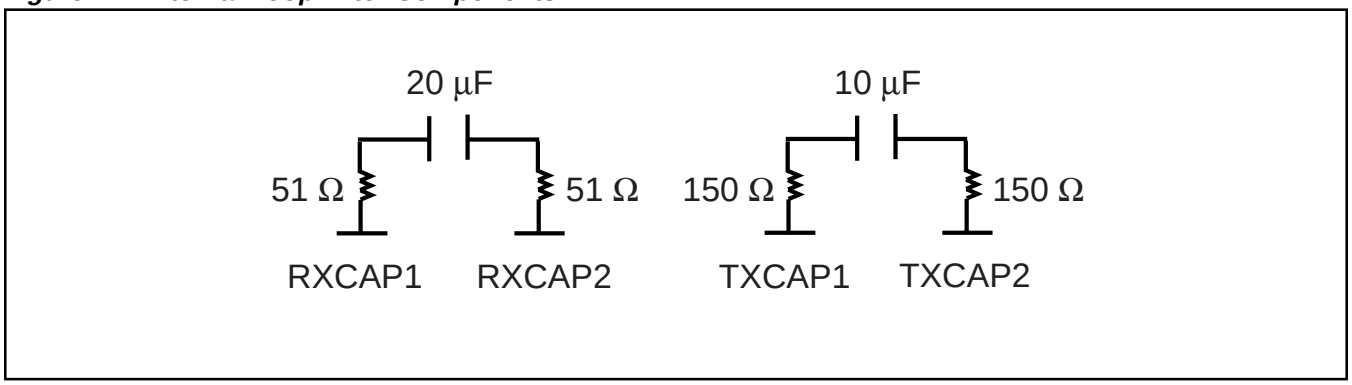


Figure 22. External Loop Filter Components



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3065	PB-324PBGA

X Prefix — XXXX Part No. — XX Package (S3065 PB)

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