65525 Electrical Specifications

65525 ABSOLUTE MAXIMUM CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
P_D	Power Dissipation	–	–	1	W
V_{CC}	Supply Voltage	–0.5	–	7.0	V
V_I	Input Voltage	–0.5	–	V_{CC}+0.5	V
V_O	Output Voltage	–0.5	–	V_{CC}+0.5	V
T_{OP}	Operating Temperature (Ambient)	–25	–	85	°C
T_{STG}	Storage Temperature	–40	–	125	°C

Note: Permanent device damage may occur if Absolute Maximum Ratings are exceeded.
Functional operation should be restricted to the conditions described under Normal Operating Conditions.

65525 NORMAL OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage (5V ±10%)	4.5	5	5.5	V
V_{CC}	Supply Voltage (3.3V ±10%)	3.0	3.3	3.6	V
T_A	Ambient Temperature	0	–	70	°C

65525 DAC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_O	Output Voltage	Io ≤ 10 mA	1.5	–	–	V
Io	Output Current	Vo ≤ 1V @ 37.5Ω Load	21	–	–	mA
	Full Scale Error		–	–	±5	%
	DAC to DAC Correlation		–	1.27	–	%
	DAC Linearity		±2	–	–	LSB
	Full Scale Settling Time		–	–	28	nS
	Rise Time	10% to 90%	–	–	6	nS
	Glitch Energy		–	–	200	pVsec
	Comparator Sensitivity		–	50	–	vM

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

65525 DC CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Notes	Min	Typ	Max	Units
I_{CCDE}	Power Supply Current	0°C, 5.5V, 50 MHz Clk, DAC Enabled	–	150	170	mA
I_{CCDO}	Power Supply Current	0°C, 5.5V, 50 MHz Clk, DAC Disabled	–	125	150	mA
I_{CCDO}	Power Supply Current	0°C, 3.3V, 40 MHz Clk, DAC Disabled	–	50	80	mA
I_{CCS}	Power Supply Current	0°C, 5.5V, Standby	–	–	200	µA
I_{IL}	Input Leakage Current		–100	–	+100	uA
I_{OZ}	Output Leakage Current	High Impedance	–100	–	+100	uA
V_{IL}	Input Low Voltage	All input pins	–0.5	–	0.8	V
V_{IH}	Input High Voltage	All input pins except clocks	2.0	–	V_{CC}+0.5	V
		CLK0, CLK1, CLK2, CLK3	2.8	–	V_{CC}+0.5	V
V_{OL}	Output Low Voltage	Under max load per table below (5V)	–	–	0.5	V
V_{OL}	Output Low Voltage	Under max load per table below (3.3V)	–	–	0.5	V
V_{OH}	Output High Voltage	Under max load per table below (5V)	V_{CC}–0.5	–	–	V
V_{OH}	Output High Voltage	Under max load per table below (3.3V)	2.4	–	–	V

65525 DC DRIVE CHARACTERISTICS

(Under Normal Operating Conditions Unless Noted Otherwise)

Symbol	Parameter	Output Pins	DC Test Conditions	Min	Units
I_{OL}	Output Low Drive	RDY, IRQ, ZWS/, IOCS16/, ENAVEE/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	8	mA
		HSYNC, VSYNC	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	16	mA
		P0-11, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		RASA/, RASB/, CASA/, CASB/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		BLANK/, FLM, LP, ENAVDD/	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	2	mA
I_{OH}	Output High Drive	RDY, IRQ, ZWS/, IOCS16, ENAVEE/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	8	mA
		HSYNC, VSYNC	$V_{OUT}=V_{OL}$, V_{CC}=4.5V	16	mA
		P0-11, PCLK, SHFCLK, D0-15	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		RASA/, RASB/, CASA/, CASB/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		BLANK/, FLM, LP, ENAVDD/	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	4	mA
		All other outputs	$V_{OUT}=V_{OH}$, V_{CC}=4.5V	2	mA

65525 AC TEST CONDITIONS

(Under Normal Operating Conditions Unless Noted Otherwise)

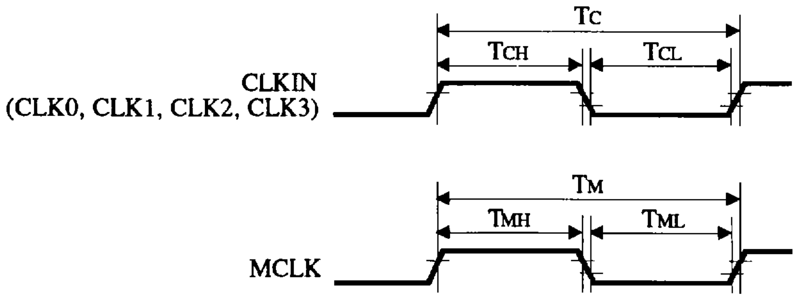
Output Pins	Output Low Voltage	Output High Voltage	Capacitive Load
D0-15, RDY, IRQ, ZWS/, IOCS16/	V_{OL}	2.4V	85pF
P0-7, PCLK, SHFCLK, FPEN/	V_{OL}	2.4V	85pF
HSYNC, VSYNC, BLANK/, FLM, LP	V_{OL}	2.4V	85pF
All Others	V_{OL}	2.4V	85pF

Note: STANDBY/ power measurement was taken using Self Refresh DRAMs.

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

65525 AC TIMING CHARACTERISTICS - CLOCK TIMING

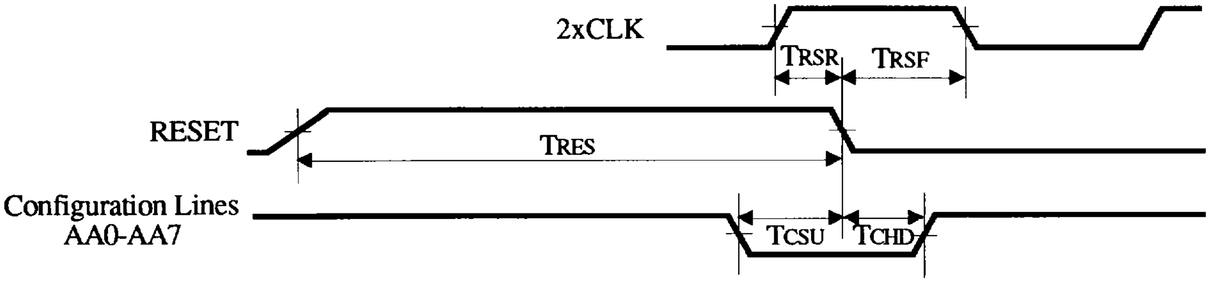
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_C	CLK Period	65 MHz, (5V)	15.4	–	–	nS
T_C	CLK Period	40 MHz, (3.3V)	25	–	–	nS
T_{CH}	CLK High Time		$0.45T_C$	–	$0.55T_C$	nS
T_{CL}	CLK Low Time		$0.45T_C$	–	$0.55T_C$	nS
T_M	MCLK Period	50.350, 56.644 MHz or 65MHz	15.4	–	20	nS
T_{MH}	MCLK High Time		$0.45T_M$	–	$0.55T_M$	nS
T_{ML}	MCLK Low Time		$0.45T_M$	–	$0.55T_M$	nS
T_{RF}	Clock Rise / Fall		–	–	5	nS
–	MCLK Frequency for 100 ns DRAMs (5V)		–	50.350	–	MHz
–	MCLK Frequency for 80 ns DRAMs (5V)		–	56.644	–	MHz
–	MCLK Frequency for 70 ns DRAMs (5V)		–	65	–	MHz



Clock Timing

65525 AC TIMING CHARACTERISTICS - RESET TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
TRES	RESET Pulse Width		64Tc	–	–	nS
TRSR	RESET Delay from 2xCLK rising edge	Local Bus only	4	–	–	nS
TRSF	RESET Delay to 2xCLK falling edge	Local Bus only	13	–	–	nS
TCSU	Configuration setup time		20	–	–	nS
TCHD	Configuration hold time		5	–	–	nS



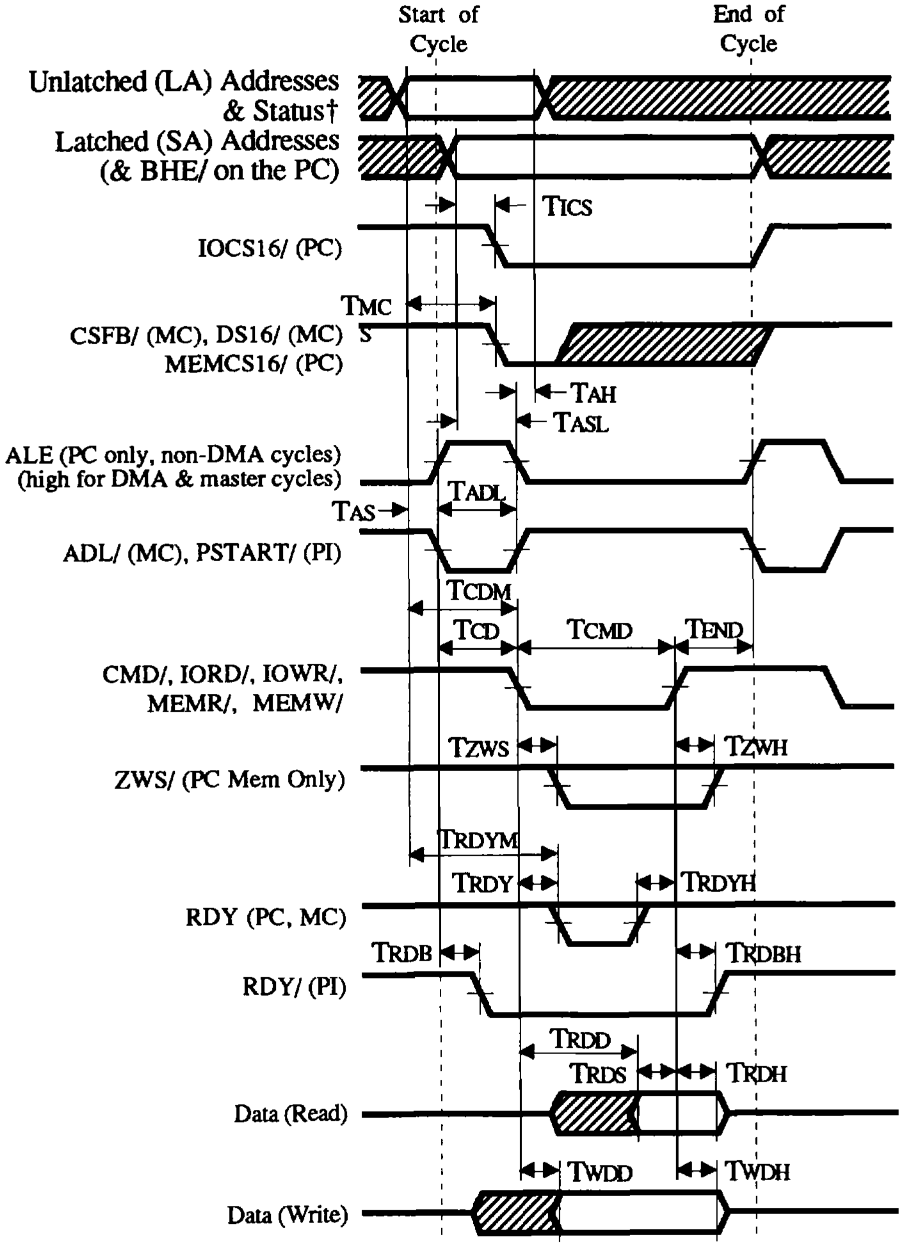
Reset Timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

COMPOSITE BUS TIMING: FOR REFERENCE ONLY

Symbol	Parameter	8 MHz PC Bus	12.5 MHz MC Bus	25 MHz PI Bus	Units
TADL	Address Latch Pulse Width	50 min	40 min	35 min	nS
TCD	Delay from Address Valid to Command Strobe	50 min	40 min	20 min	nS
TCDM	Delay from Start of Cycle to Command Strobe	109 min	85 min	30 min	nS
TCMD	Command Strobe Pulse Width (Asynchronous Cycle)	176 min	90 min	70 min	nS
TCMD	Command Strobe Pulse Width (Synchronous Cycle)	176 min	90 min	40 min	nS
TEND	Delay from End of Command to Start of Next Cycle	50 min	40 min	0 min	nS
TAS	Address Setup to Start of Cycle	0 min	10 min	10 min	nS
TASL	Address Setup to Start of Command	29 min	–	–	nS
TAH	Address Hold from Start of Command	5 min	5 min	–	nS
TRDD	Read Data Delay from Start of Command	187 max	60 max	–	nS
TRDS	Read Data Setup to End of Command	62 min	30 min	48 min	nS
TRDH	Read Data Hold from End of Command (Data Turnoff)	0 min	0 min	12 min	nS
		30 max	30 max	30 max	nS
TWDD	Write Data Delay from Start of Command	40 max	0 max	32 max	nS
TWDH	Write Data Hold from End of Command (Data Turnoff)	10 min	10 min	20 min	nS
		40 max	40 max	40 max	nS
TICS	Delay from Address to IOCS16/	90 max	–	–	nS
TMCS	Delay from Address to MEMCS16/, DS16/, CSFB/	66 max	55 max	–	nS
TZWS	Delay from Start of Command to Start of ZWS/ (16-bit)	40 max	–	–	nS
TZWS	Delay from Start of Command to Start of ZWS/ (8-bit)	1 min	–	–	SYSCLK
TZWH	Delay to End of 0WS/ from End of Command	30 max	–	–	nS
TRDY	Delay to Start of RDY from Start of Command	30 max	–	–	nS
TRDYM	Delay to Start of RDY from Address & Status Valid	–	30 max	–	nS
TRDYH	Delay from End of RDY to End of Command	1 SYSCLK	60 min	–	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Sync)	–	–	28 max	nS
TRDB	Delay from Start of Cycle to RDY/ Low (Async)	–	–	92 min	nS
TRDBH	Delay from End of Command to RDY/ High	–	–	40 max	nS

Note: PC bus specifications correspond to an 8 MHz bus (SYSCLK period of 125nS) (12 MHz bus SYSCLK period would be 80nS)
MC bus specifications correspond to a 25MHz CPU (PS/2 Model 80)
PI bus specifications correspond to 20 MHz CPU; timing specifications scale with clock frequency for other CPU speeds
0WS/ is synchronous to SYSCLK in some systems and has other timing restrictions than shown above (esp. for 8-bit cycles)
Either 0WS/ or RDY may be asserted, but not both (PC Bus)
0WS/ is used for memory accesses only; it works for I/O writes in some systems but not for I/O reads
At the end of the cycle, RDY and 0WS/ should be driven high before being tri-stated
RDY in the MC bus should be generated based on address, status, and MIO/ only



† Status signals are: MIO/ (MC, PI), S0/ & S1/ (MC), AEN (PC-I/O), BHE/ (MC, PI), RD/ (PI), RFSH/ (PC-Mem)

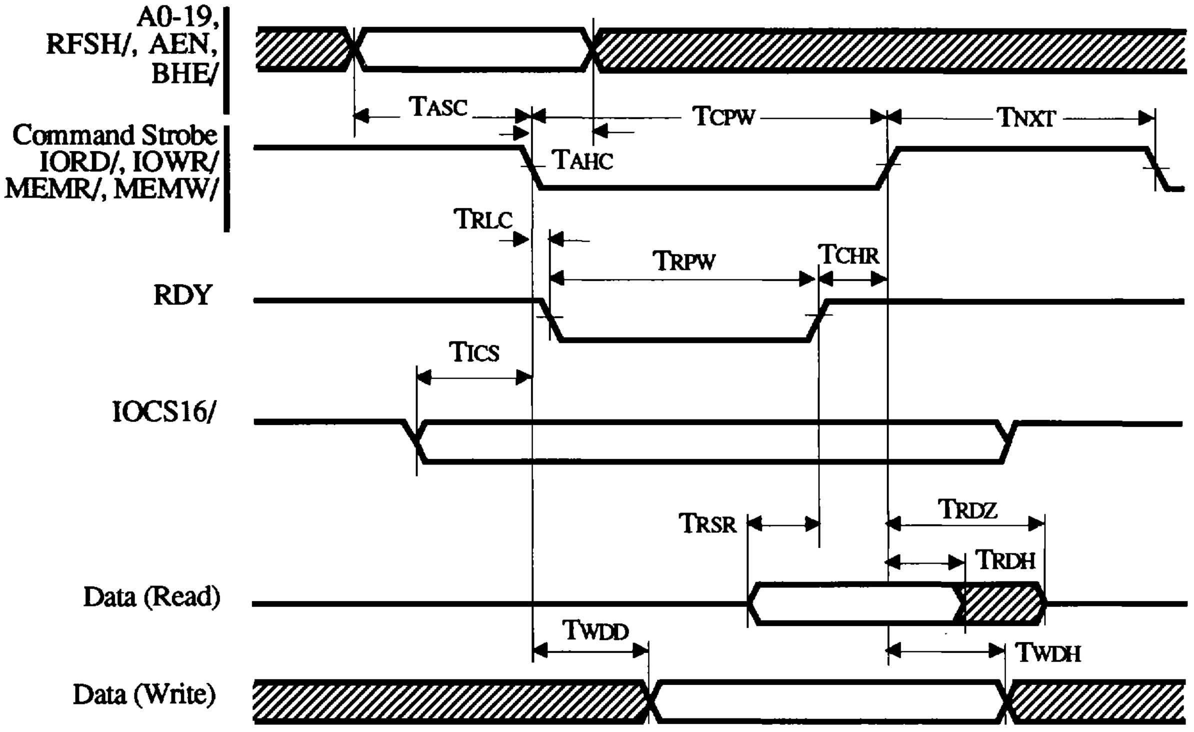
Note: Addresses must be latched on the leading edge of PSTART/ for the PI bus (addresses are not valid on the trailing edge)
Addresses should be latched on the trailing edge of ALE for the PC bus (addresses are not valid on the leading edge)
Addresses should be latched on the leading or trailing edge of ADL/ for the MC bus (addresses are valid on both edges)
Addresses may be latched on the leading edge of CMD/ instead on PC and MC bus (not PI!) if ALE or ADL/ are not used

PC / MC / PI Bus Timing Characteristics for Non-Bus-Master Peripheral Devices

65525 AC TIMING CHARACTERISTICS - PC BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width		6Tm	–	–	nS
T_{CHR}	Command Strobe Hold from Ready		0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		3Tm	–	–	nS
T_{ASC}	Address Setup to Command Strobe		30	–	–	nS
T_{ISC}	IOCS16/ Delay from valid address		–	–	2Tm	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	100Tm	nS
T_{AHC}	Address Hold to Command Strobe		20	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		10	–	–	nS
T_{RDZ}	Read Data Tristated from Command Strobe		–	–	40	nS
T_{WDD}	Write Data Delay from Command Strobe		–	–	20	nS
T_{WDH}	Write Data Hold from Command Strobe		10	–	–	nS
T_{RLC}	RDY Low Delay from Command Strobe	Mem Accesses Only	–	–	40	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

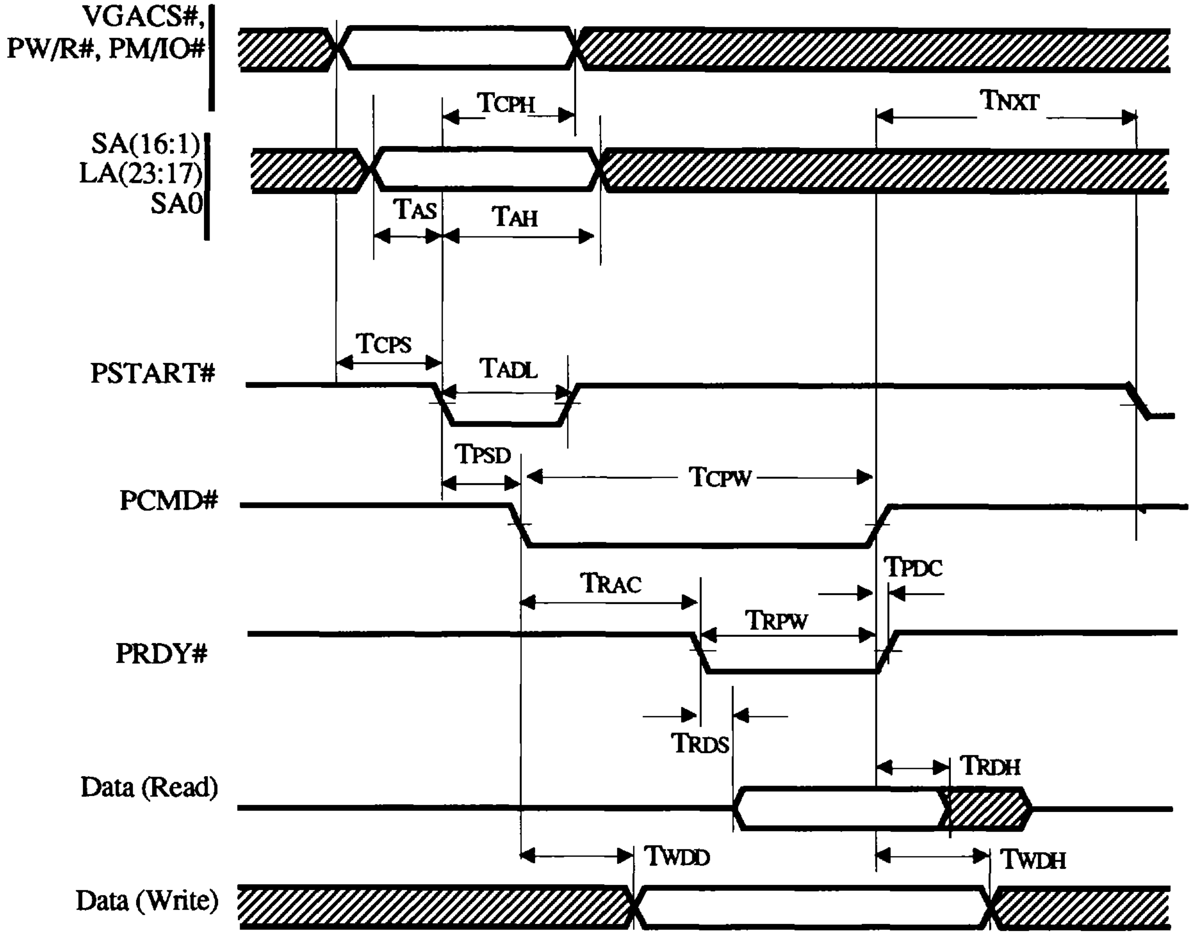


PC Bus Cycle Timing

65525 AC TIMING CHARACTERISTICS - PI BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width		4Tm	–	–	nS
T_{NXT}	Delay from Command Inactive to PSTART# Active		0			nS
T_{CPS}	CS and Command Setup Time to PSTART#Active		10			nS
T_{CPH}	CS and Command Hold Time to PSTART# Active		1.5Tm+5	–	–	nS
T_{RDS}	Read Data Setup from PRDY# Active		15	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		20	–	–	nS
T_{WDD}	Write Data Delay from PCMD#		–	–	2Tm	nS
T_{RPW}	RDY Pulse Width		0	–	100Tm	nS
T_{WDH}	Write Data Invalid Delay from PCMD# Inactive		0	–	–	nS
T_{AS}	Address Setup to PSTART# Active		10	–	–	nS
T_{AH}	Address Hold to PSTART# Active		1.5Tm+5	–	–	nS
T_{ADL}	PSTART# Pulse Width		25	–	–	nS
T_{PSD}	Delay from PSTART# to PCMD#		15	–	–	nS
T_{PDC}	Delay from PCMD# Inactive to PRDY# Inactive		8	–	40	nS
T_{RAC}	PRDY# Active from Command Strobe		2Tm	–	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

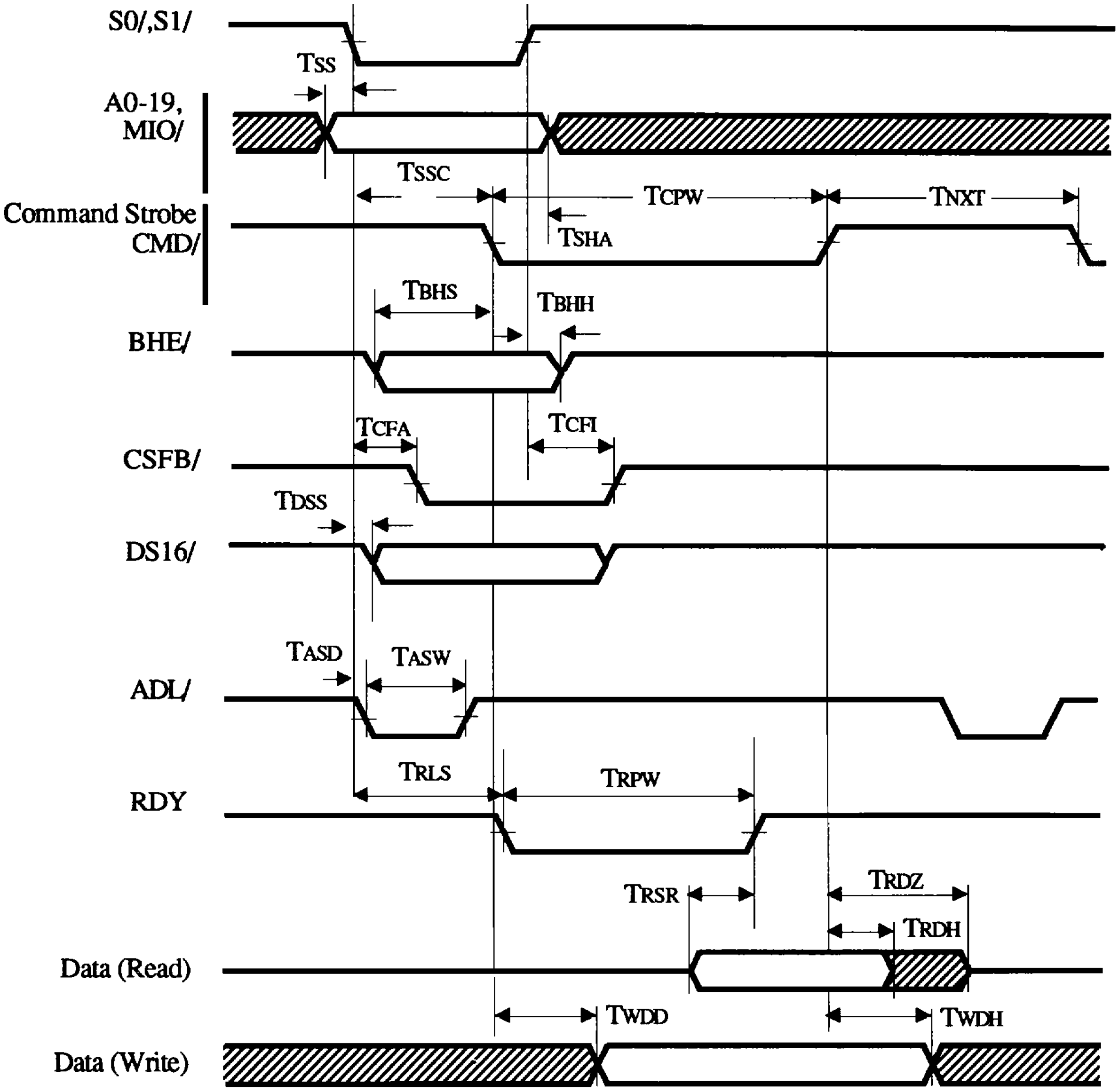


PI Bus Cycle Timing

65525 AC TIMING CHARACTERISTICS - MC BUS TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CPW}	Command Strobe Pulse Width		4Tm	–	–	nS
T_{SSC}	Status Setup to Command Strobe		55	–	–	nS
T_{SHA}	Status Hold from Command Strobe		30	–	–	nS
T_{SS}	Status Active from address valid		0	–	–	nS
T_{NXT}	Command Strobe Inactive to Next Strobe		3Tm	–	–	nS
T_{RSR}	Read Data Setup to Ready	Mem Accesses Only	25	–	–	nS
T_{RPW}	RDY Pulse Width	Mem Accesses Only	0	–	100Tm	nS
T_{DSS}	DS16/ Active from address valid		5	–	Tm	nS
T_{DS}	DS16/ Inactive from Status		–	–	Tm	nS
T_{BHS}	BHE/ Setup to CMD/		30	–	–	nS
T_{BHH}	BHE/ Hold from CMD/		20	–	–	nS
T_{RDH}	Read Data Hold from Command Strobe		10	–	–	nS
T_{RDZ}	Read Data Tristated from Command Strobe		–	–	40	nS
T_{WDD}	Write Data Delay from Command Strobe		–	–	20	nS
T_{WDH}	Write Data Hold from Command Strobe		10	–	–	nS
T_{RLS}	RDY Low Delay from Status		–	–	30	nS
T_{ASD}	ADL/ from Status Active		12	–	–	nS
T_{ASW}	ADL/ Pulse Width		40	–	–	nS
T_{CFA}	CSFB/ Active from Address/Status Valid		–	–	40	nS
T_{CFI}	CSFB/ Inactive from Address/Status Invalid		–	–	40	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.



MC Bus Cycle Timing

65525 DC TIMING CHARACTERISTICS - 386 SX LOCAL BUS TIMING AT 25MHz

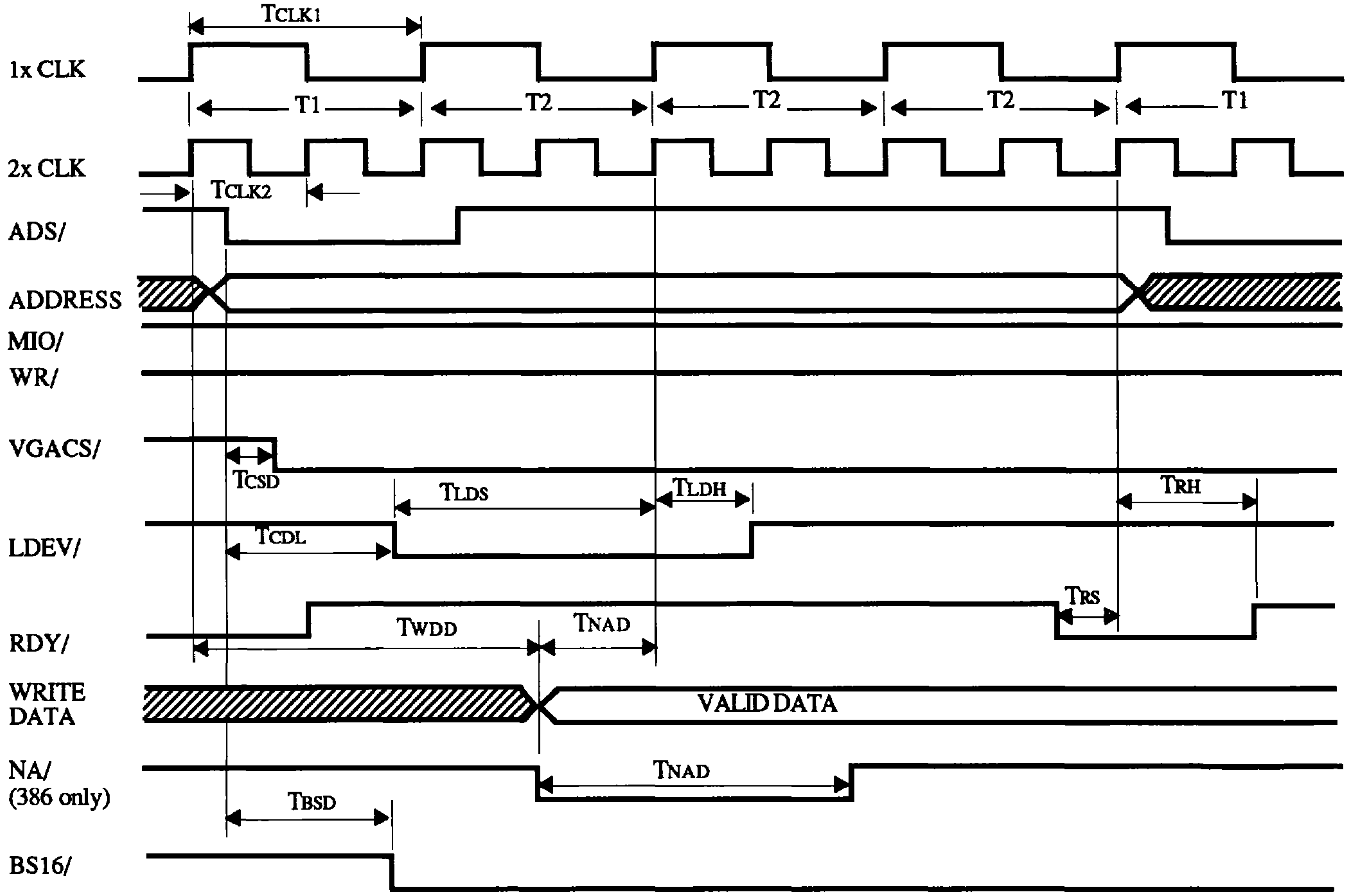
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CLK2}	2x CPU Clock Cycle Time			20		nS
T_{CDL}	Delay from Start of T1 to LDEV/			15		nS
T_{LDS}	LDEV/ Setup Time from End of T2			43		nS
T_{LDH}	LDEV/ Hold Time from End of T2			23		nS
T_{RS}	RDY/ Setup Time from End of T2			18		nS
T_{RH}	RDY/ Hold Time from End of T2			20		nS
T_{NAD}	NA/ Delay from 2x CLK			13		nS
T_{NA}	NA/ Pulse Width			40		nS
T_{WDD}	Write Data Delay from Start of T1			38		nS
T_{RDS}	Read Data Setup Time from End of T2			95		nS
T_{RDH}	Read Data Hold Time from RDY/ High			42		nS
T_{BSD}	BS16/ Delay from ADS/			43		nS
T_{CSD}	VGACS/ Delay from ADS/			18		nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

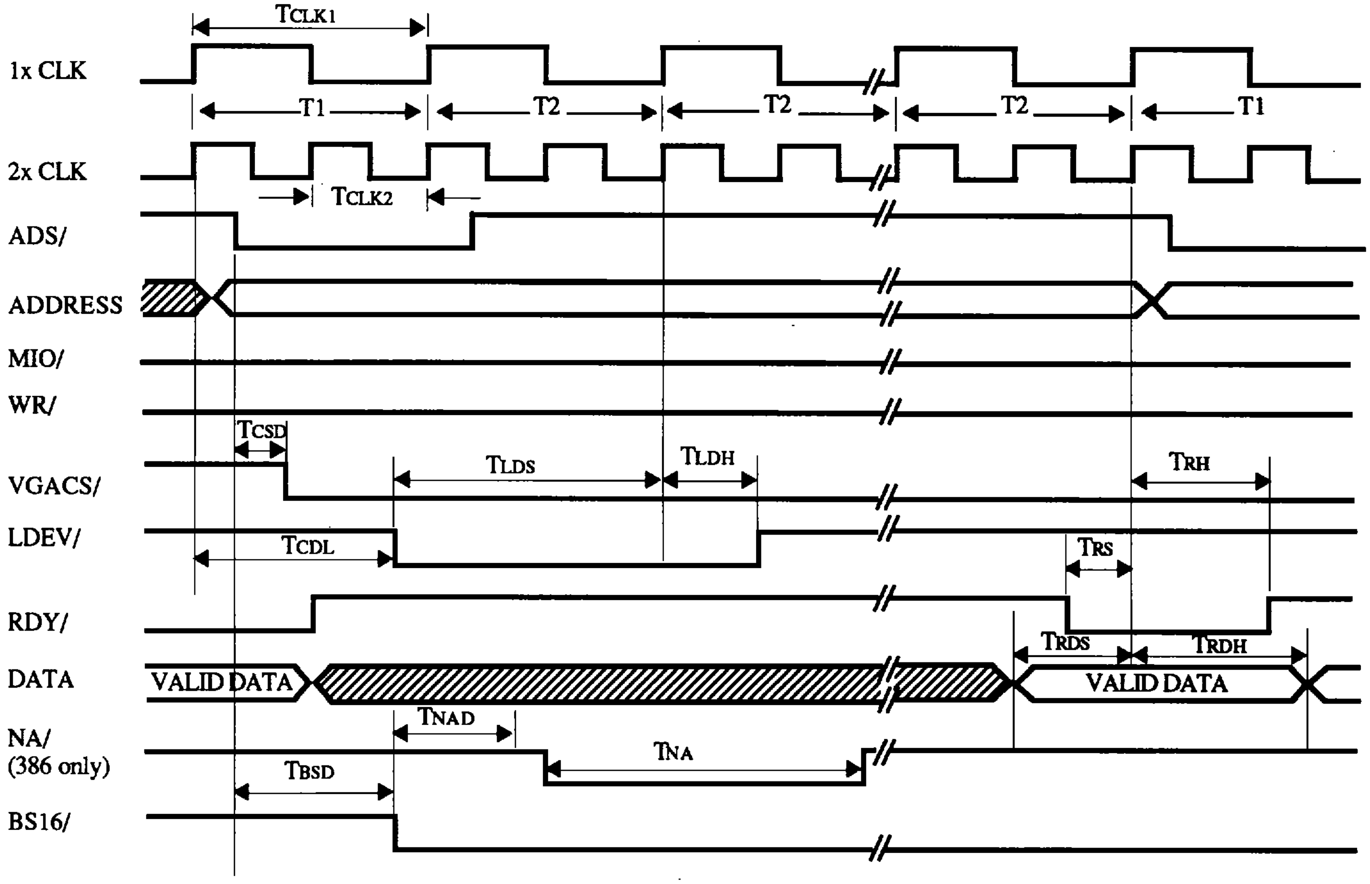
65525 DC TIMING CHARACTERISTICS - 486 LOCAL BUS TIMING AT 33MHz

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CLK1}	CPU Clock Cycle Time			30		nS
T_{CLK2}	2x CPU Clock Cycle Time			15		nS
T_{CDL}	Delay from End of T1 to LDEV/			31		nS
T_{LDS}	LDEV/ Setup Time from End of T2			17		nS
T_{LDH}	LDEV/ Hold Time from End of T2			5		nS
T_{RS}	RDY/ Setup Time from End of T2			27		nS
T_{RH}	RDY/ Hold Time from End of T2			3		nS
T_{BSD}	BS16/ Delay from ADS/			53		nS
T_{WDD}	Write Data Delay from Start of T1			55		nS
T_{RDS}	Read Data Setup Time from End of T2			55		nS
T_{RDH}	Read Data Hold Time from RDY/ High			6		nS
T_{CSD}	VGACS/ Delay from ADS/			7.5		nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.



65525 x86 Local Bus Write Cycle Timing

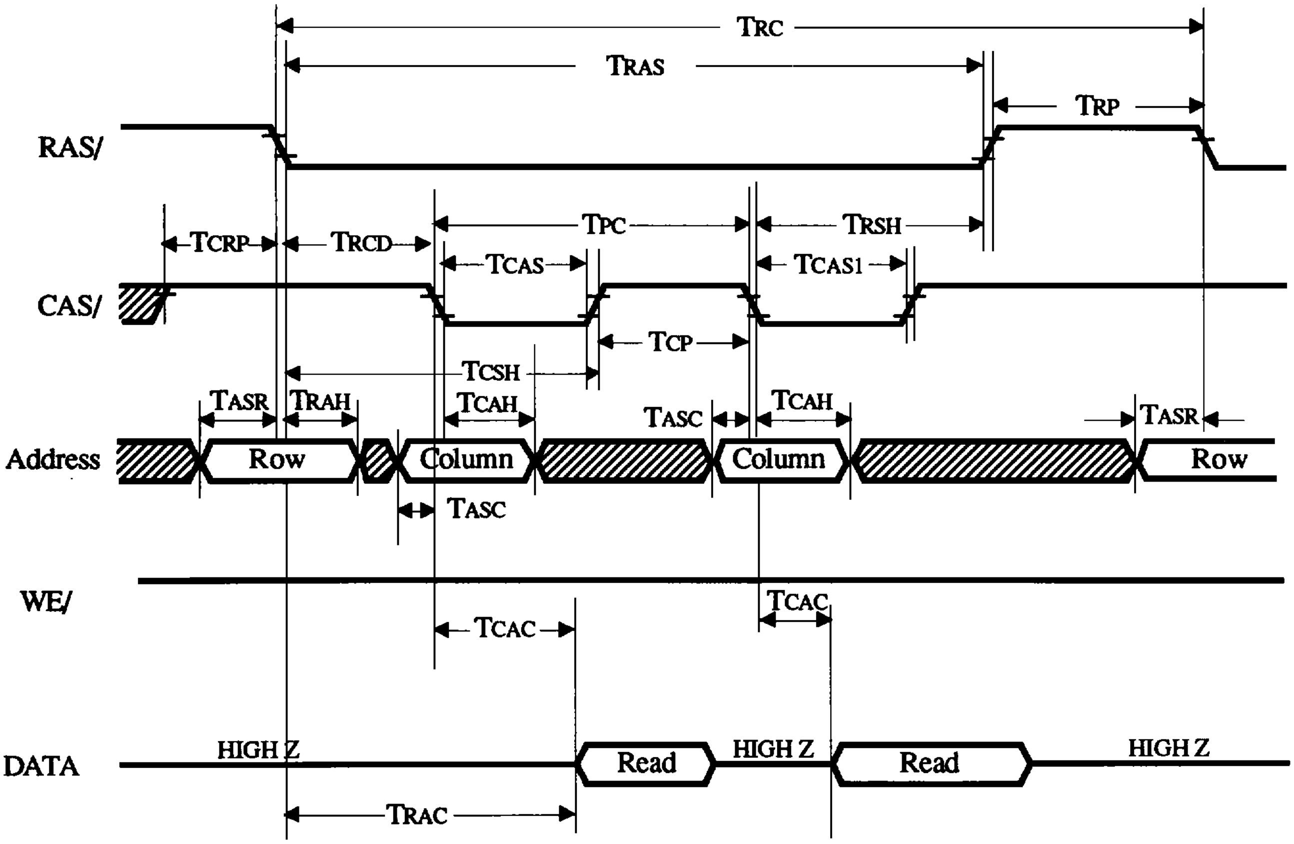


65525 x86 Local Bus Read Cycle Timing

65525 AC TIMING CHARACTERISTICS - DRAM READ/WRITE TIMING

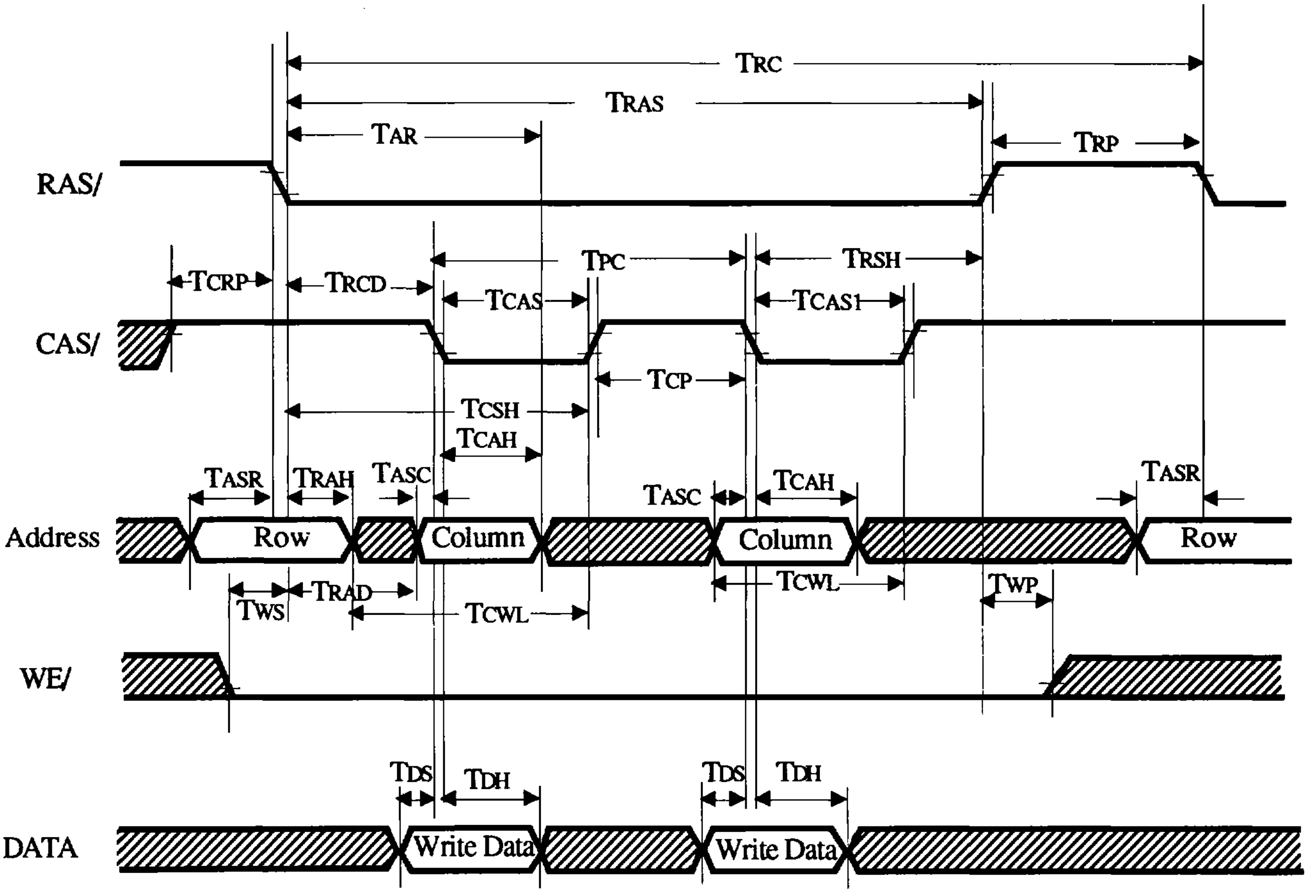
		2 DRAM	2 DRAM	4 DRAM	4 DRAM	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read/Write Cycle Time	18Tm – 5	–	12Tm – 5	–	nS
T_{RAS}	RAS/ Pulse Width	14Tm – 5	–	8Tm – 5	–	nS
T_{RP}	RAS/ Precharge	4Tm - 1	–	4Tm - 1	–	nS
T_{CRP}	CAS/ to RAS/ Precharge	4Tm – 5	–	4Tm – 5	–	nS
TCSH	CAS/ Hold from RAS/	5Tm - 2	–	5Tm - 2	–	nS
T_{RCD}	RAS/ to CAS/ delay	3Tm – 5	–	3Tm – 5	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm – 5	–	2Tm – 5	–	nS
T_{CP}	CAS/ Precharge	Tm – 5	–	Tm – 5	–	nS
T_{CAS}	CAS/ Pulse Width	3Tm – 5	–	3Tm – 5	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Tm – 5	–	2Tm – 5	–	nS
T_{ASR}	Row Address Setup to RAS/	0	–	0	–	nS
TASC	Column Address Setup to CAS/	0	–	0	–	nS
T_{RAH}	Row Address Hold from RAS/	Tm - 3	–	Tm - 3	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm	–	Tm	–	nS
T_{CAC}	Data Access Time from CAS/	–	2Tm – 5	–	2Tm – 5	nS
T_{RAC}	Data Access time from RAS/		5Tm		5Tm	nS
T_{DS}	Write Data Setup to CAS/	0	–	0	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm – 5	–	2Tm – 5	–	nS
TPC	CAS Cycle Time	3Tm - 1	–	3Tm - 1	–	nS
T_{WS}	WE/ Setup to RAS/	5	2Tm	5	2Tm	nS
T_{WP}	WE/ Hold from RAS/	0	–	0	–	nS

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.



DRAM Page Mode Read Cycle Timing

Note: The above diagram represents a typical page mode read cycle. The number of actual CAS cycles may vary. The maximum number of CAS cycles allowed is 32 (when the FIFO is being filled).

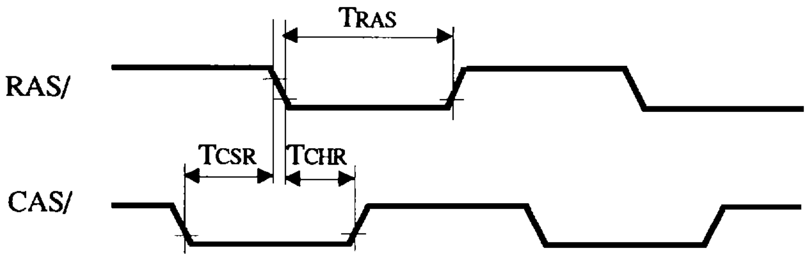


DRAM Page Mode Write Cycle Timing

Note: The above diagram represents a typical page mode write cycle. The number of actual CAS cycles may vary between 0 and 4.

65525 AC TIMING CHARACTERISTICS - REFRESH TIMING

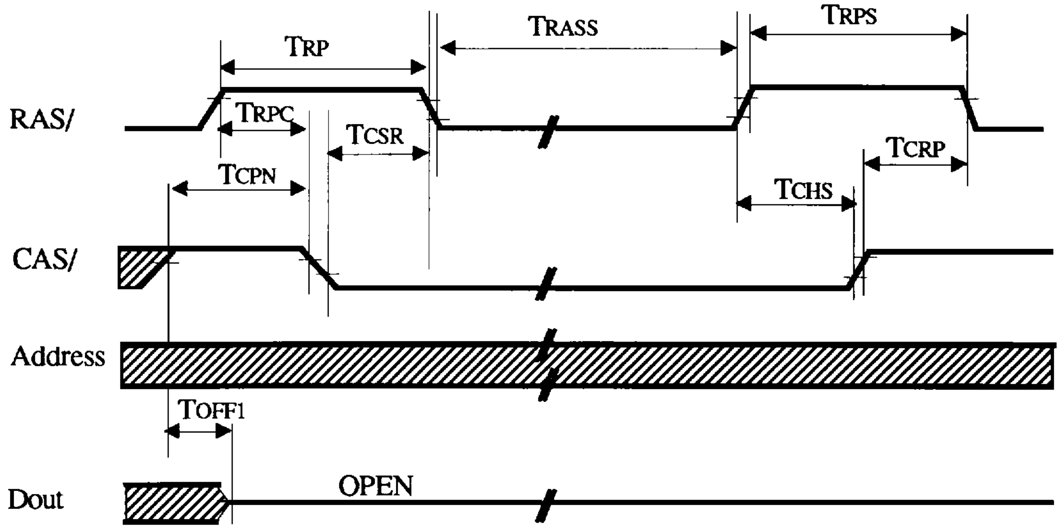
Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 15.4 @ 65 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay		Tm – 5	–	Tm + 5	nS
TRAS	RAS pulse width	5Tm = 89 ns (56 MHz) or 77 ns (65 MHz)	5Tm – 5	–	5Tm + 5	nS



CAS-Before-RAS (CBR) DRAM Refresh Cycle Timing

65525 AC TIMING CHARACTERISTICS - SELF REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{RASS}	RAS/ pulse width		100	–	–	µS
TRPS	RAS/ precharge time		4Tm	–	–	nS
TCHS	CAS/ hold time		0	–	–	nS



Self Refresh DRAM Refresh Cycle Timing

Note: Upon exiting self refresh mode, the 65525 will perform a complete set of CAS/ before RAS/ refresh cycles before resuming normal DRAM activity. The duration of the burst refresh will equal the panel power sequencing delay, programmed in XR5B bits 7-4.

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

65525 AC TIMING CHARACTERISTICS - VRAM READ/WRITE TIMING

		2 VRAM	2 VRAM	4 VRAM	4 VRAM	
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Units**
T_{RC}	Read/Write Cycle Time	12Tm - 5	–	9Tm - 5	–	nS
T_{RAS}	RAS/ Pulse Width	8Tm - 5	–	5Tm - 5	–	nS
T_{AR}	Column Address Hold from RAS/	4Tm	–	4Tm	–	nS
T_{RP}	RAS/ Precharge	4Tm	–	4Tm	–	nS
T_{CRP}	CAS/ to RAS/ Precharge	4Tm	–	4Tm	–	nS
T_{CSH}	CAS/ Hold from RAS/	5Tm - 2	–	5Tm - 2	–	nS
T_{RCD}	RAS/ to CAS/ delay	2Tm	–	2Tm	–	nS
T_{RSH}	RAS/ Hold from CAS/	2Tm - 5	–	2Tm - 5	–	nS
T_{CPN}	CAS/ Precharge	Tm	–	Tm	–	nS
T_{CAS}	CAS/ Pulse Width	3Tm - 5	–	3Tm - 5	–	nS
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Tm - 5	–	2Tm - 5	–	nS
T_{ASR}	Row Address Setup to RAS/	2Tm - 10	–	2Tm - 10	–	nS
T_{ASC}	Column Address Setup to CAS/	Tm -10	–	Tm -10	–	nS
T_{RAD}	Column Address from RAS/	Tm	–	Tm	–	nS
T_{RAH}	Row Address Hold from RAS/	Tm	–	Tm	–	nS
T_{CAH}	Column Address Hold from CAS/	Tm + 1	–	Tm + 1	–	nS
T_{CAC}	Data Access Time from CAS/	–	2Tm	–	2Tm	nS
T_{RAC}	Data Access Time from RAS/	–	5Tm	–	5Tm	nS
T_{OEA}	Data Access Time from OE/	–	4Tm	–	4Tm	nS
T_{WP}	WE/ Pulse Width	6Tm	–	6Tm	–	nS
T_{DS}	Write Data Setup to CAS/	Tm	–	Tm	–	nS
T_{DH}	Write Data Hold from CAS/	2Tm	–	2Tm	–	nS
T_{DHR}	Write Data Hold from RAS/	4Tm	–	4Tm	–	nS
T_{WS}	WE/ Setup to RAS/	5	2Tm	5	2Tm	nS
T_{WP}	WE/ Hold from RAS/	0	–	0	–	nS
T_{DLS}	DT/ Low Setup	Tm - 5	–	Tm - 5	–	nS
T_{RDH}	DT/ Low Hold after RAS/ Low	4Tm	–	4Tm	–	nS
T_{CDH}	DT/ Low Hold after CAS/ Low	3Tm - 5	–	3Tm - 5	–	nS
T_{THS}	DT/ High Setup	Tm - 5	–	Tm - 5	–	nS
T_{THH}	DT/ High Hold	Tm	–	Tm	–	nS

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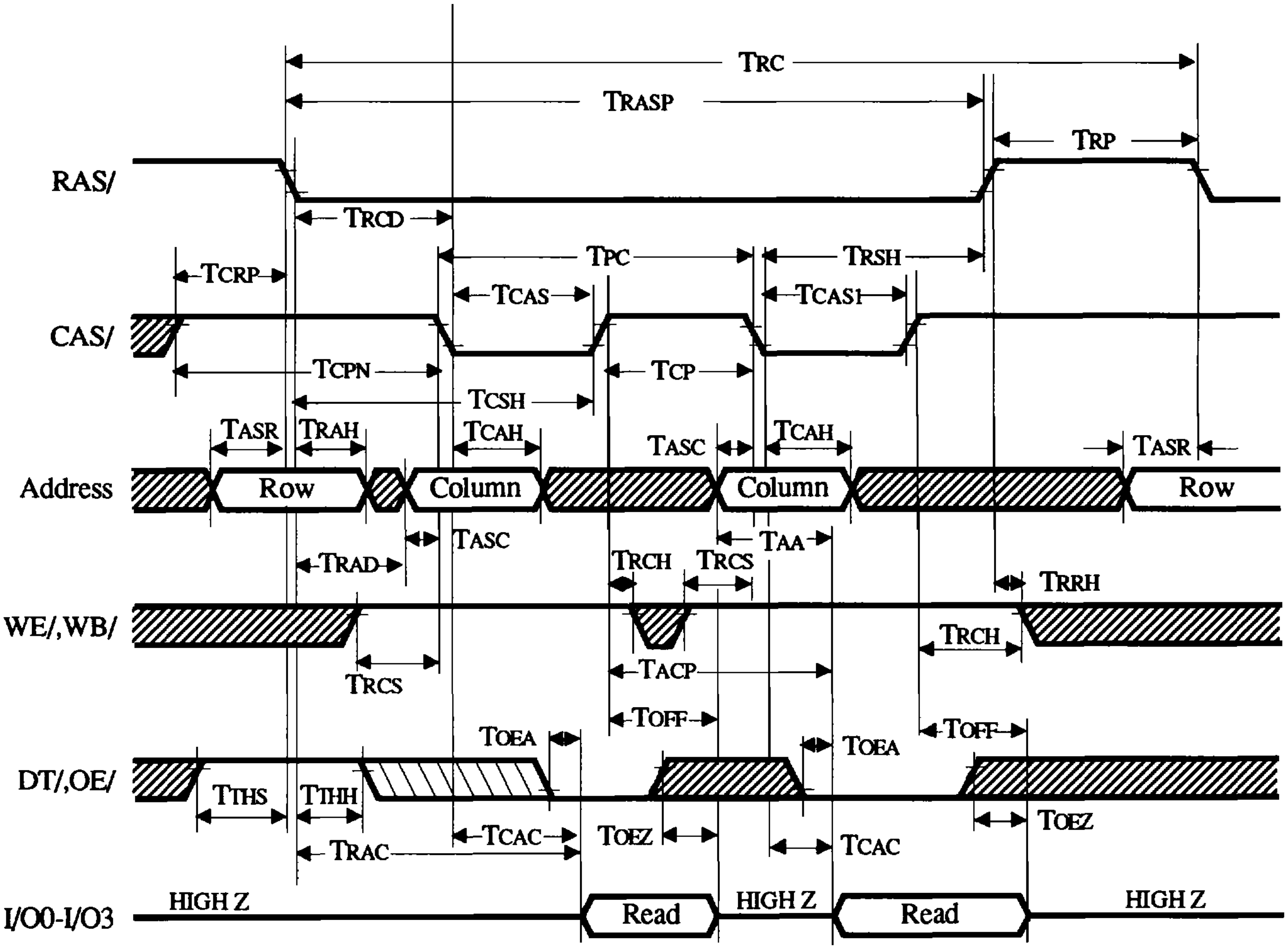
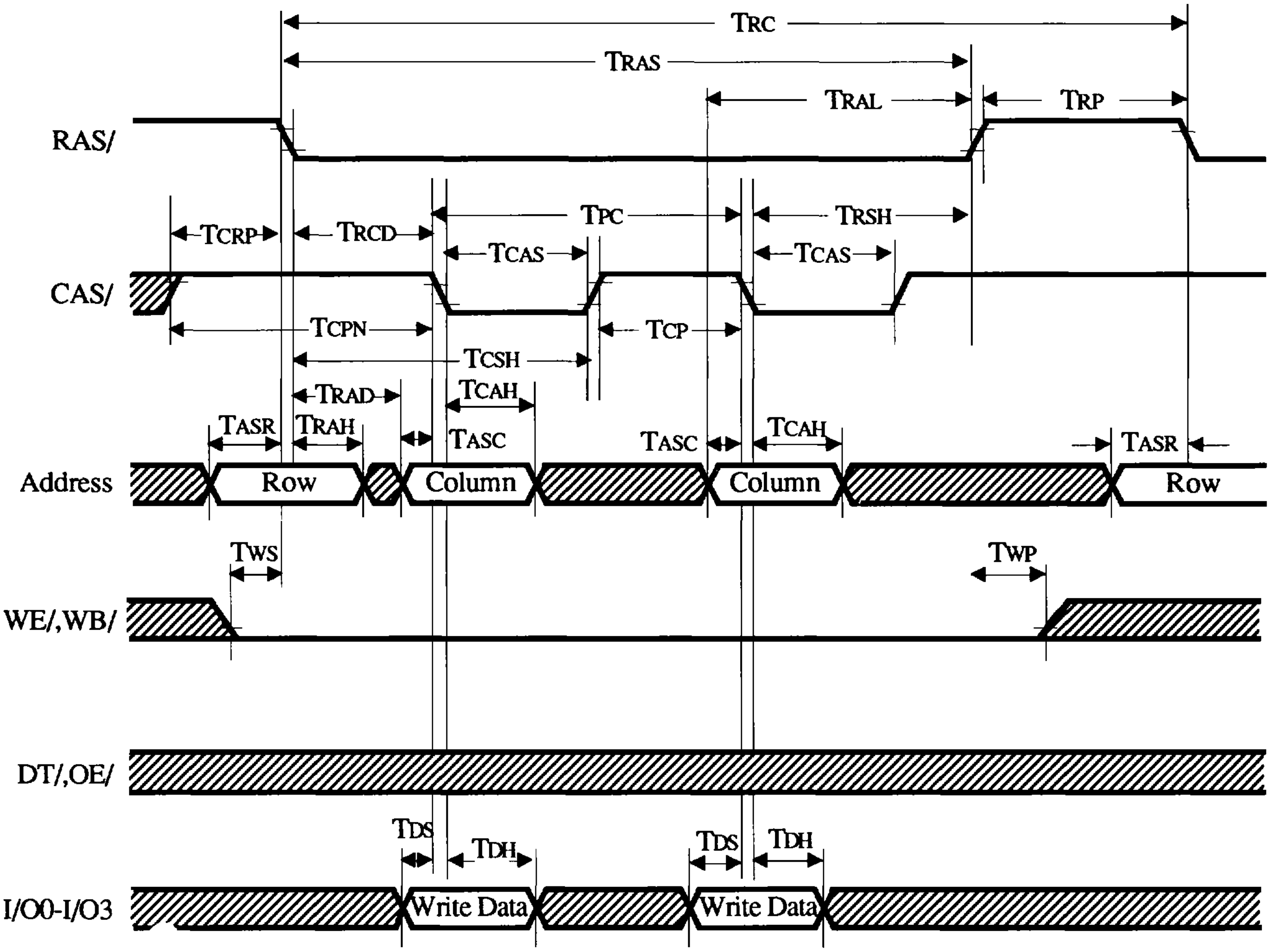
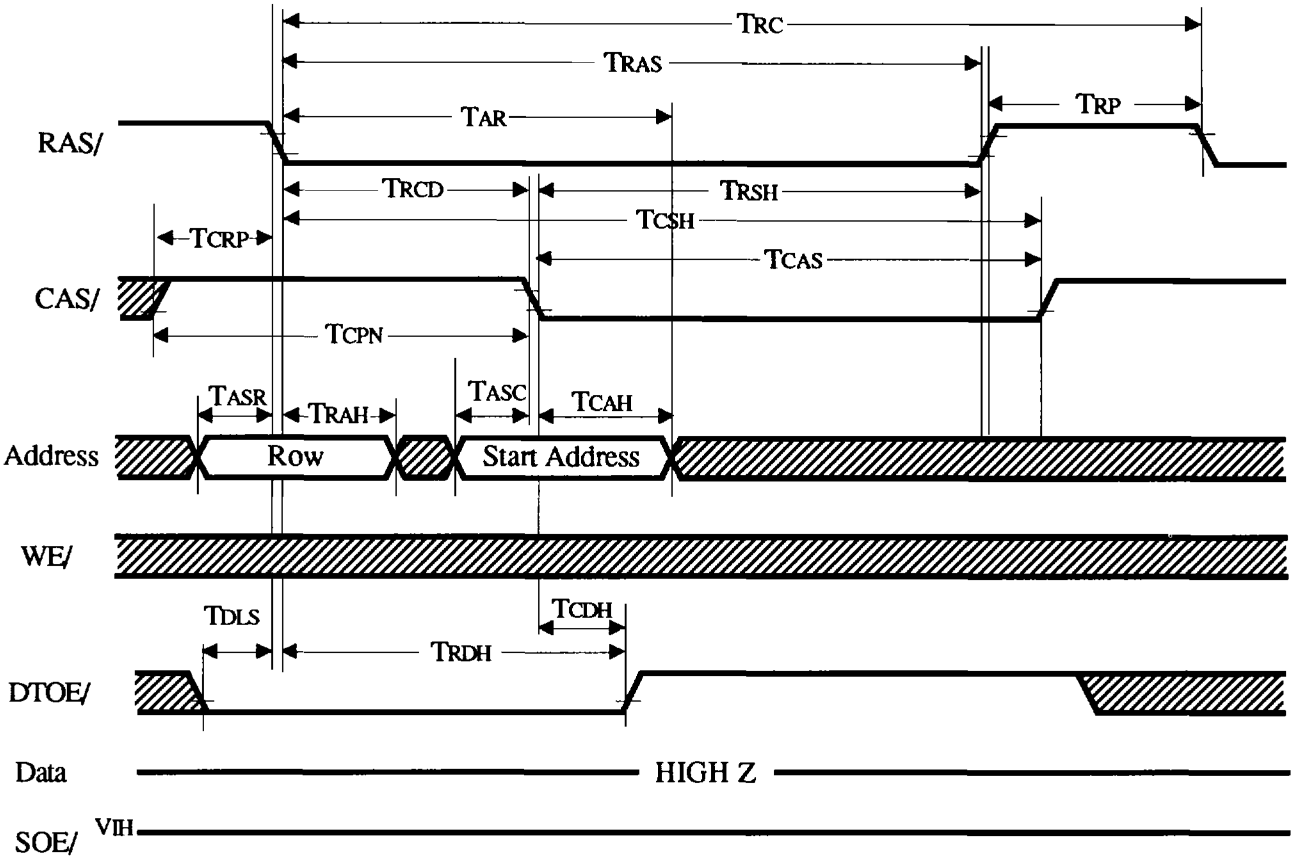


VRAM Page Mode Read Cycle Timing



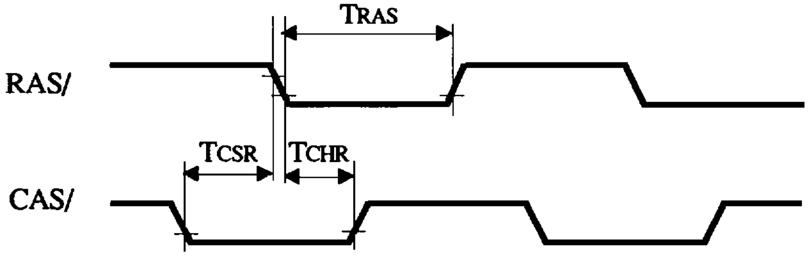
VRAM Page Mode Write Cycle Timing



VRAM Transfer Cycle Timing

65525 AC TIMING CHARACTERISTICS - VRAM REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	Tm = 15.4 @ 65 MHz	5Tm – 5	–	5Tm + 5	nS
T_{CSR}	CAS to RAS delay		Tm – 5	–	Tm + 5	nS
T_{RAS}	RAS pulse width	5Tm = 89 ns (56 MHz) or 77 ns (65 MHz)	5Tm – 5	–	5Tm + 5	nS



CAS-Before-RAS (CBR) VRAM Refresh Cycle Timing

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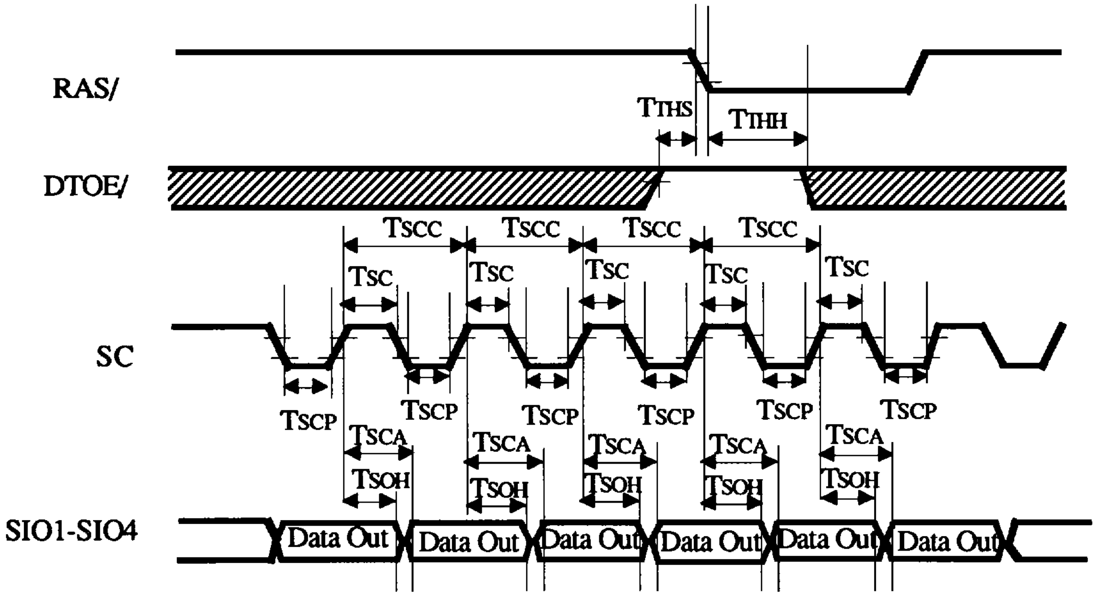
65525 AC TIMING CHARACTERISTICS - VRAM SERIAL PORT TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_{SCC}	Sequencer Clock	40	–	50	nS
T_{SC}	Serial Clock Cycle Time	–	0.45 T_{SCC}	–	nS
T_{SCP}	Serial Clock Precharge Time	–	0.45 T_{SCC}	–	nS
T_{SCA}	Access Time from SC	–	–	25	nS
T_{SOH}	Serial Output Hold Time	5	–	–	nS
T_{THS}	DT/ High Setup	T_M - 5	–	–	nS
T_{THH}	DT/ High Hold	T_M	–	–	nS



VRAM Serial Read Cycle Timing

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65525 AC TIMING CHARACTERISTICS - FRAME BUFFER TIMING

Symbol	Parameter	Min	Max	Units
T_{PC}	Fast Page Cycle Time	6Td	–	ns
T_{RC}	Read/Write Cycle Time	10Td	–	ns
T_{RAS}	RAS/ Pulse Width	6Td	–	ns
T_{RP}	RAS/ Precharge	4Td	–	ns
T_{CRP}	CAS/ to RAS/ precharge	5Td	–	ns
T_{CSH}	CAS/ Hold from RAS/	5Td	–	ns
T_{RCD}	RAS/ to CAS/ delay	2Td	–	ns
T_{RSH}	RAS/ Hold from CAS/	5Td	–	ns
T_{CP}	CAS/ Precharge	3Td	–	ns
T_{CAS1}	CAS/ Pulse Width (Fast Page Cycle)	2Td	–	ns
T_{ASR}	Row Address Setup to RAS/	5Td	–	ns
T_{ASC}	Column Address Setup to CAS/	Td -10	–	ns
T_{RAD}	Column Address from RAS/	Td	–	ns
T_{RAH}	Row Address Hold from RAS/	Td	–	ns
T_{CAH}	Column Address Hold from CAS/	Td	–	ns
T_{WP}	WE/ Pulse Width	6Td	–	ns
T_{DS}	Write Data Setup to CAS/	Td + 5	–	ns
T_{DH}	Write Data Hold from CAS/	Td	–	ns
T_{WCS}	WE/ Setup	Td	–	ns
T_{WPR}	WE/ Hold from RAS/	Td	–	ns
T_{THS}	DT/ High Setup	6Td	–	ns
T_{THH}	DT/ High Hold	Td	–	ns
T_{DLS}	DT/ Low Setup	5Td	–	ns
T_{RDH}	DT/ Low Hold after RAS/ Low	4Td	–	ns
T_{CDH}	DT/ Low Hold after CAS/ Low	2Td - 5	–	ns

Note: These specifications are based on the dot clock rate. The maximum dot clock rate for frame buffer operation is 40 MHz (Td = 25 ns).

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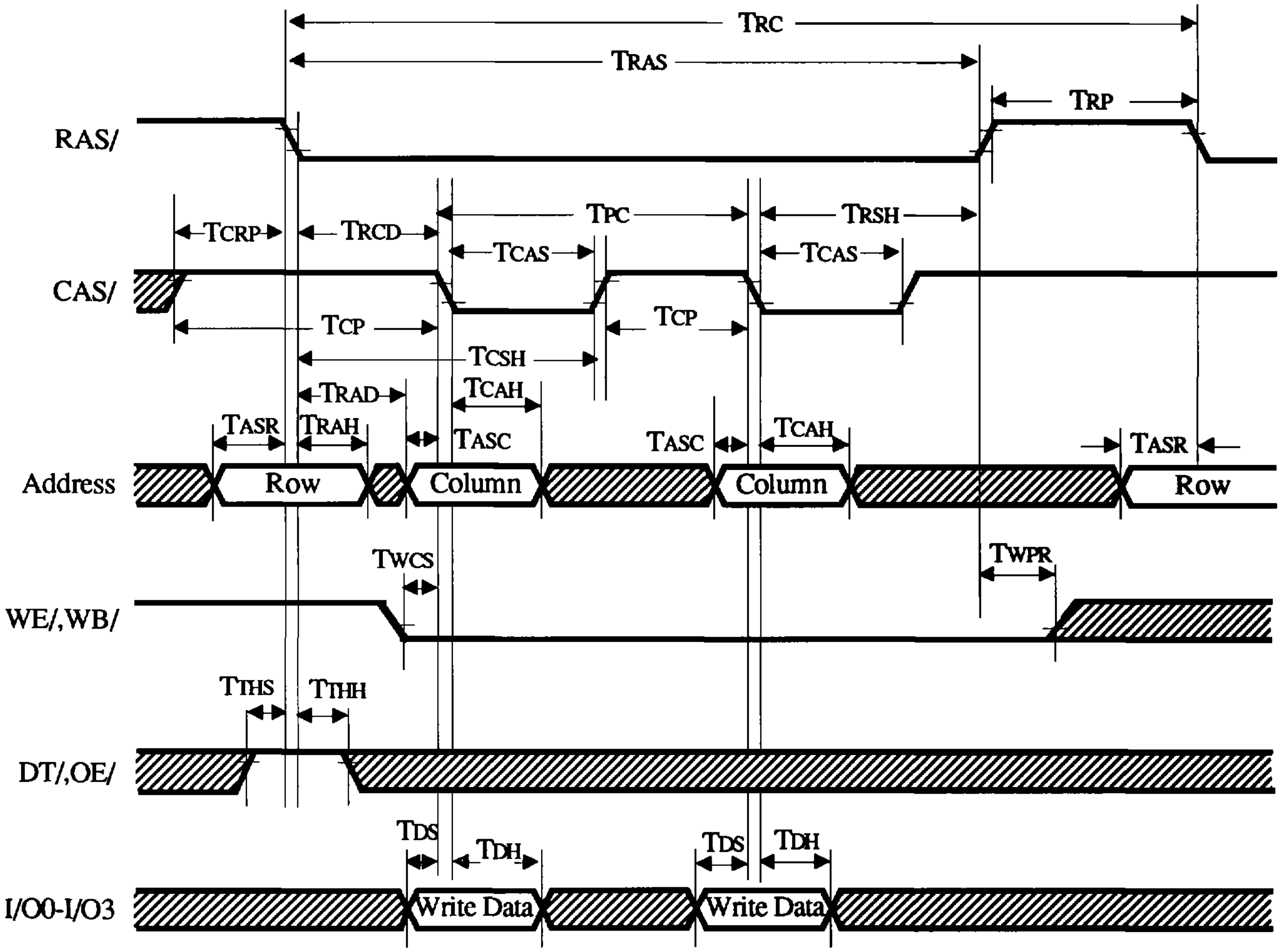
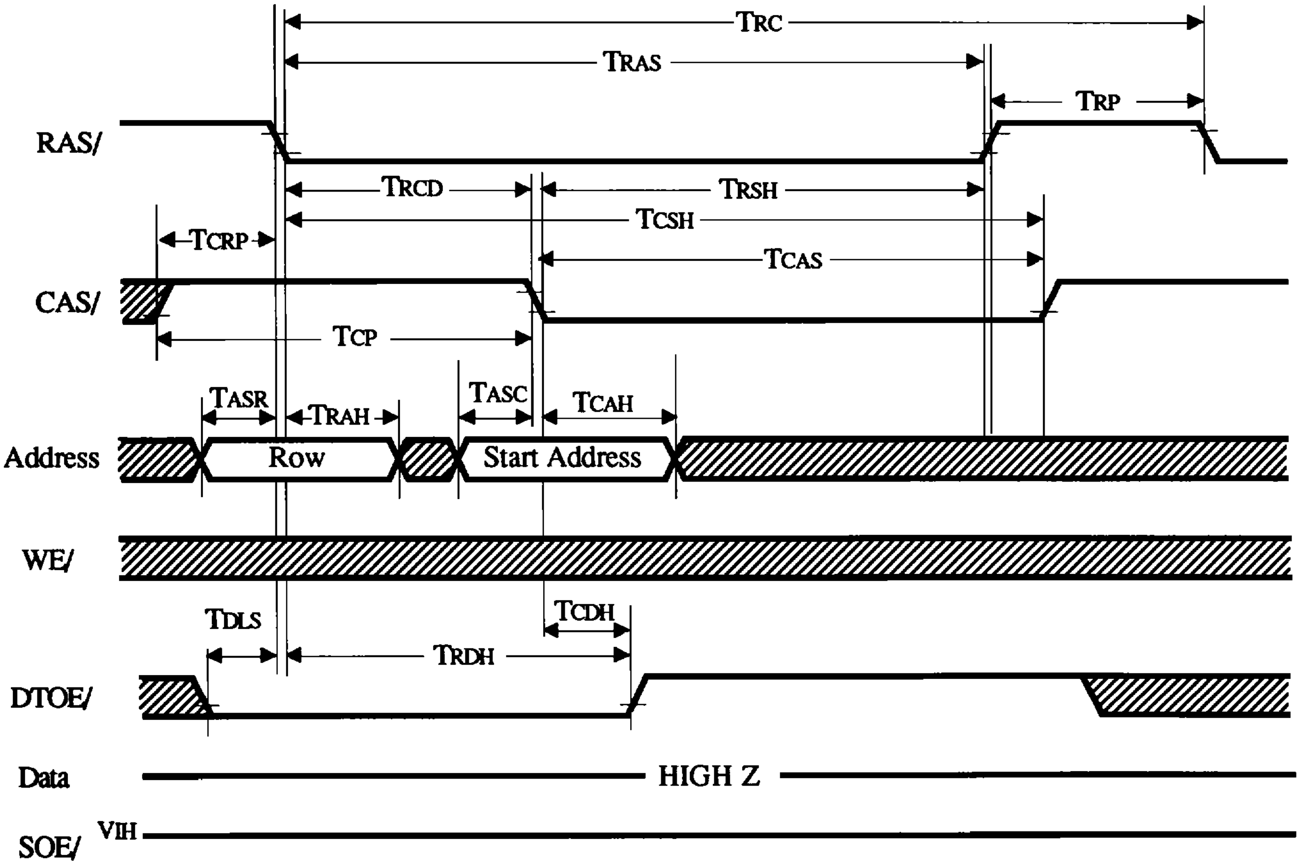


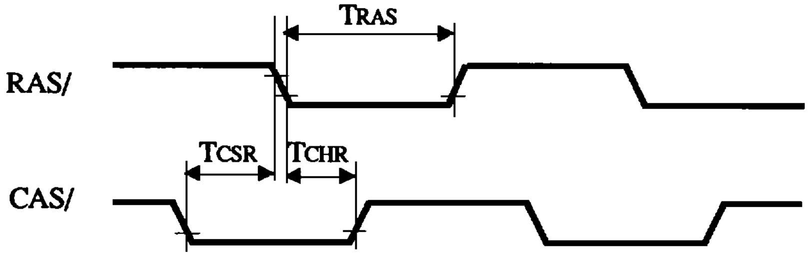
Frame Buffer Page Mode Write Cycle Timing



Frame Buffer Transfer Cycle Timing

65525 AC TIMING CHARACTERISTICS - FRAME BUFFER REFRESH TIMING

Symbol	Parameter	Notes	Min	Typ	Max	Units
T_{CHR}	RAS to CAS delay	2Td = 50 ns @ 40MHz	2Td– 5	–	2Td+ 5	ns
T_{CSR}	CAS to RAS delay	Td = 25 ns @ 40MHz	Td– 5	–	Td+ 5	ns
T_{RAS}	RAS pulse width	5Td = 125 @ 40 MHz	5Td– 5	–	5Td + 5	ns

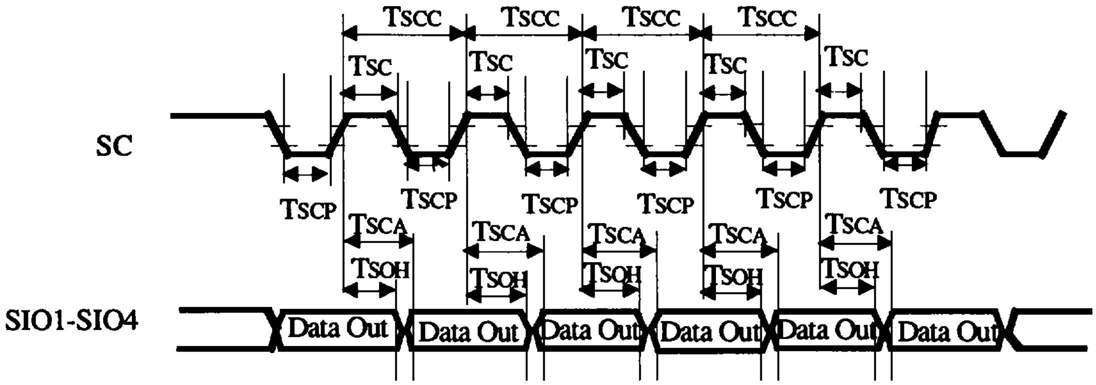


Frame Buffer VRAM CAS-Before-RAS (CBR) Refresh Cycle Timing

65525 AC TIMING CHARACTERISTICS - FRAME BUFFER VRAM SERIAL PORT TIMING

Symbol	Parameter	Min	Typ	Max	Units
T_{SCC}	Sequencer Clock	-	–	100	ns
T_{SC}	SC Cycle Time	–	0.45 T_{SCC}	–	nS
T_{SCP}	SC Precharge Time	–	0.45 T_{SCC}	–	nS
T_{SCA}	Access Time from SC	–	–	50	nS
T_{SOH}	Serial Output Hold Time	5	–	–	nS

Note: These specifications are based on the dot clock rate. The maximum dot clock rate for frame buffer operation is 40 MHz (Td = 25 ns).



Frame Buffer VRAM Serial Port Read Cycle Timing

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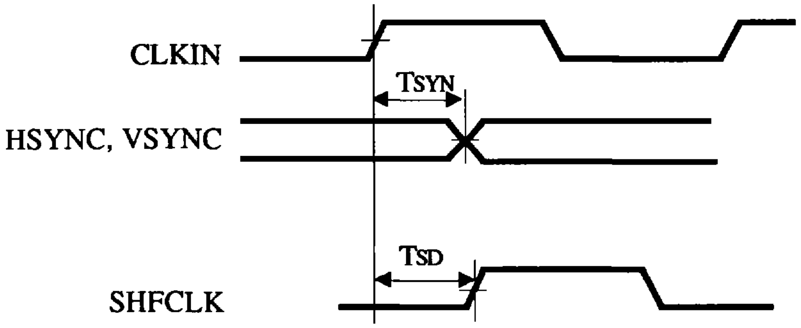
65525 AC TIMING CHARACTERISTICS - CRT VIDEO TIMING

Symbol	Parameter		Min	Max	Units
T_{SYN}	HSYNC, VSYNC delay from CLKIN		-	50	nS
T_{SYN}	HSYNC, VSYNC delay from CLKIN (3.3V)		-	80	nS
T_{SD}	CLKIN to SHFCLK delay		-	30	nS
T_{SD}	CLKIN to SHFCLK delay (3.3V)		-	50	nS

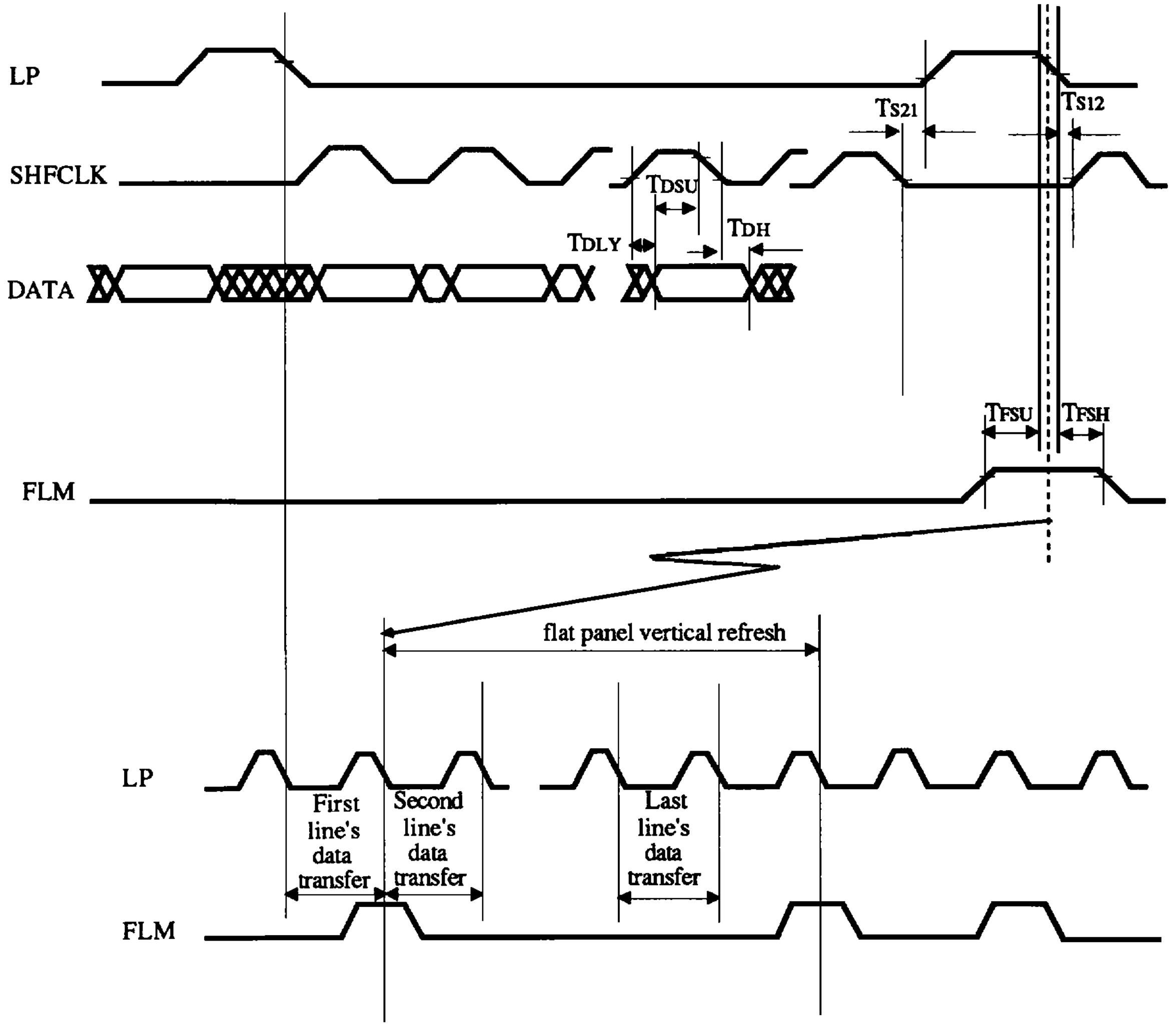


CRT Video Data and Control Signal timing

Note: Unless otherwise specified, specifications above apply to both 5V and 3.3V operation.
Electrical specifications contained herein are preliminary and subject to change without notice.

65525 AC TIMING CHARACTERISTICS - FLAT PANEL VIDEO TIMING

Symbol	Parameter		Min	Max	Units
T_{DSU}	Panel data setup to SHFCLK		5	–	nS
T_{DH}	Panel data hold to SHFCLK		10	–	nS
T_{DLY}	Panel data delay from SHFCLK		10	–	nS
T_{S12}	SHFCLK allowance time from LP		Tc	–	nS
T_{S21}	LP allowance time from SHFCLK		Tc	–	nS
T_{FSU}	FLM setup time		8 Tc	–	nS
T_{FSH}	FLM hold time		8 Tc	–	nS



Flat Panel Video Data and Control Signal timing

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