TDK SEMICONDUCTOR CORP.

5511 DTD

Digital TV Downconverter IC

Target Information

January 1999

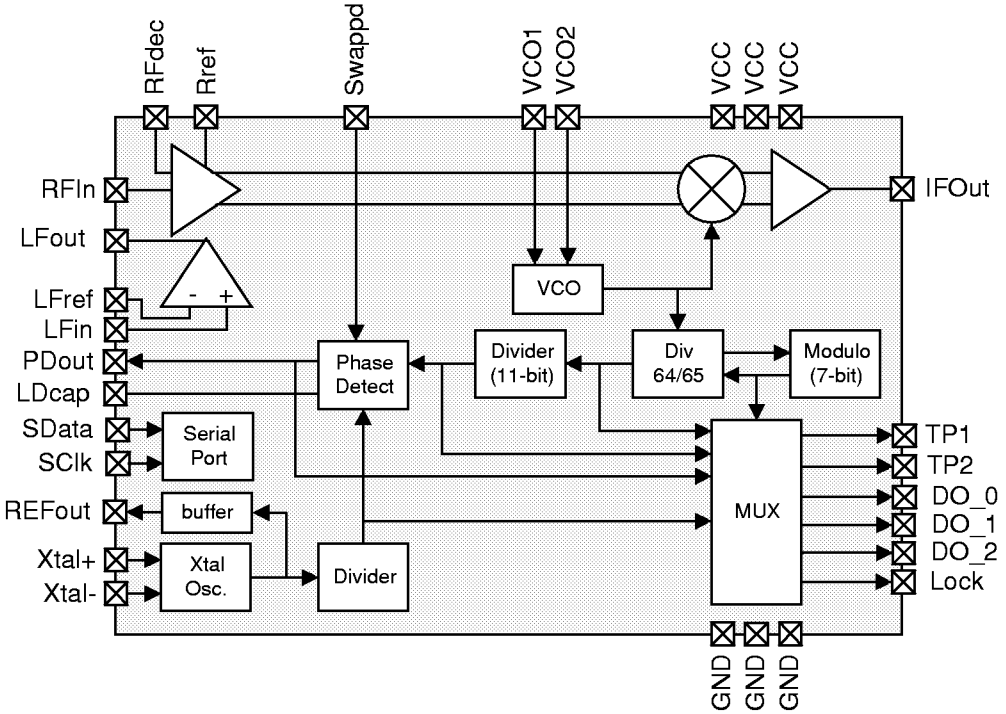
DESCRIPTION

The 5511 is a low cost, high performance downconverter for digital communication applications. The device accepts an RF input signal in the range of 900 to 1400 MHz and downconverts to an intermediate frequency of 20 to 100 MHz. The device includes an integrated frequency synthesizer and VCO. Typical applications for the 5511 include CATV set-top converters and digital terrestrial television receivers.

FEATURES

- **Wideband input**
- **Integrated frequency synthesizer**
  - **800 to 1380 MHz center frequency**
  - **Maximum phase noise -86dBc @ 10 kHz**
- **I2C serial port control**
- **5 volt operation**
- **32 Lead TQFP package**

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The 5511 is a complete down conversion receiver IC that includes an amplifier, mixer, integrated frequency synthesizer, and serial port.

RF Input: The device accepts an AC coupled, RF input within the range of 900 MHz to 1400 MHz. The circuit includes decoupling pin *RFdec*, which should be connected through high quality 100pF capacitors to ground. The device is designed to be compatible with a 75-ohm source.

Down Conversion: The device includes a mixer that allows the RF input to be down converted to an IF frequency of 20 to 100 MHz. The IF frequency is determined by the difference between the frequency of the input signal and the center frequency of the VCO.

Frequency Synthesizer

The 5511 includes an integrated frequency synthesizer that can be tuned over a range of 800 MHz to 1480 MHz. The external tank circuit determines actual tuning range. Connections for VCO tank circuit are pins *VCO1* & *VCO2*. The typical tank circuit consists of a series inductor, 2 RF chokes, 2 resistors for bias, 2 capacitors, and a varactor diode. See application drawing for topology and recommended values.

PLL Description: The integrated phase-locked loop accepts a clock input from an external crystal (or other clock source) and compares that signal to the output of the VCO to adjust the frequency. The device includes a reference divider, a feedback divider, and a variable modulus prescaler counter. These programmable functions are addressed through a standard two-wire serial interface. The *Lock* pin output is high when the loop is locked.

The loop filter amplifier is integrated. Non-inverting input pin is *LFin*. The inverting input is pin *LFref*, and is biased to ½ the supply voltage. Output pin is *LFout*. The filter elements are external allowing the user maximum flexibility to meet system requirements. The *LFout* pin typically drives an external transistor that supplies voltage to the varicap diode of the VCO tank circuit. See application drawing for topology and recommended values.

The phase detector compares the reference signal to the selected VCO. It's output is available at the *PDout* pin, and is typically connected to the loop filter amp *LFin* pin. The phase detector output increases when the selected VCO frequency/phase is greater than the reference for normal operation. The phase detector circuit features a swap polarity function. Connect the the *Swappd* pin to ground for normal operation. When the *Swappd* pin is high, the sense is opposite. (The phase detector output decreases when the VCO frequency/phase is greater than the reference.)

A Lock Detect circuit indicates when the loop is locked. The *LDcap* pin determines the set point, and it typically 1.0 nF.(TBD) The *Lock* pin is high when the loop is locked.

Reference Oscillator: A crystal can be connected across the *XTAL+/XTAL-* pins of the device to drive the internal crystal oscillator. The 5511 can also be driven by an external reference source with a frequency of 20 MHz or less. In this case, a single-ended clock is AC coupled into the *XTAL+* pin of the device with the *XTAL-* pin left open. The output of the oscillator is also available from the *Refout* pin. It is designed to provide reference input to the 5510 *XTAL+* pin or another PLL function IC, helping reduce external component count.

Reference Divider: The output of the crystal oscillator drives a reference divider that sets the update frequency of the PLL. The output of this divider serves as the frequency reference input for the phase detector circuit. The update frequency (f_{UPD}) of the PLL is determined by the frequency of the reference source (f_{REF}) and the value set in the 10-bit reference divider (RD), according to the following equation:

$$f_{UPD} = f_{REF}/RD$$

Register 0 contains the lower 8-bits (RD0-RD7) of the RD value. Bits 0 and 1 of Register 1 contain RD8 and RD9 (MSB) of the RD value.

Modulus Counter: The modulus counter (MC) is a 7-bit counter that is used to control the divide-by-64/65 prescaler. The value programmed into the MC register will determine how many cycles the prescaler will count to 65 before switching to the 64 count.

Feedback Counter: The feedback counter (FC) is an 11-bit counter that is used to divide the clock input from the VCO to match the PLL update frequency, f_{UPD}. When the feedback counter reaches the terminal count, a pulse is generated. This pulse resets the feedback counter and the modulus counter. The pulse is also provided to the phase detector for comparison to the frequency reference.

Frequency Programming: The PLL operating frequency (f_{PLL}) is determined by programming counter values for the reference divider (RD), the feedback counter (FC), and the modulus counter (MC) and by setting the VCO center frequency through the VCF register.

After the user determines the desired PLL operating frequency and the phase detector update frequency (f_{UPD}), the feedback counter (FC) and the modulus counter (MC) values can be determined. The first step is to determine the total count (TC) that is required to divide the PLL frequency down to the update frequency:

$$TC = f_{PLL} / f_{UPD}$$

Now divide the TC value by the lower count value of the prescaler to get the feedback counter (FC) value. When the result is a whole number, FC is equal to that number and the modulus counter (MC) is equal to zero (0). If there is a remainder, then MC is equal to that remainder:

FC = (whole number value of TC/LCV), and

MC = remainder of TC/LCV, where

LCV = lower count value of prescaler

Example: If f_{PLL} is 980 GHz, and the phase detector update frequency (f_{UPD}) is 20 kHz, then TC is:

$$TC = (9.8 \times 10^8)/(2.0 \times 10^4) = 4.9 \times 10^4$$

The feedback count (FC) is now determined by dividing 4.9×10^4 by the lower count of the prescaler, 64:

$(4.9 \times 10^4)/64 = 765$ remainder 40, then

FC = 765, and MC = 40

Digital Outputs

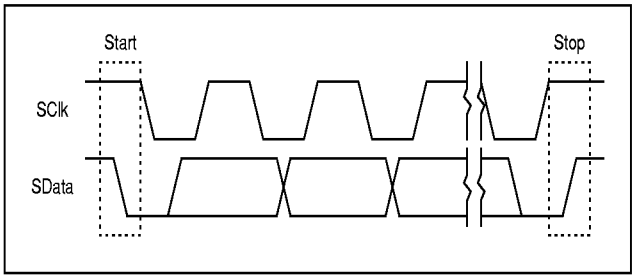
The device includes several programmable digital outputs (*DO_0, DO_1,* and *DO_2).* These pins are general purpose open-collector outputs decoded by 2 bits in serial port register, DIG1 = Register 3 bit 7 & DIG0 = Register 1 bit 7. The outputs are programmed per the following table. External pull-up resistors are required for normal operation.

DIG1	DIG0	Output Low
0	0	DO_0
0	1	DO_1
1	0	DO_2
1	1	none

Serial Port Definition

A simple two-wire serial port that is compatible with the inter-IC (I^2C) bus controls internal functions of the device. The address of the device is 1100100. The serial port uses a clock input (*SClk*) that is driven by the bus master and a bi-directional data input (*SData*) to perform all data transfers.

Data Transfers: The device is enabled for a data transfer when the *SData* pin is driven from HIGH to LOW by the bus master while the *SClk* pin is HIGH. The data transfer is complete when the bus master drives the *SData* pin from LOW to HIGH while the *SClk* pin is HIGH.



The first eight bits of data clocked into the device are decoded to determine if a valid address has been received. The first seven bits of information are the address with the eighth bit indicating whether the cycle is a read (bit is HIGH) or a write (bit is LOW). If the address is valid for this device, on the falling *SClk* edge of the eighth bit of data, the device will drive the *SData* pin low and hold it LOW until the next falling edge of the *SClk* pin to acknowledge the address transfer. Once a valid address is detected the device will continue to transmit or receive data until the bus master has issued a stop.

Write Operation: When the read/write bit (bit 8) is LOW and a valid address is decoded, the device will receive data from the *SData* pin and latch the data into the internal registers. The write data register allocation is given in the Serial Port Register Table. The device will continue to latch data into the registers until a stop condition is detected or the last register has been loaded. After each byte of data written, the device generates an acknowledge.

Test Points

The 5510 provides a pair of programmable test pins (*TP1, TP2*) that allow monitoring of internal PLL signals. These test pins are CMOS outputs.

Under normal operation, these pins should be left open (no external load) to reduce power consumption and internal noise. The source signals for each test pin are determined by setting bits in serial port Register 1 as follows:

TPS 1	TPS 0	TP1 Source	TP2 Source
0	0	Feedback divider	Reference divider
0	1	Prescaler output	Modulo output
1	0	PD pump up	PD pump down
1	1	Not used	Not used

Serial Port Register Table (Base Address = 11000100)

REGISTER	FUNCTION	BITS	DESCRIPTION
0	Reference Divider	00000000	Bits 0-7 of the 10-bit reference divide value (RD)
1	Reference Divider	xxxxxx00	LSB = bit 8- 9 of the 10-bit reference divide value (RD)
1	Feedback Count	xxx000xx	Bits 8, 9, 10 of the 10-bit feedback divide value (FD)
1	Test Point Select	x00xxxxx	Controls signal routing to test pins TP1 and TP2
1	Digital Output Select 0	0xxxxxxx	Controls signal routing to pins DO_0, DO_1, DO_2
2	Feedback Count	00000000	Bits 0-7 of the 10-bit feedback divide value (FD)
3	Modulus Count	x0000000	Bits 0-6 of the 7-bit modulus counter value (MC)
3	Digital Output Select 1	0xxxxxxx	Controls signal routing to pins DO_0, DO_1, DO_2

Register Bit Allocation

Register 0:

RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

RD0 = LSB of Reference Divider

Register 1:

DIG0	TPS1	TPS0	FC10	FC9	FC8	RD9	RD8

RD9 = MSB of Reference Divider (RD) value
FD10 = MSB of Feedback Count (FC) value
TPS0 & TSP1 = Testpoint control bits
DIG0 = Digital control bit 0

Register 2:

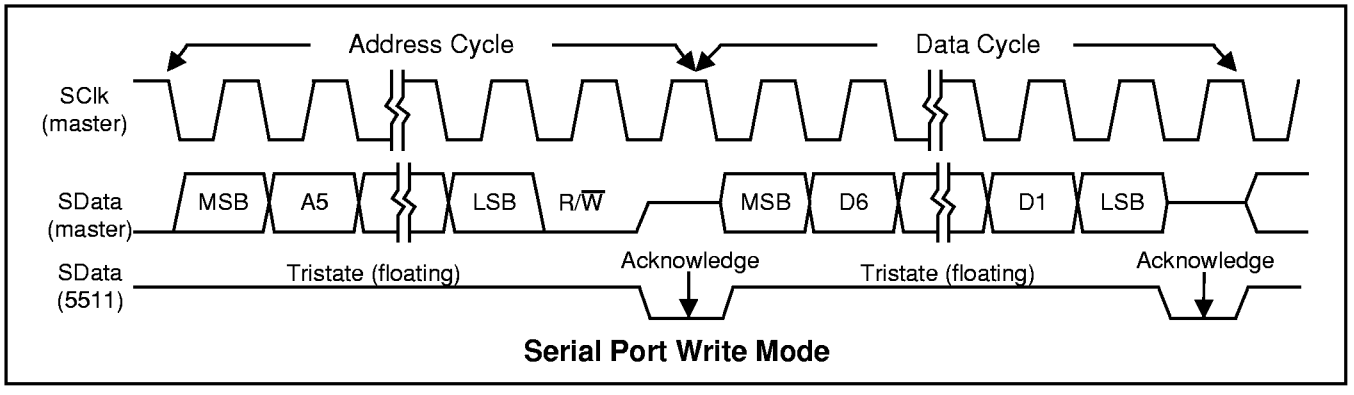
FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0

FC0 = LSB of Feedback Count (FC) value

Register 3:

DIG1	MC6	MC5	MC4	MC3	MC2	MC1	MC0

MC0 = LSB of Modulus Count (MC) value
MC6 = MSB of Modulus Count value
DIG1 = Digital control bit 1



Serial Port Write Mode

PIN DESCRIPTIONS (Pins marked N/C should be left unconnected during normal use)

NAME	TYPE	DESCRIPTION
Analog Pins:		
PDout	O	Phase detector output: This pin connects to the loop filter interface for the tank circuits.
LFin+	I	Loop filter amp noninverting input.
LFref	I	Loop filter amp inverting input. It's biased to ½ power supply.
LFout	O	Loop filter amp output.
IFOut	O	IF Output: This pin is the intermediate frequency output from the device.
RFIn	I	RF Input: This input is the RF signal that will be upconverted. The pin is AC coupled to a 75-ohm source. The input frequency range is 50 MHz to 860 MHz.
RFdec	-	RF input amplifier decoupling input pin. A high quality 100 pF capacitor resistor should be connected between this pin and analog ground.
Rref	-	Current source load pin. A 120 k ohm resistor should be connected between this pin and ground.
VCO1	-	VCO tank circuit connection #1.
VCO2	-	VCO tank circuit connection #2.
LDcap	-	Phase detector bias pin used to determine Lock Detect response. Connect a capacitor to ground.
Refout	O	Crystal oscillator buffered output.
Xtal+/-	-	Crystal Inputs: These pins are the input for an external frequency reference. A crystal can be connected across these pins, or a clock can be AC coupled into the *Xtal+* pin while leaving the *Xtal-* pin open.
Digital Pins:		
SClk	I	Serial Clock Input: This input pin accepts a serial port clock signal. The rising edge of the clock signal is used to shift data into the device.
SData	I	Serial Data Input: This input pin accepts serial port data. Data on this pin should be valid and stable when the *SClk* signal is HIGH. Data can change when the SCLK pin is LOW.
Swappd	I	Swap phase detector polarity. When low, the phase detector output increases when the selected VCO frequency/phase is greater than the reference.
DO_0	O	Digital Output 0: This pin is an open-collector output that is controlled by serial port register. (Not available in all device packages.)
DO_1	O	Digital Output 1: This pin is an open-collector output that is controlled by serial port register. (Not available in all device packages.)
DO_2	O	Digital Output 2: This pin is an open-collector output that is controlled by serial port register. (Not available in all device packages.)
Lock	O	PLL Lock Signal: This pin is HIGH when the loop is phase locked, LOW when it's not.
TP1/2	O	Test Point Outputs: These pins are test points that allow internal signals to be monitored. These pins are CMOS outputs. In normal operation, these pins should be left open.

PIN DESCRIPTIONS(cont.)

NAME	TYPE	DESCRIPTION
Power/Ground Pins:		
VCC	-	+5 VDC power input
GND	-	Ground

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

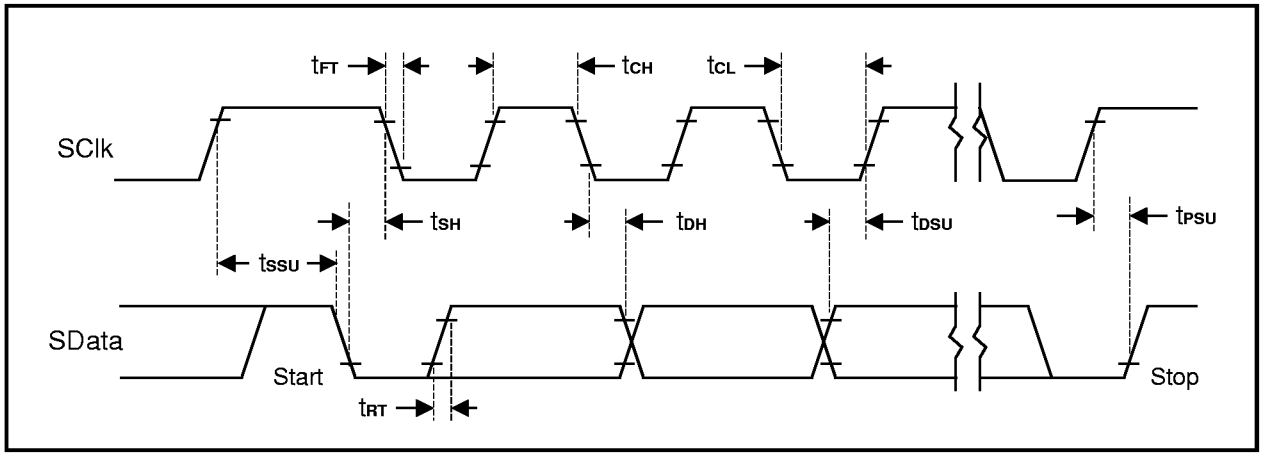
PARAMETER	RATING	UNIT
Storage temperature	-55 to 150	°C
Junction operating temperature	+110	°C
Positive supply voltages	Gnd > 0.3; VCC < 6	V
Voltage applied to any pin	-0.3V to VCC+0.3	V

TARGET SPECIFICATIONS

Unless otherwise specified: 0° < Ta < 70° C; positive power supplies VCC = +5.0 V +/-5%.

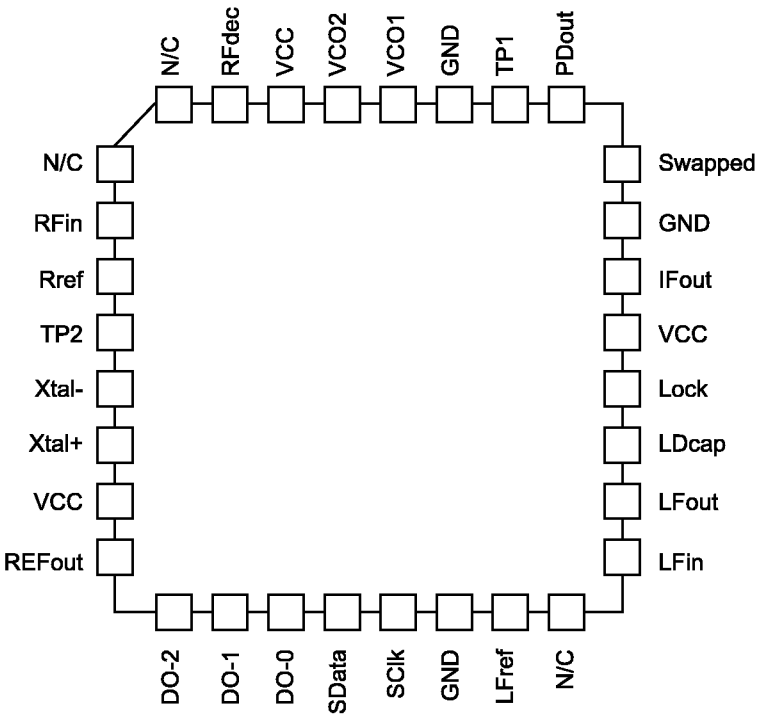
PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Operating Characteristics					
Power dissipation	All outputs loaded		350		mW
PSRR	f_{in} = 100 Hz, 0.3 Vpp on VCC	40			dB
Digital I/O Characteristics (*SClk, SData, Lock, Swappd*)					
High level input voltage		0.7*VCC		VCC+0.3	V
Low level input voltage		GND-0.3		0.3*VCC	V
High level input current	Vin = Vcc - 1.0V	-10		10	µA
Low level input current	Vin = 1.0V	-10		-10	µA
Digital output sink current	(*DO_0, DO_1, DO_2*)		1.0		mA
Digital output fall time	(*DO_0, DO_1, DO_2*) R_L = 10k C_L = 15 pF		20		nsec
Receiver Characteristics - Unless otherwise noted, input is AC coupled from a 75 Ω source.					
Input impedance	*RFIn+/-*		75		Ω
Input return loss	(Reference plane at IC input pin)	8.0	10.0		dB
Input frequency range		900		1400	MHz
Conversion gain	(RFIn to Ifout)	19.0		22.0	dB
Noise figure			18		dB
3rd order IIP	V_{RFI}n = min, AGC = max gain	53			dBmV
LO leakage	Measured at *RFIn*	20			dBmV
VCO Characteristics					
Tuning range	Set via external components	800		980	MHz
Phase noise	10 kHz offset			-86	dBc/Hz

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baseband Characteristics					
IFOut output impedance	(Reference plane at IC input pin)		75		Ω
IFOut output amplitude	(maximum output level)		50		dBmV
Output return loss	(Reference plane at IC input pin)	8.0	10.0		dB
Serial Port Timing (reference timing diagram below)					
SClk Input Frequency				400	kHz
SClk LOW time (t_{CL})		1.3			usec
SClk HIGH time (t_{CH})		0.6			usec
Rise time (t_{RT})	*SClk* and *SData*			300	nsec
Fall time (t_{FT})	*SClk* and *SData*			300	nsec
Data set-up time* (t_{DSU})	*SData* change to *SClk* HIGH	100			nsec
Data hold time* (t_{DH})	*SClk* LOW to *SData* change	0			nsec
Start set-up time (t_{SSU})		0.6			usec
Start hold time (t_{SH}		0.6			usec
Glitch rejection	maximum pulse on *SClk* and/or *SData*			50	nsec
* These specifications also apply to an acknowledge generated by the device.					



PACKAGE PIN DESIGNATIONS

(Top View)



ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
5511 DTD Digital TV Downconverter IC	Consult factory	5511-CGT

TDK Semiconductor Corp., 2642 Michelle Dr., Tustin, CA 92780, (714) 508-8800, FAX (714) 508-8877, http://www.tsc.tdk.com

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