MC68184

Technical Summary

Broadband Interface Controller

The MC68184 broadband interface controller (BIC) is a high-performance interface device for use with the MC68824 token bus controller (TBC) to implement the digital portion of the physical layer of a broadband IEEE 802.4 token bus node. The BIC manipulates both data and control for RF transmitter circuitry and RF receiver circuitry. The CMOS BIC supports data rates up to 10 Mbps using a duo-binary modulation technique. The BIC is available in a 40-pin plastic dual-in-line package.

The MC68184 provides the following features:

- Implements Digital Portion of IEEE 802.4 Broadband Physical Layer
- Provides Station Management for Physical Layer
- Supports Serial Data Rates up to 10 Mbps
- 20 Lines for Receiver/Transmitter Control with 13 User-Defined Outputs
- Includes Ability to Scramble and Descramble Data
- Kicker Insertion and Deletion Capability
- Two Loopback Modes
- Interfaces via a Standard Serial Interface to MC68824 TBC
- Able to Connect Either Directly to TBC or to TBC through an Arbitrary Length of Cable

This document contains information on a new product. Specifications and information herein are subject to change without notice.

GENERAL DESCRIPTION

The BIC performs the digital functions of the physical layer when implementing a broadband token bus node as shown in Figure 1. The modem side of the BIC provides data and control for the RF transmitter/receiver circuitry. A standard serial interface is used to connect the BIC to the MC68824 TBC. The TBC performs the media access control (MAC) function.

The functional block diagram of the BIC is shown in Figure 2. The encoder accepts data from the serial interface using the TXCLK signal and outputs duobinary signals corresponding to the coding rules listed in Table 1.

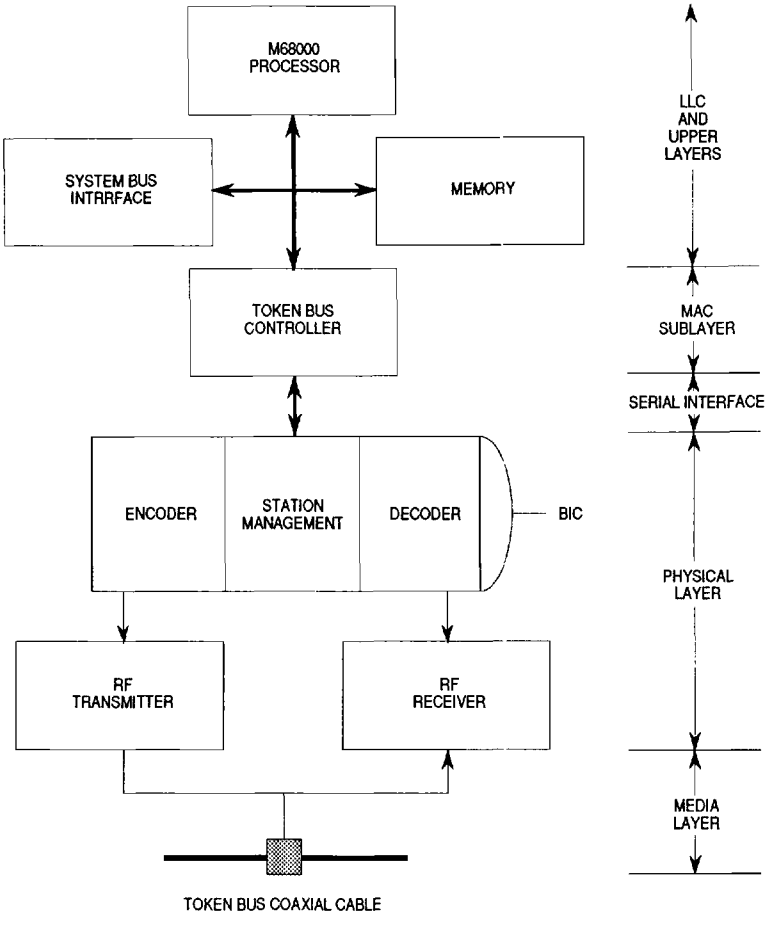


Figure 1. Token Bus Node

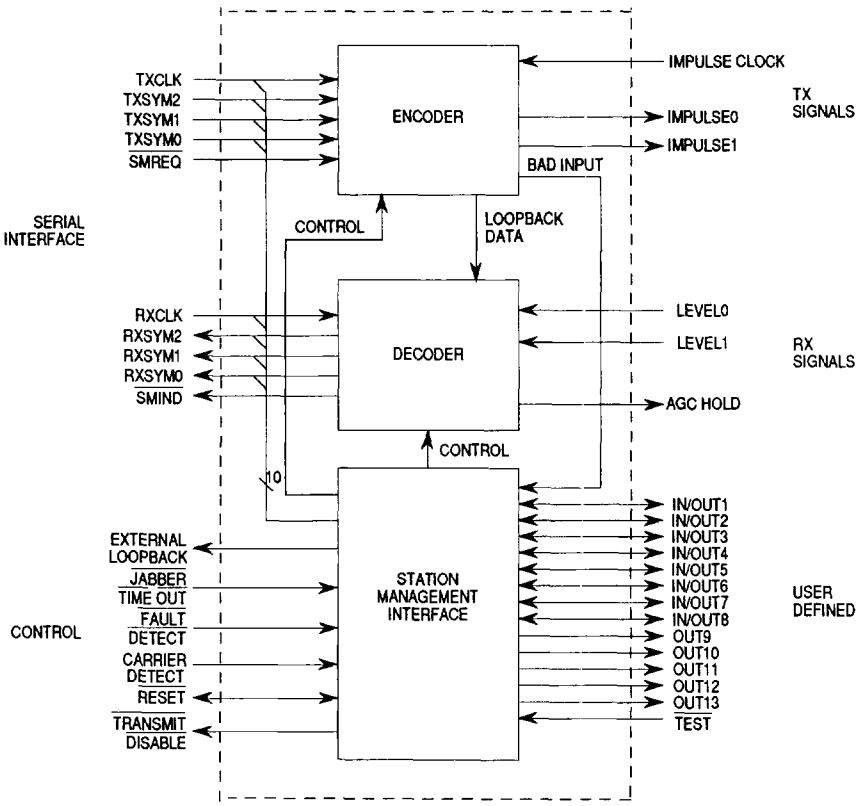


Figure 2. BIC Functional Block Diagram

8

Table 1. IMPULSE0 and IMPULSE1 Encoding

IMPULSE0	IMPULSE1	Duo-Binary Encoder	
		Enabled	Disabled
0	0	0	Zero
0	1	−2	One
1	0	+2	Nondata
1	1	Silence	Silence

NOTE: Duo-Binary Encoding Defined by IEEE 802.4 — 1985 (Table 14-1)

The decoder accepts the encoded receiver levels from the RF receiver circuitry and outputs data to the TBC using the serial interface. LEVEL0 and LEVEL1 signals are inputs to the decoder according to the encoding listed in Table 2.

Table 2. LEVEL0 and LEVEL1 Encoding

LEVEL0	LEVEL1	Encoding
0	0	Data Zero
0	1	Data One
1	0	2–0 Nondata
1	1	2–4 Nondata

The station management interface accepts $\overline{\text{JABBER}}$ $\overline{\text{TIME}}$ $\overline{\text{OUT}}$, $\overline{\text{FAULT}}$ $\overline{\text{DETECT}}$, and CARRIER DETECT signals. $\overline{\text{TRANSMIT}}$ $\overline{\text{DISABLE}}$ and $\overline{\text{RESET}}$ are bidirectional signals which can be inputs from external circuitry or generated by the BIC after receiving commands from the TBC. EXTERNAL LOOPBACK is an output signal from the BIC. In addition, the station management interface accepts commands from the TBC over the serial interface and uses them to control the operation mode of the encoder and decoder and the state of control lines IN/OUT1–IN/OUT8 and output lines OUT9–OUT13.

SIGNAL DESCRIPTION

The BIC signals can be broken into several groups including the serial interface, RF transmitter signals, RF receiver signals, and control signals. Of the 20 control signals, 13 are user-defined signals.

SERIAL INTERFACE

The serial interface is composed of the physical data request channel and the physical data indication channel.

Physical Data Request Channel

Five signals comprise the physical data request channel: TXCLK, $\overline{\text{SMREQ}}$, TXSYM2, TXSYM1, and TXSYM0. TXSYM2, TXSYM1, and TXSYM0 are multiplexed and have different meanings depending on the mode selected by the state of $\overline{\text{SMREQ}}$.

TXCLK — The transmit clock can be from 1–10 MHz. TXSYM2, TXSYM1, TXSYM0, and $\overline{\text{SMREQ}}$ are synchronized to TXCLK. The IEEE 802.4 standard for broadband allows 1, 5, or 10 MHz clocks.

$\overline{\text{SMREQ}}$ — $\overline{\text{SMREQ}}$ indicates if the physical layer is in the media access control (MAC) mode ($\overline{\text{SMREQ}} = 1$) or in the station management (SM) mode ($\overline{\text{SMREQ}} = 0$) of operation.

TXSYM2, **TXSYM1**, and **TXSYM0** — In SM mode, TXSYM2, TXSYM1, and TXSYM0 have the encoding listed in Table 3.

Table 3. Request Channel SM Mode Encoding ($\overline{\text{SMREQ}} = 0$)

State	TXSYM2	TXSYM1	TXSYM0
Reset	1	1	1
Disable Loopback	1	0	1
Enable Transmitter	0	1	1
Serial SM Data/Idle	0	0	0/1

In SM mode, the TBC can pass commands to the BIC. In addition to the three standard commands of reset, disable loopback, and enable transmitter, user-generated commands can be passed to the BIC to control or monitor the RF circuitry.

In MAC mode, TXSYM2, TXSYM1, and TXSYM0 have the encoding listed in Table 4.

Table 4. Request Channel MAC Mode Encoding ($\overline{\text{SMREQ}}$ = 1)

Symbol	TXSYM2	TXSYM1	TXSYM0
Zero	0	0	0
One	0	0	1
Nondata	1	0	*
Pad–Idle	0	1	*
Silence	1	1	*

Where:
Zero is the logical state zero.
One is the logical state one.
Nondata is a delimiter flag and is always requested in pairs.
Pad–Idle is one symbol of preamble/ interframe idle.
Silence is silence or pseudo-silence.
*Don't Care

Physical Data Indication Channel

Five signals comprise the physical data indication channel: RXCLK, $\overline{\text{SMIND}}$, RXSYM2, RXSYM1, and RXSYM0. RXSYM2, RXSYM1, and RXSYM0 are multiplexed and have different meanings depending on the state of $\overline{\text{SMIND}}$.

RXCLK — The receive clock can be from 1–10 MHz. RXSYM2, RXSYM1, RXSYM0, and $\overline{\text{SMIND}}$ are synchronized to RXCLK. The IEEE 802.4 standard for broadband networks allows 1, 5, or 10 MHz clocks.

$\overline{\text{SMIND}}$ — $\overline{\text{SMIND}}$ indicates whether the physical layer is in MAC mode ($\overline{\text{SMIND}}$ = 1) or SM mode ($\overline{\text{SMIND}}$ = 0) of operation. When in MAC mode of operation, RXSYM2, RXSYM1, and RXSYM0 are encoded indications of data reception. When in SM mode of operation, RXSYM2, RXSYM1, and RXSYM0 are encoded to confirm response to management commands.

8

RXSYM2, RXSYM1, and **RXSYM0** — In SM mode, the encoding for RXSYM2, RXSYM1, and RXSYM0 is shown in Table 5.

Table 5. Indication Channel SM Mode Encoding ($\overline{\text{SMIND}}$ = 0)

State	RXSYM2	RXSYM1	RXSYM0
NACK (Nonacknowledgment)	1	0	*
ACK (Acknowledgment)	0	1	*
IDLE	0	0	1
Physical Layer Error	1	1	1

*Indicates RXSYM0 contains the SM RX data when responding to a serial data command.

The encoding of RXSYM2, RXSYM1, and RXSYM0 in MAC mode is shown in Table 6.

Table 6. Indication Channel MAC Mode Encoding ($\overline{\text{SMIND}}$ = 1)

Symbol	RXSYM2	RXSYM1	RXSYM0
Zero	0	0	0
One	0	0	1
Nondata	1	0	0
Silence	1	1	1

Where:
Zero is the logical state zero.
One is the logical state one.
Nondata is a delimiter flag. In the absence of errors, nondata will always be present in pairs.
Silence is silence or pseudo-silence.

RF TRANSMITTER SIGNALS

The following paragraphs describe the RF transmitter signals.

IMPULSE0 and IMPULSE1

IMPULSE0 and IMPULSE1 are output signals from the BIC encoder and pass duo-binary signals to the RF transmitter circuitry with the meanings given in Table 1.

IMPULSE CLOCK

IMPULSE CLOCK is an input signal which must be the same frequency as the transmit clock (TXCLK) and the receive clock (RXCLK).

RF RECEIVER SIGNALS

The following paragraphs describe the RF receiver signals.

LEVEL0 AND LEVEL1

LEVEL0 and LEVEL1 are input signals to the BIC decoder from the RF receiver circuitry. These signals are decoded by the BIC decoder as shown in Table 2.

AGC HOLD

The automatic gain control (AGC) HOLD is low whenever CARRIER DETECT is low. If CARRIER DETECT is high, then AGC HOLD will be high whenever a start delimiter is found on LEVEL0 and LEVEL1. A start delimiter consists of the following sequence of eight bits: 2-0 or 2-4, 2-0 or 2-4, 0, 2-0 or 2-4, 2-0 or 2-4, 0, 0, 0. When CARRIER DETECT is high, AGC HOLD will be low if one of the following occurs: 24 of the same inputs are received on LEVEL0 and LEVEL1 (the encodings 2-0 and 2-4 are considered different inputs); if two, three, or four nondatas (2-0 or 2-4) are contained in bit positions 1, 2, 4, and 5 relative to the start delimiter; if the error corrector is disabled (bit 7 of register 1 is set) and a nondata in bit positions 3, 6, 7, or 8 not belonging to a kicker is present; if the descrambler disable bit is set (bit 4 of register 1) and a kicker is present; if a reset occurs.

CONTROL SIGNALS

The BIC has 20 control signals, 13 of which are user-defined.

$\overline{\text{RESET}}$

$\overline{\text{RESET}}$ is a bidirectional signal. When $\overline{\text{RESET}}$ is driven low, the BIC will reset. $\overline{\text{RESET}}$ must be driven low at power-up and held low for at least 10 clock cycles after all clocks become stable. A pullup resistor (>150 kΩ) is provided to drive this pin to the inactive state. In addition, when the BIC receives a reset command from the TBC, it will drive $\overline{\text{RESET}}$ low for as long as the reset command is asserted.

$\overline{\text{JABBER TIME OUT}}$

The $\overline{\text{JABBER TIME OUT}}$ pin is an input to the BIC from the external jabber timer circuitry. When $\overline{\text{JABBER TIME OUT}}$ is driven low, the BIC will drive IMPULSE0 and IMPULSE1 high (silence state), drive $\overline{\text{TRANSMIT DISABLE}}$ and $\overline{\text{SMIND}}$ low, and drive RXSYM2, RXSYM1, and RXSYM0 high. These pins will continue in these states until a reset is received by the BIC. The reset can occur by either driving the $\overline{\text{RESET}}$ pin low or sending a reset command to the BIC. A pullup resistor (>150 kΩ) is provided to drive the $\overline{\text{JABBER TIME OUT}}$ pin to the inactive state.

CARRIER DETECT

No carrier is present when the CARRIER DETECT pin is driven low. This pin is driven by external circuitry that senses when the carrier is lost on the broadband cable. AGC HOLD will also be driven low when CARRIER DETECT is low. When CARRIER DETECT is low and the BIC is not in internal loopback mode nor in SM mode, then RXSYM2, RXSYM1, and RXSYM0 are driven high, meaning silence. If CARRIER DETECT is low and the BIC not in external loopback mode, then IMPULSE0 and IMPULSE1 are driven high, meaning silence.

$\overline{\text{FAULT DETECT}}$

The $\overline{\text{FAULT DETECT}}$ pin operates in the same manner as the $\overline{\text{JABBER TIME OUT}}$ pin. When $\overline{\text{FAULT DETECT}}$ is driven low, the BIC will drive IMPULSE0 and IMPULSE1 high, drive $\overline{\text{TRANSMIT DISABLE}}$ and $\overline{\text{SMIND}}$ low, and drive RXSYM2, RXSYM1, and RXSYM0 high. These pins will continue in these states until a reset is received by the BIC. The reset can occur by either driving the $\overline{\text{RESET}}$ pin low or sending a reset command to the BIC. An internal pullup resistor (>150 kΩ) is provided to drive $\overline{\text{FAULT DETECT}}$ to the inactive state.

EXTERNAL LOOPBACK

The EXTERNAL LOOPBACK pin is driven high if, since the last reset, bits 1 and 2 of register 1 have been set to zero and one, respectively, and a loopback disable command has not been received by the BIC from the TBC. When EXTERNAL LOOPBACK is high, the BIC is in external loopback mode.

$\overline{\text{TRANSMIT DISABLE}}$

The $\overline{\text{TRANSMIT DISABLE}}$ pin is bidirectional. $\overline{\text{TRANSMIT DISABLE}}$ is driven active low by any one of the following conditions: during a reset; after a reset until a loopback command and an enable transmitter command are received from the TBC; while TXSYM3 is low; while a physical error is being reported (RXSYM2 = 1, RXSYM1 = 1, RXSYM0 = 1, and $\overline{\text{SMIND}}$ = 0). Since a pullup resistor (>150 kΩ) is provided, $\overline{\text{TRANSMIT DISABLE}}$ can also be driven low by an external source. When $\overline{\text{TRANSMIT DISABLE}}$ is driven active low, IMPULSE0 and IMPULSE1 will be forced high (silence) unless the BIC is in external loopback mode. In external loopback mode (EXTERNAL LOOPBACK signal high), the state of $\overline{\text{TRANSMIT DISABLE}}$ does not affect IMPULSE0 or IMPULSE1.

USER-DEFINED CONTROL SIGNALS

The following paragraphs describe the user-defined control signals.

IN/OUT1–IN/OUT8

These eight independent pins are bidirectional. Register 3E contains the state of these eight pins. Each pin can be individually programmed as an output to control the RF section. As inputs, these pins can be used to monitor the RF section. Register 3F determines if these pins are inputs or outputs.

OUT9–OUT13

These five output signals are user-defined. OUT9, OUT10, and OUT11 are driven low when a reset is sent to the BIC; OUT12 and OUT13 are driven high when a reset is received by the BIC. These outputs can be used to control the RF section as required.

BIC REGISTERS

Five registers are present in the BIC. All registers are read/write except register 0, which is a read-only register.

REGISTER 0

Register 0, an 8-bit, read-only register, has the following format:

0 — JABBER TIME OUT
This bit indicates the state of the $\overline{\text{JABBER}}$ $\overline{\text{TIME}}$ $\overline{\text{OUT}}$ pin prior to the last reset command from the TBC. When the $\overline{\text{JABBER}}$ $\overline{\text{TIME}}$ $\overline{\text{OUT}}$ pin becomes active, the BIC goes into physical error mode, which can only be exited by a reset to the BIC. Before the first reset command is given (after the BIC is powered up), this bit has no meaning.

1 — MODEM FAILURE
This bit indicates the state of the $\overline{\text{FAULT}}$ $\overline{\text{DETECT}}$ pin prior to the last reset command from the TBC. Before the first reset command is given (after the BIC is powered up), this bit has no meaning.

2 — INPUT FAILURE
This bit indicates the state of the bad input (from the encoder) prior to the last reset command from the TBC. Before the first reset command is given (after the BIC is powered up), this bit has no meaning.

3 — MEDIUM FAILURE
This bit indicates the inverse of the CARRIER DETECT pin.

4 — TRANSMIT DISABLE
This bit indicates whether the transmitter has been disabled by reset or enabled by an enable transmitter command.

5 — INTERNAL LOOPBACK
This bit indicates that the BIC is currently in internal loopback state when high.

6 — EXTERNAL LOOPBACK
This bit indicates that the BIC is currently in external loopback state when high.

7 — LOOPBACK ENABLE
This bit indicates whether loopback has been enabled or disabled. If this bit is set and neither internal loopback or external loopback is set, the BIC will only activate the $\overline{\text{TRANSMIT DISABLE}}$ pin.

REGISTER 1

Register 1, an 8-bit read/write register, has the following format:

0 — NOT USED
This bit always reads as zero.

1, 2 — LOOPBACK SELECT 1 and LOOPBACK SELECT 2
These bits determine which loopback state to go into when loopback is enabled as listed in Table 7.

Table 7. Loopback State

LOOPBACK SELECT 1	LOOPBACK SELECT 2	Mode
0	0	None
0	1	External Loopback
1	0	Internal Loopback
1	1	None

3 — SCRAMBLER DISABLE
When high, this bit disables the encoder scrambler and the kicker inserter.

4 — DESCRAMBLER DISABLE
When high, this bit disables the decoder descrambler and kicker deleter.

5 — PSEUDO-SILENCE ADDER DISABLE
When high, this bit disables the pseudo-silence adder in the encoder. The psuedo-silence adder only operates when the BIC is in internal loopback or external loopback mode.

6 — PSEUDO-SILENCE SUBTRACTER DISABLE
When high, this bit disables the pseudo-silence subtracter in the decoder.

7 — ERROR CORRECTOR DISABLE
When high, this bit disables the decoder error corrector.

REGISTER 3D

Register 3D, an 8-bit read/write register, can disable functions of the BIC as well as control the state of the five user-defined output pins. Register 3D has the following format:

0 — DUO-BINARY DISABLE
This bit disables the duo-binary encoder when high.

1 — BAD INPUT DISABLE
This bit disables the bad input detector in the encoder when high.

2 — SYNCHRONIZER DISABLE
This bit disables the encoder synchronizer when high.

3 — OUT9
This bit controls the state of OUT9. When this bit is read, it indicates the actual TTL state of OUT9 and not the requested state. A reset forces OUT9 low.

4 — OUT10
This bit controls the state of OUT10. When this bit is read, it indicates the actual TTL state of OUT10 and not the requested state. A reset forces OUT11 low.

5 — OUT11
This bit controls the state of OUT11. When this bit is read, it indicates the actual TTL state of OUT11 and not the requested state. A reset forces OUT11 low.

6 — OUT12
This bit controls the state of OUT12. When this bit is read, it indicates the actual TTL state of OUT12 and not the requested state. A reset forces OUT12 high.

7 — OUT13
This bit controls the state of OUT13. When this bit is read, it indicates the actual TTL state of OUT13 and not the requested state. A reset forces OUT13 high.

REGISTER 3E

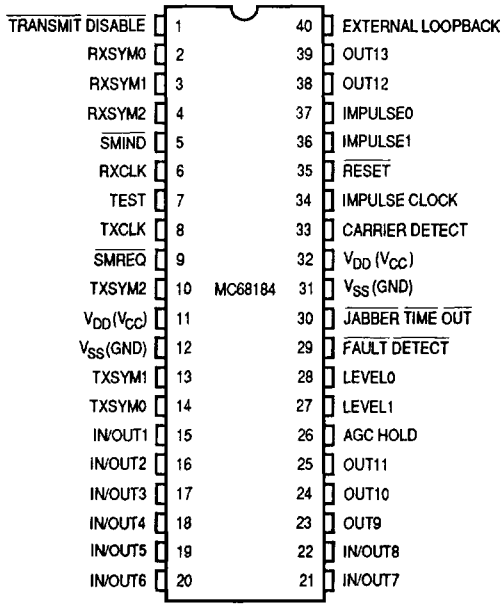
Register 3E is an 8-bit read/write register that allows the control bits to be read or written. When read, this register always indicates the actual TTL state of the IN/OUT1–IN/OUT8 pins. Writing to a bit of register 3E that has been defined as an input by the respective IN/OUT DIRECTION bit does not affect what is read. However, it will change the pin state when changed to an output. IN/OUT1–IN/OUT8 pins have internal pullup resistors.

REGISTER 3F

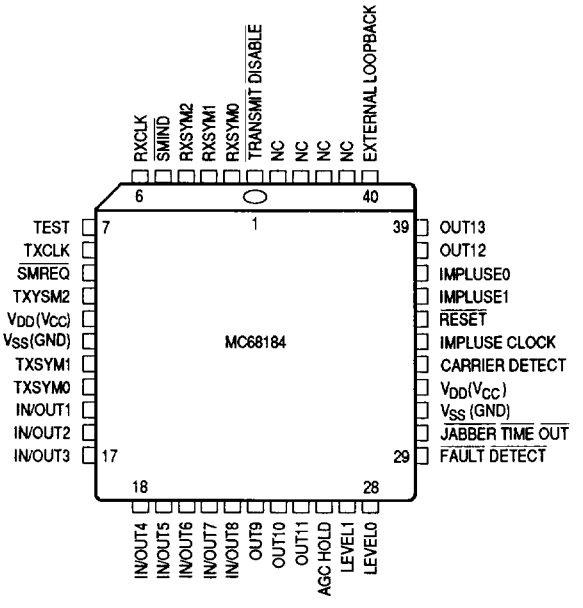
Register 3F, an 8-bit read/write register, determines if the IN/OUT pins are being read or written. Reset forces IN/OUT1–IN/OUT8 pins low, defining IN/OUT1–IN/OUT8 as inputs.

PIN ASSIGNMENTS

40-LEAD DUAL-IN-LINE PACKAGE



44-LEAD PLASTIC LEADED CHIP CARRIER



8