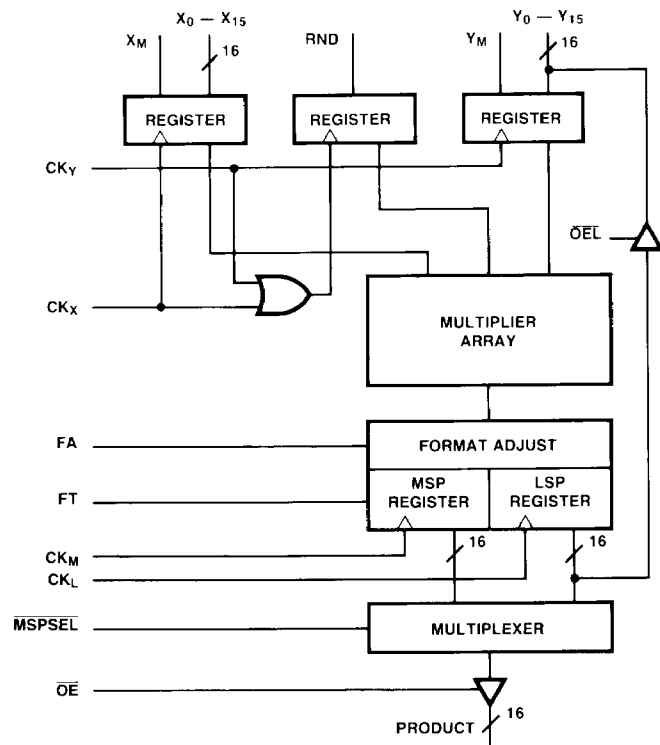


### FEATURES

- 16 x 16 MULTIPLIER — DOUBLE PRECISION PRODUCT
- HIGH SPEED MULTIPLY — 45 ns Max Clocked Multiply Time
- LOW POWER CMOS TECHNOLOGY — 550 mW Max (active) — 550  $\mu$ W Max (CMOS Standby)
- SIMPLE INTERFACE — Single 5V  $\pm$  10% Supply — TTL Compatible Inputs and Outputs
- ROUND-OFF CONTROL OF MSP TERM
- TWO'S COMPLEMENT AND UNSIGNED MAGNITUDE MULTIPLICATION
- PIN COMPATIBLE, HIGH PERFORMANCE REPLACEMENT FOR TRW MPY016HJ, AMD 29516
- AVAILABLE IN DIP OR LCC PACKAGES

### FUNCTIONAL BLOCK DIAGRAM

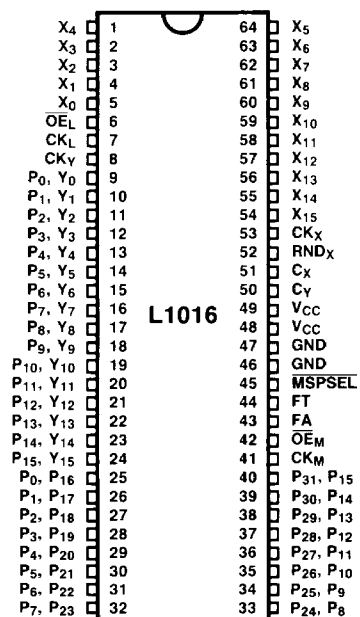


The LATTICE L1016 devices are high performance 16 x 16 bit double precision multipliers. Designed with high speed circuit techniques and a modified Booth's algorithm, the devices feature 45 ns, 65 ns, and 90 ns multiply times. These devices offer a performance upgrade and are pin compatible with industry standard multipliers like the MPY016HJ.

UltraMos™, LATTICE's high performance CMOS technology, provide the multipliers with an active power dissipation of 550 mW maximum and a low CMOS standby power consumption of 550  $\mu$ W maximum.

The L1016 multipliers generate a 32-bit product from two 16-bit input busses. The input data can be specified as unsigned magnitude or two's complement, by controlling the state of the C<sub>x</sub> and C<sub>y</sub> mode lines. Mixed input modes are also permitted. The most significant half of the product (MSP) is available on the 16-bit output port. The least significant half (LSP) is multiplexed with MSP and is available at either the 16-bit output port or the Y input port.

S-113 RES Corp  
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F877 LAT



## ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	RATING	VALUE	UNIT
$C_{TERM}$	Terminal Voltage with Respect to GND(2)	-0.5 to +7.0	V
$T_A$	Operating Temperature	0 to +70	°C
$T_{BIAS}$	Temperature Under Bias	-55 to +125	°C
$T_{STG}$	Storage Temperature	-65 to +150	°C
$P_T$	Power Dissipation	1.0	W
$I_{OUT}$	DC Output Current	50	mA

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS ( $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ )

Symbol	Parameter	Min	Typ	Max	Unit
$V_{CCM}$	Military Supply Voltage	4.5	5.0	5.5	V
$V_{CCC}$	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
$V_{IH}$	Input High Voltage	2.0	—	—	V
$V_{IL}$	Input Low Voltage	—	—	0.8	V

(Commercial:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ\text{C}$  to  $125^\circ\text{C}$ )

SYMBOL	PARAMETER	TEST CONDITIONS	COMMERCIAL		MILITARY		UNIT
			MIN.	MAX.	MIN.	MAX.	
$ I_{LI} $	Input Leakage Current	$V_{CC} = \text{Max}, V_{IN} = 0 \text{ to } V_{CC}$	—	2	—	10	$\mu\text{A}$
$ I_{LO} $	Output Leakage Current	High Z, $V_{CC} = \text{max.}, V_{OUT} = 0 \text{ to } V_{CC}$	—	2	—	10	$\mu\text{A}$
$I_{CC(1)}$	Operating Power Supply Current	Output Open	—	100	—	120	mA
$I_{CCQ1}$	Quiescent Power Supply Current	$V_{IN} \geq V_{IH}, V_{IN} \leq V_{IL}$	—	30	—	30	mA
$I_{CCQ2}$	Quiescent Power Supply Current	$V_{IN} \geq V_{CC} - .2V \text{ or } \leq .2V$	—	.1	—	.1	mA
$V_{OH}$	Output High Voltage	$V_{CC} = \text{Min.}, I_{OH} = -0.4 \text{ mA}$	2.4	—	2.4	—	V
$V_{OL}$	Output Low Voltage	$V_{CC} = \text{Min.}, I_{OL} = 4.0 \text{ mA}$	—	0.5	—	0.5	V

- $I_{CC}$  is measured at clock cycle = 10 mhz and  $V_{IN} = \text{TTL}$  voltages.

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

SYMBOL	ITEM	CONDITIONS	MAX.	UNIT
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	10	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	12	pF

NOTE: This parameter is sampled and not 100% tested.

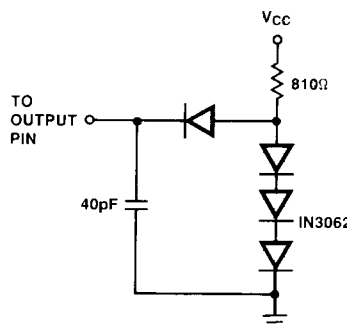


Figure 1. A.C. Output Test Load

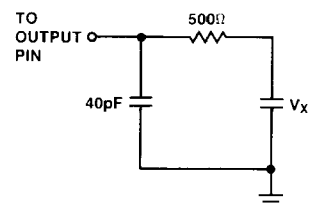


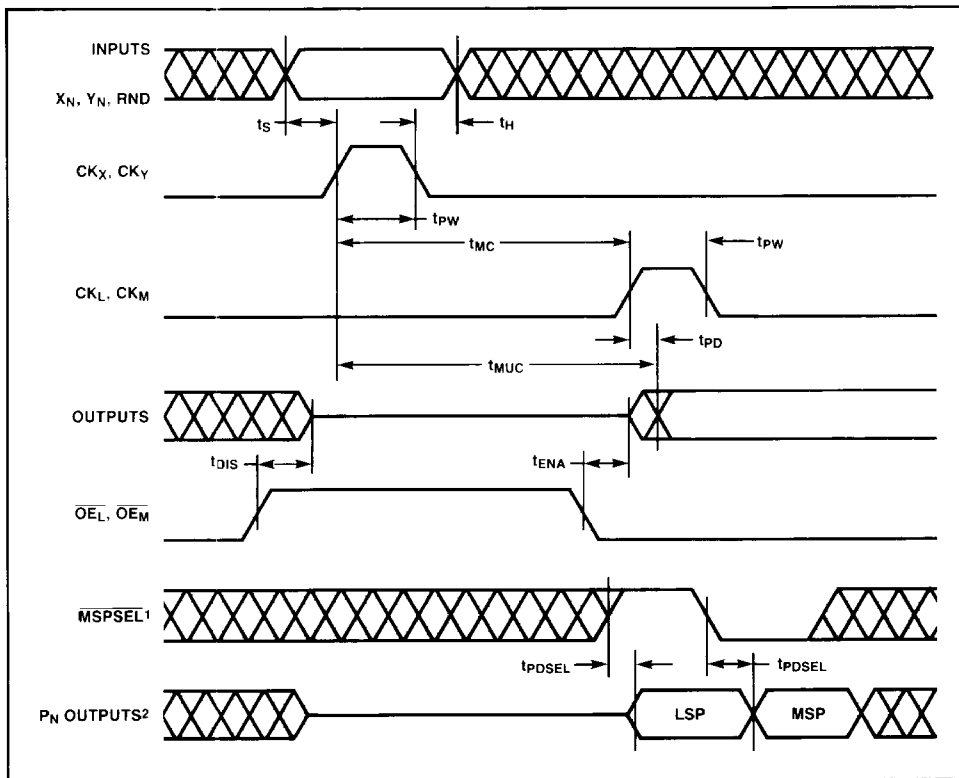
Figure 2. Output Three State Delay Load  
 $V_x = 0V \text{ or } 2.6V$

### AC ELECTRICAL CHARACTERISTICS

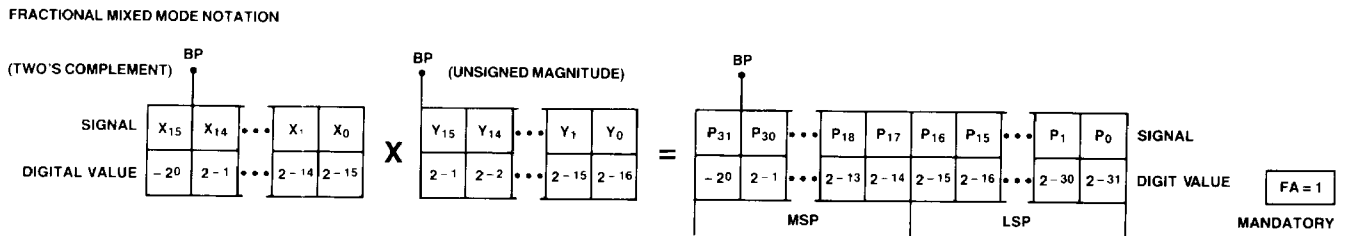
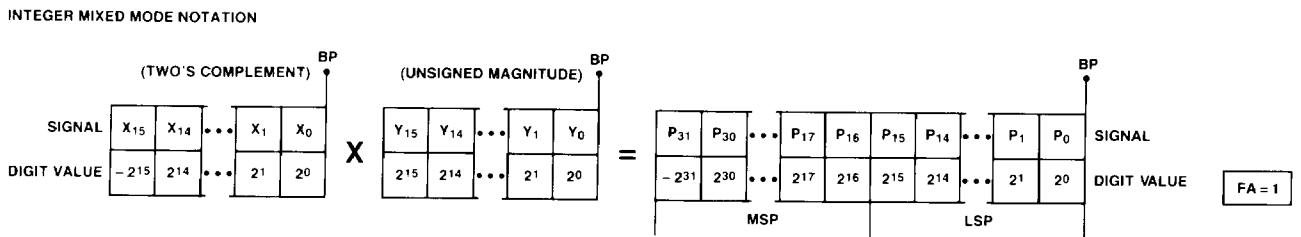
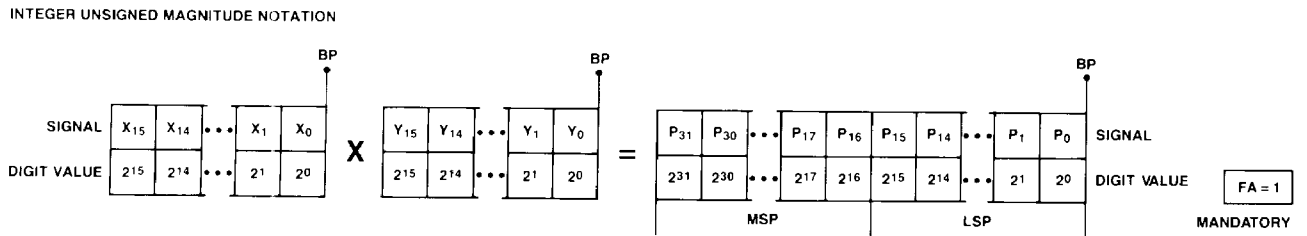
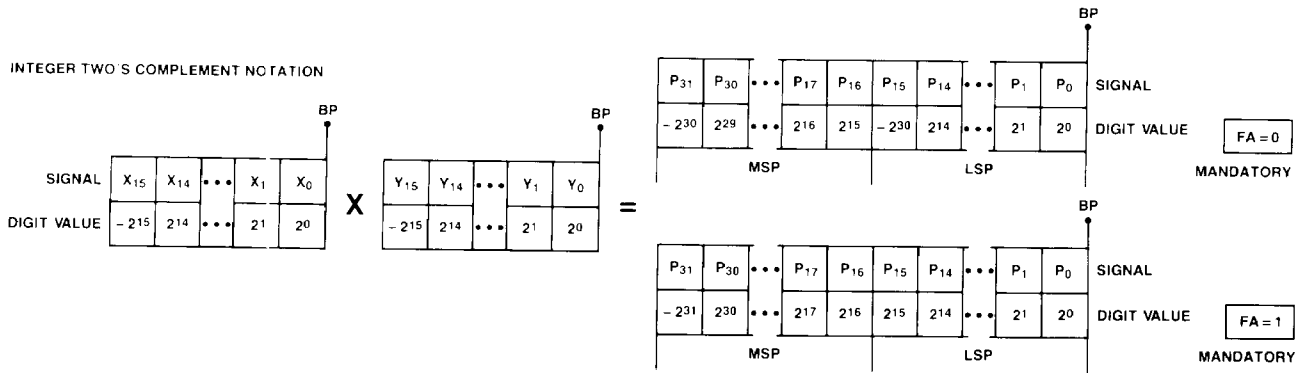
(Commercial:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ C$  to  $70^\circ C$ ; Military:  $V_{CC} = 5V \pm 10\%$ ,  $T_A = -55^\circ C$  to  $125^\circ C$ )

SYMBOL	PARAMETER	L1016-45		L1016-65		L1016-90		UNITS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$t_{MUC}$	Unlocked Multiply Time	—	65	—	95	—	120	ns
$t_{MC}$	Clocked Multiply Time	—	45	—	65	—	90	ns
$t_S$	X, Y, RND Setup Time	15	—	20	—	25	—	ns
$t_H$	X, Y, RND Hold Time	0	—	0	—	0	—	ns
$t_{ENA}$	3 State Enable Time	0	20	0	30	0	30	ns
$t_{DIS}$	3 State Disable Time	0	20	0	30	0	30	ns
$t_{PW}$	Clock Pulse Width	15	—	20	—	25	—	ns
$t_{PD}$	Output Clock to Valid Data	—	20	—	30	—	30	ns
$t_{PSEL}$	Output Control to Valid Data	—	20	—	30	—	30	ns

### GRAM



1. A Transition of  $\overline{MSPSEL}$  is not required during any cycle, and in some applications it can be grounded.
2. The order of appearance of the LSP and MSP on the output bus is determined by the logic level sequence of  $\overline{MSPSEL}$ .



### SIGNAL DESCRIPTIONS

**X<sub>0</sub> — X<sub>15</sub>** The 16 multiplicand data inputs.

**Y<sub>0</sub> — Y<sub>15</sub>** The 16 multiplier data inputs. These inputs are time-multiplexed with the least significant product (LSP) outputs.

**P<sub>0</sub> — P<sub>15</sub>** The LSP output term. These 16 bits are time-multiplexed with the Y<sub>0</sub> — Y<sub>15</sub> multiplier inputs or can be accessed from the output port under control of the MSPSEL line.

**P<sub>16</sub> — P<sub>31</sub>** The most significant product (MSP) term output port, comprising the 16 most significant bits of the output. The LSP term can also be accessed from this output port under control of the MSPSEL line.

**C<sub>X</sub>, C<sub>Y</sub>** Mode controls for each X<sub>N</sub> and Y<sub>N</sub> input. When LOW, the controlled input is unsigned data, and when HIGH, the input is 2's complement.

**RND** This is the round control for the MSP. When active, the L1016 adds 1 to the most significant bit of the LSP, rounding the MSP upward.

**CK<sub>X</sub>, CK<sub>Y</sub>** These are the input register clocks. In ad-

dition to the inputs, the mode control bits (C<sub>X</sub>, C<sub>Y</sub>) and the RND bit are latched with these signals.

**CK<sub>L</sub>, CK<sub>M</sub>** These are the LSP and MSP output register clocks.

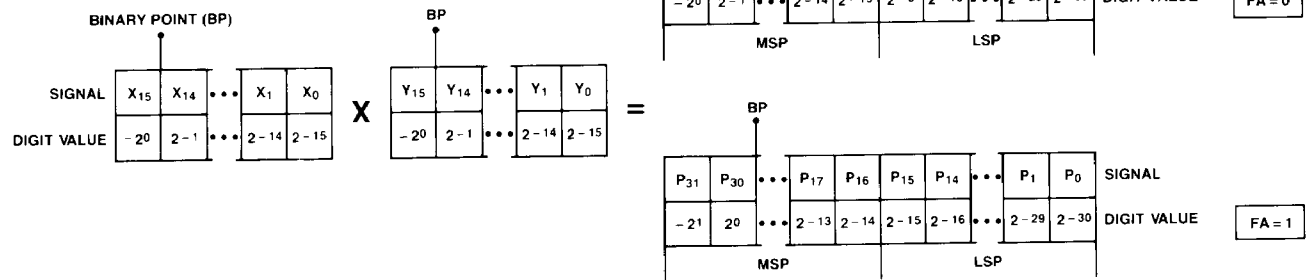
**FT** Flow-through control. When active (HIGH), the output registers of the LSP and MSP are in transparent or flow-through mode.

**OE<sub>L</sub>, OE<sub>M</sub>** Three-state output enable controls for the LSP and MSP.

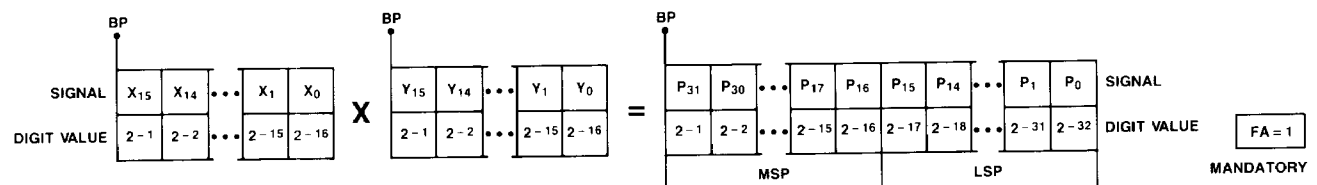
**MSPSEL** Controls the output multiplexer which presents either MSP or LSP terms to the P<sub>16</sub> — P<sub>32</sub> output port.

**FA** Format adjust control. In 2's complement arithmetic, if FA is HIGH, a full 32-bit product is produced with a sign bit in the MSP. If FA is LOW, the sign value of the product is replicated in the most significant bits of the LSP and MSP. In integer or mixed mode, FA must be HIGH to get a valid product, and the most significant bit of the product contains the sign bit if the output is in 2's complement.

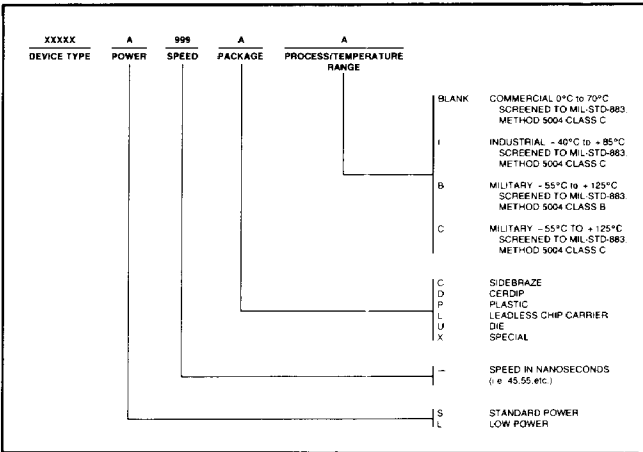
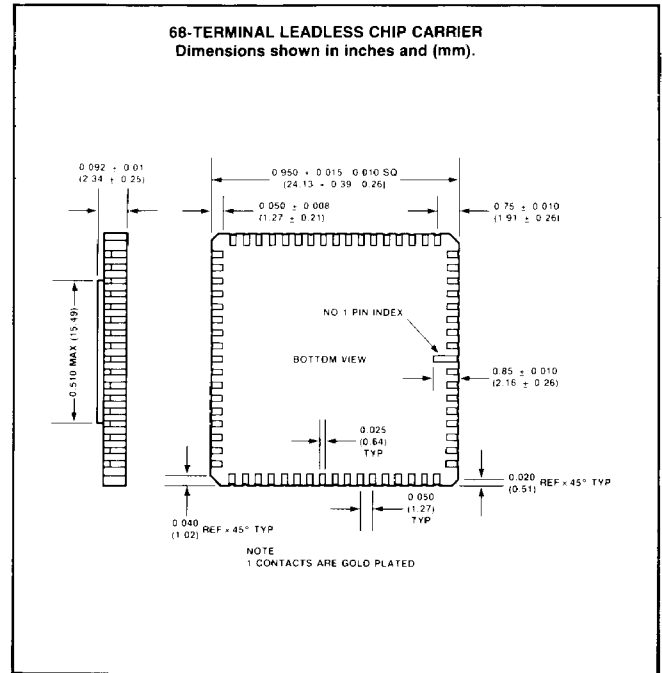
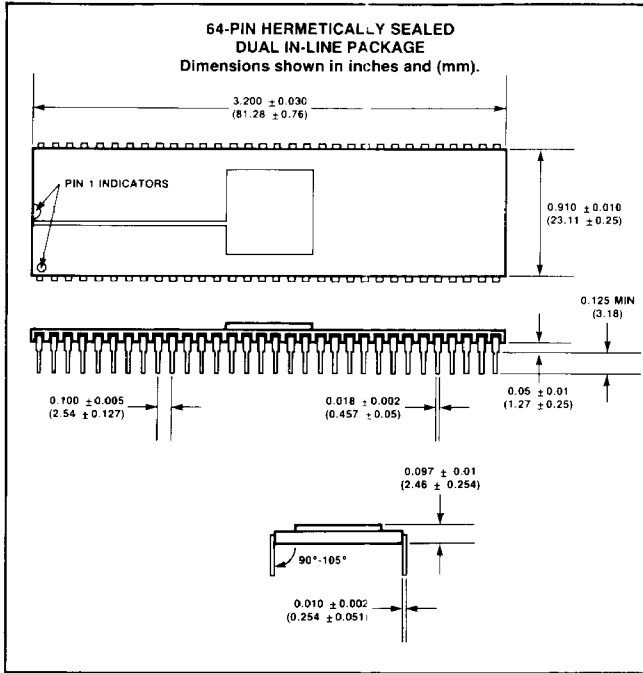
#### FRACTIONAL TWO'S COMPLEMENT NOTATION



#### FRACTIONAL UNSIGNED MAGNITUDE NOTATION



### PACKAGE INFORMATION



PIN	FUNCTION	PIN	FUNCTION
1	V <sub>CC</sub>	35	P <sub>7</sub> , Y <sub>7</sub>
2	GND	36	P <sub>6</sub> , Y <sub>6</sub>
3	GND	37	P <sub>5</sub> , Y <sub>5</sub>
4	MSPSEL	38	P <sub>4</sub> , Y <sub>4</sub>
5	FT	39	P <sub>3</sub> , Y <sub>3</sub>
6	FA	40	P <sub>2</sub> , Y <sub>2</sub>
7	OEM	41	P <sub>1</sub> , Y <sub>1</sub>
8	CKM	42	P <sub>0</sub> , Y <sub>0</sub>
9	N/C	43	N/C
10	P <sub>31</sub> , P <sub>15</sub>	44	CK <sub>Y</sub>
11	P <sub>30</sub> , P <sub>14</sub>	45	CK <sub>L</sub>
12	P <sub>29</sub> , P <sub>13</sub>	46	OEL
13	P <sub>28</sub> , P <sub>12</sub>	47	X <sub>0</sub>
14	P <sub>27</sub> , P <sub>11</sub>	48	X <sub>1</sub>
15	P <sub>26</sub> , P <sub>10</sub>	49	X <sub>2</sub>
16	P <sub>25</sub> , P <sub>9</sub>	50	X <sub>3</sub>
17	P <sub>24</sub> , P <sub>8</sub>	51	X <sub>4</sub>
18	P <sub>23</sub> , P <sub>7</sub>	52	X <sub>5</sub>
19	P <sub>22</sub> , P <sub>6</sub>	53	X <sub>6</sub>
20	P <sub>21</sub> , P <sub>5</sub>	54	X <sub>7</sub>
21	P <sub>20</sub> , P <sub>4</sub>	55	X <sub>8</sub>
22	P <sub>19</sub> , P <sub>3</sub>	56	X <sub>9</sub>
23	P <sub>18</sub> , P <sub>2</sub>	57	X <sub>10</sub>
24	P <sub>17</sub> , P <sub>1</sub>	58	X <sub>11</sub>
25	P <sub>16</sub> , P <sub>0</sub>	59	X <sub>12</sub>
26	NC	60	NC
27	P <sub>15</sub> , Y <sub>15</sub>	61	X <sub>13</sub>
28	P <sub>14</sub> , Y <sub>14</sub>	62	X <sub>14</sub>
29	P <sub>13</sub> , Y <sub>13</sub>	63	X <sub>15</sub>
30	P <sub>12</sub> , Y <sub>12</sub>	64	CK <sub>X</sub>
31	P <sub>11</sub> , Y <sub>11</sub>	65	RND
32	P <sub>10</sub> , Y <sub>10</sub>	66	C <sub>X</sub>
33	P <sub>9</sub> , Y <sub>9</sub>	67	C <sub>Y</sub>
34	P <sub>8</sub> , Y <sub>8</sub>	68	V <sub>CC</sub>