

# MB98A8040x- / 8050x- / 8060x- / 8070x-30 EEPROM MEMORY CARD

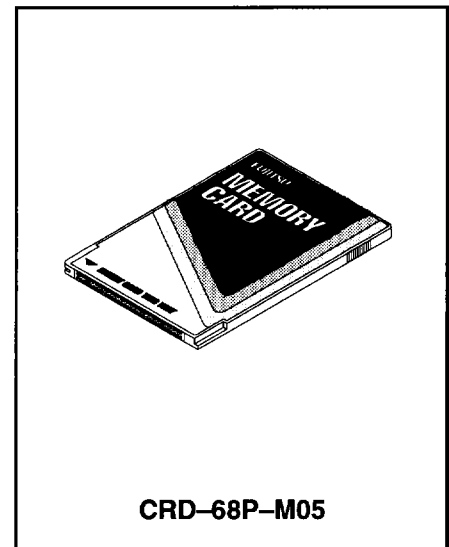
## ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY CARD 16K / 32K / 64K / 128K-BYTE

The Fujitsu MB98A8040x, MB98A8050x, MB98A8060x and MB98A8070x are Electrically Erasable Programmable Read Only Memory (EEPROM) cards capable of storing and retrieving large amounts of data. The memory circuits are housed in a credit-card sized 68-pin package. Internal circuit is protected by two metal panels, one at the top and bottom of the card, that help to reduce chip damage from electrostatic discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit bus configuration. All cards are portable and operate on low power at high speed.

In accordance with the Personal Computer Memory Card International Association (PCMCIA) and Japan Electrical Industry Development Association (JEIDA) industry standard specification, EEPROM cards offer additional EEPROM memory that is used to store attribute data. The attribute memory is an EEPROM card option. (See page 2 for description of the three available options.)

- PCMCIA and JEIDA industry standard for 68-pin memory card
- Credit card size dimensions: 85.6mm (length) x 54.0mm (width) x 3.3mm (thick)
- PCMCIA / JEIDA industry standard, two-piece 68-pin connector (with a two-row built-in receptacle)
- Write protect function
- Single +5V±5% power supply
- Static operation: No clock required
- TTL compatible inputs and outputs



### ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Unit
Supply Voltage	VCC	-0.5 to +6.0	V
Input Voltage	VIN	-0.5 to VCC +0.5	V
Output Voltage	VOUT	-0.5 to VCC +0.5	V
Temperature under Bias	TBIAS	-10 to +60	°C
Storage Temperature	TSTG	-30 to +70	°C

**NOTE:** Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

\*FUJMS147\*

## ATTRIBUTE MEMORY OPTIONS

PCMCIA and JEIDA standard memory cards from Fujitsu provide a separate EEPROM memory address space for recording fundamental card information. It is used by the card manufacturers to record basic configuration information such as device type, size, speed, etc.

The attribute memory is selected by asserting the  $\overline{\text{REG}}$  pin on the card interface. Option descriptions as follows.

### OPTION 1: Attribute memory is not supported. $\overline{\text{REG}}$ pin : Not Contacted

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A80401	MBM28C65 x 2 pcs	300 ns	N / A	N / A	16K x 8 bits/ 8K x 16 bits
MB98A80501	MBM28C65 x 4 pcs	300 ns	N / A	N / A	32K x 8 bits/ 16K x 16 bits
MB98A80601	MBM28C65 x 8 pcs	300 ns	N / A	N / A	64K x 8 bits/ 32K x 16 bits
MB98A80701	MBM28C65 x 16 pcs	300 ns	N / A	N / A	128K x 8 bits/ 64K x 16 bits

### OPTION 2: Attribute memory in a separate location is not supported.

When  $\overline{\text{REG}}$  line is asserted, "FF" is output to the data bus to indicate that attribute data may be stored in main memory.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A80402	MBM28C65 x 2 pcs	300 ns	N / A	N / A	16K x 8 bits/ 8K x 16 bits
MB98A80502	MBM28C65 x 4 pcs	300 ns	N / A	N / A	32K x 8 bits/ 16K x 16 bits
MB98A80602	MBM28C65 x 8 pcs	300 ns	N / A	N / A	64K x 8 bits/ 32K x 16 bits
MB98A80702	MBM28C65 x 16 pcs	300 ns	N / A	N / A	128K x 8 bits/ 64K x 16 bits

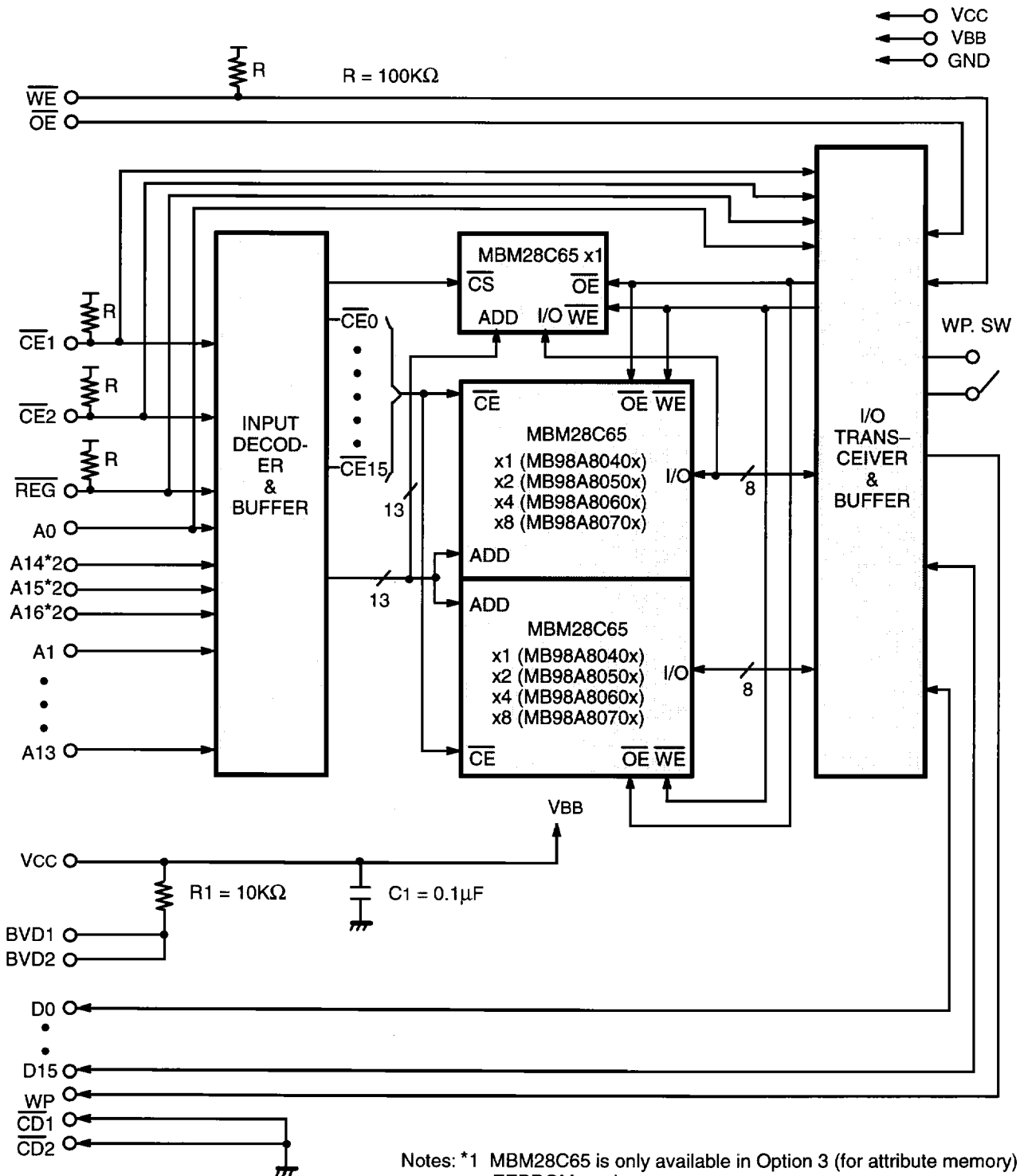
### OPTION 3: Attribute memory is supported. The data is stored in an 8K-bit EEPROM.

When  $\overline{\text{REG}}$  line is asserted, data stored in EEPROM is output to the data bus.

Part Number	Main Memory		Attribute Memory		Memory Organization *
	Memory Device	Access Time	Memory Device	Access Time	
MB98A80403	MBM28C65 x 2 pcs	300 ns	MBM28C65 x 1 pc	300 ns	16K x 8 bits/ 8K x 16 bits
MB98A80503	MBM28C65 x 4 pcs	300 ns	MBM28C65 x 1 pc	300 ns	32K x 8 bits/ 16K x 16 bits
MB98A80603	MBM28C65 x 8 pcs	300 ns	MBM28C65 x 1 pc	300 ns	64K x 8 bits/ 32K x 16 bits
MB98A80703	MBM28C65 x 16 pcs	300 ns	MBM28C65 x 1 pc	300 ns	128K x 8 bits/ 64K x 16 bits

Note: \* To be configured by user.

**Fig. 1 - MB98A8040x, 8050x, 8060x, and 8070x BLOCK DIAGRAM**



Notes: \*1 MBM28C65 is only available in Option 3 (for attribute memory) EEPROM cards.

\*2 See pin 14, 19, and 20 in "PIN ASSIGNMENTS."

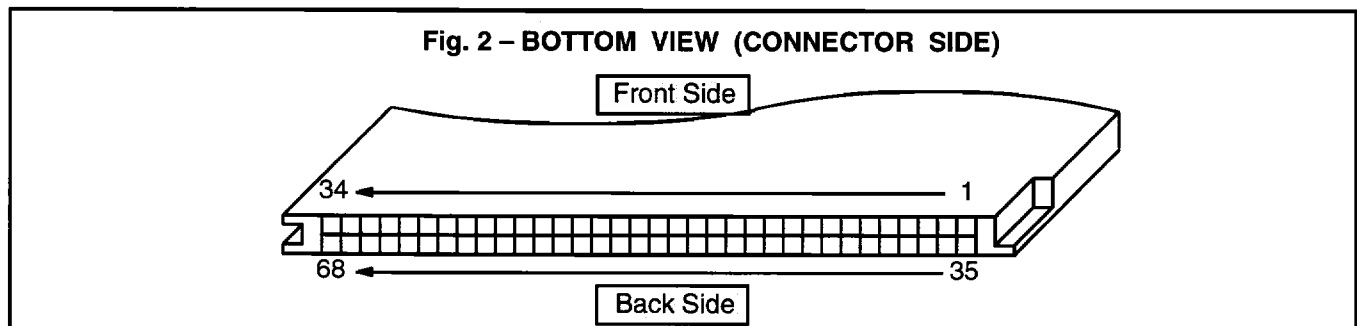
## PIN ASSIGNMENTS

MB98A8040x	MB98A8050x	MB98A8060x	MB98A8070x	Pin No.		MB98A8040x	MB98A8050x	MB98A8060x	MB98A8070x
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	$\overline{CE1}$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$	$\overline{CE2}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	NC	NC	NC	NC
A13	A13	A13	A13	13	47	NC	NC	NC	NC
NC	A14	A14	A14	14	48	NC	NC	NC	NC
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	15	49	NC	NC	NC	NC
NC	NC	NC	NC	16	50	NC	NC	NC	NC
VCC	VCC	VCC	VCC	17	51	VCC	VCC	VCC	VCC
NC	NC	NC	NC	18	52	NC	NC	NC	NC
NC	NC	NC	A16	19	53	NC	NC	NC	NC
NC	NC	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$	$\overline{REG}$
A1	A1	A1	A1	28	62	BVD2	BVD2	BVD2	BVD2
A0	A0	A0	A0	29	63	BVD1	BVD1	BVD1	BVD1
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

## PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A16	Address Input	Input	Address Inputs, A0–A16.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. The data bus size (8-bit or 16-bit) selected with CE1 and CE2.
$\overline{CE1}$	Card Enable for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function of EEPROM cards.
$\overline{CE2}$	Card Enable for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function of EEPROM cards.
$\overline{REG}$	Attribute Memory Select	Input	Active Low. –Attribute memory is selected for read/write function of identification data of EEPROM cards. (NC or "FF" data or attribute data.)
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for EEPROM cards.
$\overline{WE}$	Write Enable	Input	Active Low. –Write enable for EEPROM cards.
$\overline{CD1}, \overline{CD2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for EEPROM cards. This pin outputs the Protect / Non Protect status of "WP Switch".
BVD1, BVD2	Battery Voltage Detect	Output	Both pins are tied to VCC internally.
VCC	Power Supply	–	Power Supply Voltage. (+5.0V $\pm$ 5%)
GND	Ground	–	System Ground.
NC	No Connection	–	

## PIN LOCATIONS



## FUNCTION TRUTH TABLE

### MAIN MEMORY FUNCTION \*1 ( $\overline{\text{REG}}=\text{VIH}$ )

$\overline{\text{CE}}_2$	$\overline{\text{CE}}_1$	A0 (Byte)	$\overline{\text{OE}}$	$\overline{\text{WE}}$	WP	Mode	Data Input/Output		WP SW.
							D15-D8	D7-D0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (x8)	High-Z	DOUT (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High-Z	DOUT (Upper Byte)	NP
H	L	L	H	L	L	Write (x8)	High-Z	DIN (Lower Byte)	NP
H	L	H	H	L	L	Write (x8)	High-Z	DIN (Upper Byte)	NP
L	H	X	L	H	L	Read (x8)	DOUT (Upper Byte)	High-Z	NP
L	H	X	H	L	L	Write (x8)	DIN (Upper Byte)	High-Z	NP
L	L	X	L	H	L	Read (x16)	DOUT		NP
L	L	X	H	L	L	Write (x16)	DIN		NP
X	X	X	H	H	L	Output Disable	High-Z		NP

H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (x8)	High-Z	DOUT (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High-Z	DOUT (Upper Byte)	P
H	L	L	H	L	H	Output Disable	High-Z		P
H	L	H	H	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (x8)	DOUT (Upper Byte)	High-Z	P
L	H	X	H	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (x16)	DOUT		P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

Note: \*1 H = VIH, L = VIL, X = Either VIL or VIH, WP SW = Write Protect Switch, NP = Non Protect, P = Protect

**FUNCTION TRUTH TABLE (Continued)**  
**ATTRIBUTE MEMORY FUNCTION \*1 ( $\overline{\text{REG}}=\text{VIL}$ ) \*2**

$\overline{\text{CE2}}$	$\overline{\text{CE1}}$	A0 (Byte)	$\overline{\text{OE}}$	$\overline{\text{WE}}$	WP	Mode	Data Input/Output		WP SW.
							D15–D8	D7–D0	
H	H	X	X	X	L	Standby	High-Z		NP
H	L	L	L	H	L	Read (x8)	High-Z	DOUT *3 (Lower Byte)	NP
H	L	H	L	H	L	Read (x8)	High-Z	H	NP
H	L	L	H	L	L	Write (x8)	High-Z	DIN (Lower Byte)	NP
H	L	H	H	L	L	Write (x8)	High-Z	X	NP
L	H	X	L	H	L	Read (x8)	H	High-Z	NP
L	H	X	H	L	L	Write (x8)	High-Z	High-Z	NP
L	L	X	L	H	L	Read (x16)	H	DOUT *3 (Lower Byte)	NP
L	L	X	H	L	L	Write (x16)	X	DIN (Lower Byte)	NP
X	X	X	H	H	L	Output Disable	High-Z		NP

H	H	X	X	X	H	Standby	High-Z		P
H	L	L	L	H	H	Read (x8)	High-Z	DOUT *3 (Lower Byte)	P
H	L	H	L	H	H	Read (x8)	High-Z	H	P
H	L	L	H	L	H	Output Disable	High-Z		P
H	L	H	H	L	H	Output Disable	High-Z		P
L	H	X	L	H	H	Read (x8)	H	High-Z	P
L	H	X	H	L	H	Output Disable	High-Z		P
L	L	X	L	H	H	Read (x16)	H	DOUT *3 (Lower Byte)	P
L	L	X	H	L	H	Output Disable	High-Z		P
X	X	X	H	H	H	Output Disable	High-Z		P

Notes: \*1 H = VIH, L = VIL, X = Either VIL or VIH, WP SW = Write Protect Switch, NP = Non Protect, P = Protect

\*2 NC for MB98A80401, 80501, 80601, and 80701.

\*3 H-level is output for MB98A80402, 80502, 80602, and 80702.

## ADDRESS CONFIGURATIONS \*1 (MAIN MEMORY)

### 8-BIT BUS ORGANIZATION ( $\overline{CE1} = \text{VIL}, \overline{CE2} = \text{VIH}$ )

A16 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
0 0000 0000 0000 0000	H	L	-----	0 Add.
0 0000 0000 0000 0001	H	L	-----	1 Add.
0 0000 0000 0000 0010	H	L	-----	2 Add.
0 0000 0000 0000 0011	H	L	-----	3 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 1100	H	L	-----	131,068 Add.
1 1111 1111 1111 1101	H	L	-----	131,069 Add.
1 1111 1111 1111 1110	H	L	-----	131,070 Add.
1 1111 1111 1111 1111	H	L	-----	131,071 Add.

### 8-BIT BUS ORGANIZATION ( $\overline{CE1} = \text{VIH}, \overline{CE2} = \text{VIL}$ ) \*2

A16 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
0 0000 0000 0000 000X	L	H	1 Add.	-----
0 0000 0000 0000 001X	L	H	3 Add.	-----
0 0000 0000 0000 010X	L	H	5 Add.	-----
0 0000 0000 0000 011X	L	H	7 Add.	-----
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 100X	L	H	131,065 Add.	-----
1 1111 1111 1111 101X	L	H	131,067 Add.	-----
1 1111 1111 1111 110X	L	H	131,069 Add.	-----
1 1111 1111 1111 111X	L	H	131,071 Add.	-----

### 16-BIT BUS ORGANIZATION ( $\overline{CE1} = \text{VIL}, \overline{CE2} = \text{VIL}$ )

A16 to A0	$\overline{CE2}$	$\overline{CE1}$	D15-D8	D7-D0
0 0000 0000 0000 000X	L	L	1 Add.	0 Add.
0 0000 0000 0000 001X	L	L	3 Add.	2 Add.
0 0000 0000 0000 010X	L	L	5 Add.	4 Add.
0 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
1 1111 1111 1111 100X	L	L	131,065 Add.	131,064 Add.
1 1111 1111 1111 101X	L	L	131,067 Add.	131,066 Add.
1 1111 1111 1111 110X	L	L	131,069 Add.	131,068 Add.
1 1111 1111 1111 111X	L	L	131,071 Add.	131,070 Add.

Notes: \*1 H = VIH, L = VIL, X = Either 0 or 1.

\*2 Even addresses are not available in this mode.

## RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	4.75	5.0	5.25	V
Ground	GND		0		V
Input High Voltage	VIH	2.4		VCC+0.3	V
Input Low Voltage	VIL	-0.3		0.8	V
Ambient Temperature	TA	0		55	°C

## DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Standby Supply Current	$\overline{CE}1, \overline{CE}2 \geq VCC - 0.2V$	ISB1			100	$\mu A$
	$\overline{CE}1, \overline{CE}2 = VIH$	ISB2			10	mA
Active Supply Current	$VIN = VIH \text{ or } VIL$ $\overline{CE}1, \overline{CE}2 = VIL, IOUT = 0mA$	ICC1			100	mA
Operating Supply Current	$VIN = VIH \text{ or } VIL, \text{ Cycle} = \text{Min.}$ $\text{Duty} = 100\%, IOUT = 0mA$ $\overline{OE} = VIH \text{ during Write Cycle}$	ICC2			100	mA
Input Leakage Current *1	$VIN = 0V \text{ to } VCC$	ILI	-10		10	$\mu A$
Output Leakage Current *2	$VOUT = 0V \text{ to } VCC,$ $\overline{CE}1, \overline{CE}2 = VIH \text{ or}$ $\overline{OE} = VIH \text{ or } \overline{WE} = VIL$	ILI/O	-10		10	$\mu A$
Output High Voltage *3	$I_{OH} = -1.0mA$	VOH	2.4			V
Output Low Voltage	$I_{OL} = 2.1mA$	VOL			0.4	V

Notes: \*1 This value does not apply to  $\overline{CE}1, \overline{CE}2, \overline{REG}$  and  $\overline{WE}$ .

\*2 This value does not apply to BVD1, BVD2,  $\overline{CD}1, \overline{CD}2$  and WP.

\*3 This value does not apply to BVD1, BVD2,  $\overline{CD}1$  and  $\overline{CD}2$ .

## CAPACITANCE (TA=25°C, f=1MHz, VIN=VIO=GND)

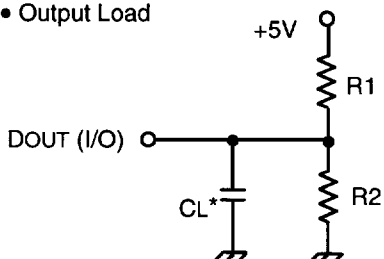
Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance *1	CIN			50	pF
I/O Capacitance *2	COUT			50	pF

Notes: \*1 This value does not apply to  $\overline{CE}1, \overline{CE}2, \overline{REG}$  and  $\overline{WE}$ .

\*2 This value does not apply to BVD1, BVD2,  $\overline{CD}1$  and  $\overline{CD}2$ .

**Fig. 3 – AC TEST CONDITIONS**

• Output Load



• Input Pulse Levels: 0.6V to 2.6V

• Input Pulse Rise and Fall Times: 5ns (Transition between 0.8V and 2.4V)

• Timing Reference Levels

Input:  $V_{IL} = 0.8V$ ,  $V_{IH} = 2.4V$

Output:  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$

\* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8k $\Omega$	990 $\Omega$	100pF	All parameters except tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ,
Load II	1.8k $\Omega$	990 $\Omega$	5pF	tRCHZ, tROHZ, tWLZ and tWHZ, tCLZ, tOLZ, tCHZ, tOHZ, tRCLZ, tROLZ, tRCHZ, tROHZ, tWLZ and tWHZ

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRC	300		ns
Address Access Time	tAA		300	ns
Card Enable Access Time	tCE		300	ns
Output Enable Access Time	tOE		150	ns
Output Hold from Address Change	tOH	5		ns
Card Enable to Output Low-Z *1*2	tCLZ	5		ns
Output Enable to Output Low-Z *1*2	tOLZ	5		ns
Card Enable to Output High-Z *1*2	tCHZ		60	ns
Output Enable to Output High-Z *1*2	tOHZ		60	ns

### ATTRIBUTE MEMORY READ CYCLE \*3

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	tRRC	300		ns
Address Access Time	tRAA		300	ns
Card Enable Access Time	tRCE		300	ns
Output Enable Access Time	tROE		150	ns
Output Hold from Address Change	tROH	5		ns
Card Enable to Output Low-Z *1*2	tRCLZ	5		ns
Output Enable to Output Low-Z *1*2	tROLZ	5		ns
Card Enable to Output High-Z *1*2	tRCHZ		60	ns
Output Enable to Output High-Z *1*2	tROHZ		60	ns

Notes: \*1 Transition is measured at the point of  $\pm 500mV$  from steady state voltage.

\*2 This parameter is specified using Load II in Fig.3.

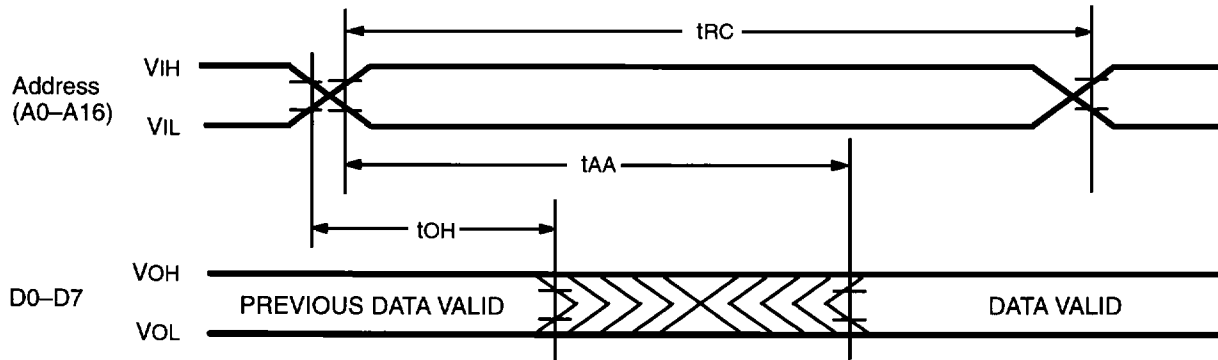
\*3 This parameter is for MB98A80403, 80503, 80603, and 80703.

## AC CHARACTERISTICS (Continued)

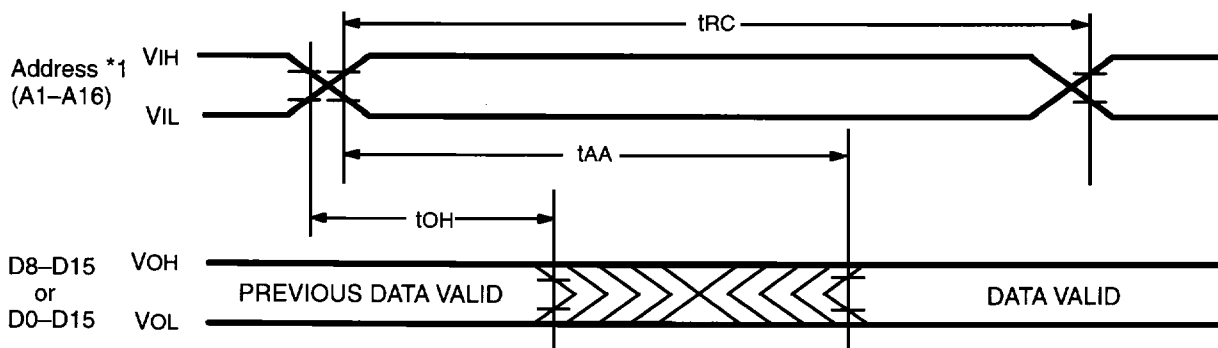
(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = VIH, \overline{REG} = VIH$ )

READ CYCLE 1:  $\overline{CE1} = \overline{OE} = VIL, \overline{CE2} = VIH$ : x 8-bit Bus Organization



READ CYCLE 2:  $\overline{CE1} = VIH, \overline{CE2} = \overline{OE} = VIL$ : x 8-bit Bus Organization  
 $\overline{CE1} = \overline{CE2} = \overline{OE} = VIL$ : x 16-bit Bus Organization



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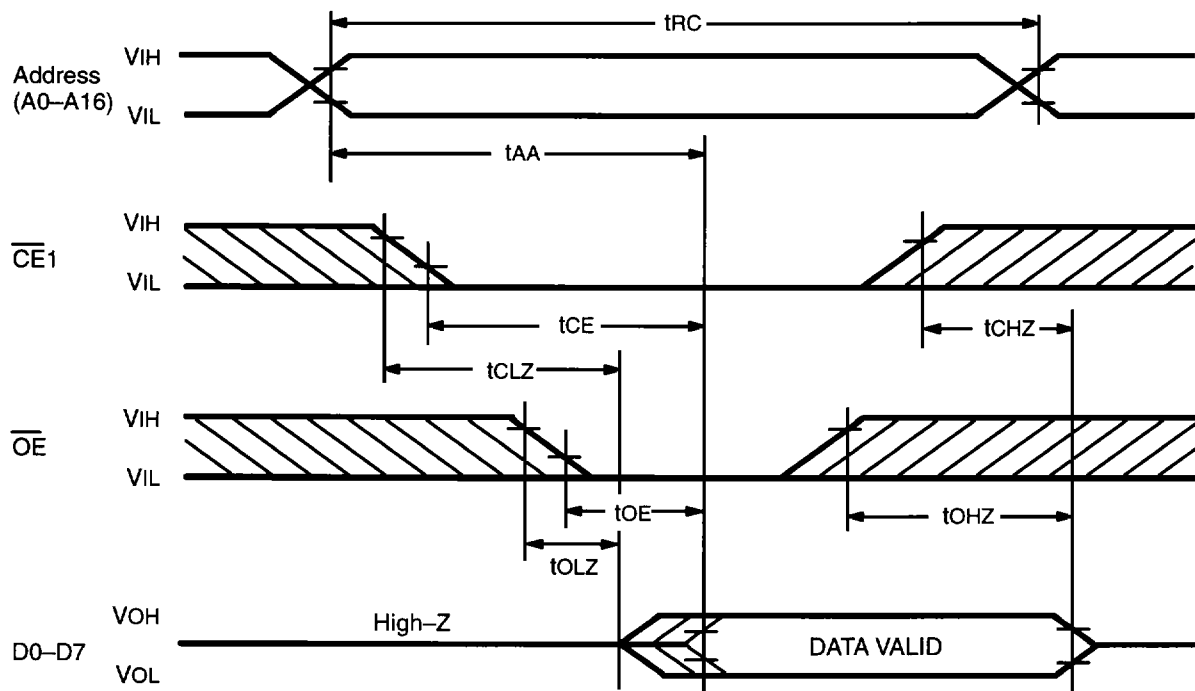
Note: \*1 A0 = Either VIH or VIL.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = VIH$ , $\overline{REG} = VIH$ )

READ CYCLE 3:  $\overline{CE2} = VIH$ : x 8-bit Bus Organization



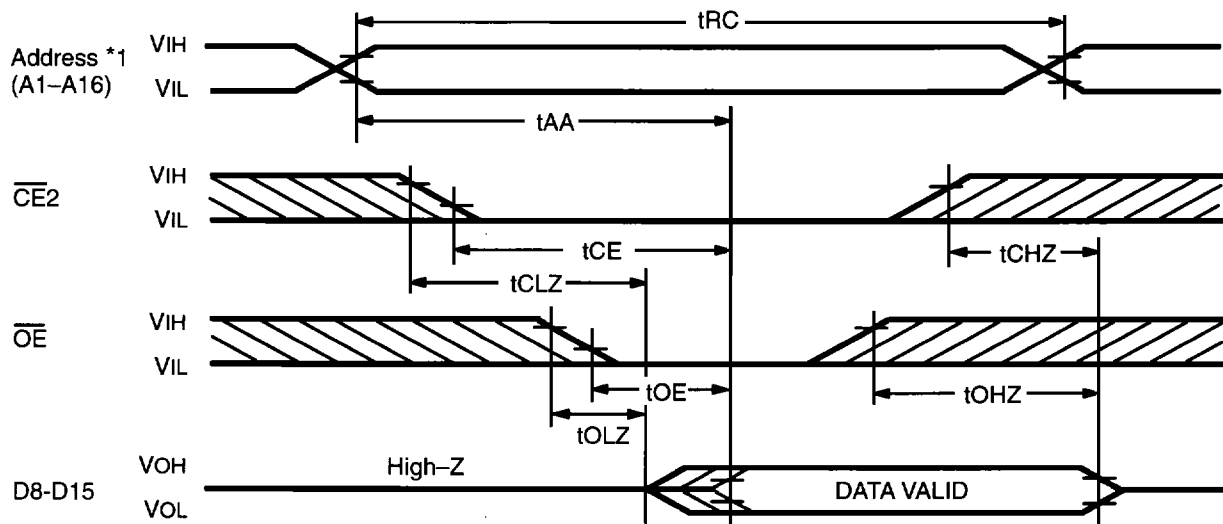
 :Undefined

## AC CHARACTERISTICS (Continued)

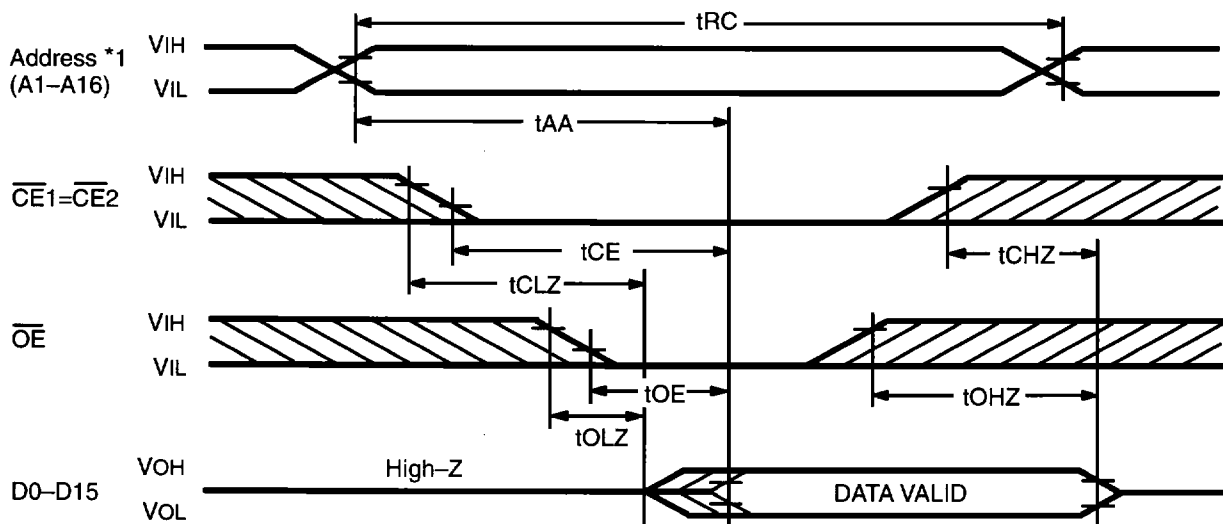
(Recommended operating conditions unless otherwise noted.)


### MAIN MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = VIH$ , $\overline{REG} = VIH$ )

READ CYCLE 4:  $\overline{CE1} = VIH$ : x 8-bit Bus Organization



READ CYCLE 5:  $\overline{CE1} = \overline{CE2}$ : x 16-bit Bus Organization



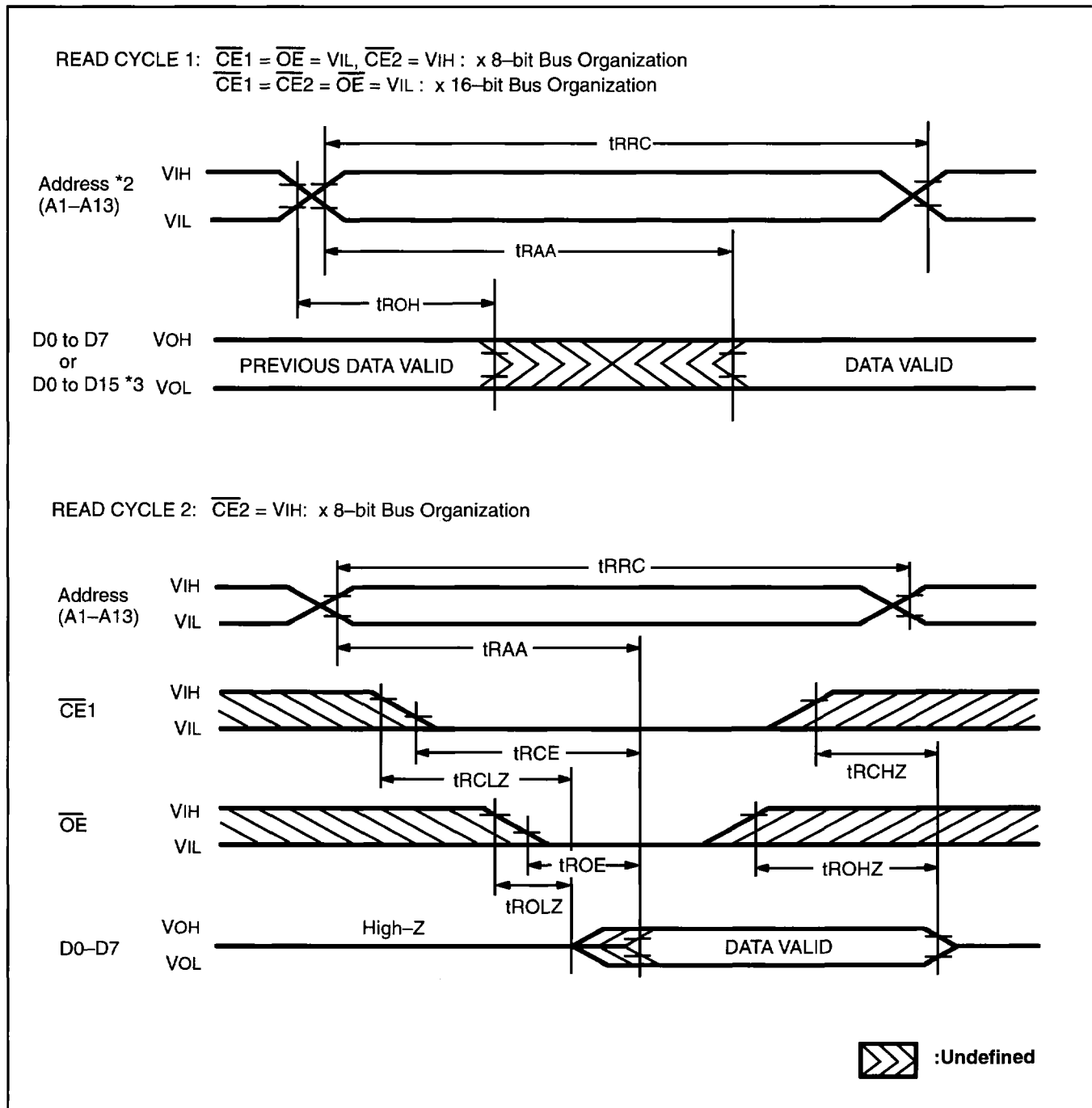
 :Undefined

Note: \*1 A0 = Either VIH or VIL.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = VIH, \overline{REG} = VIL$ ) \*1



Notes: \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

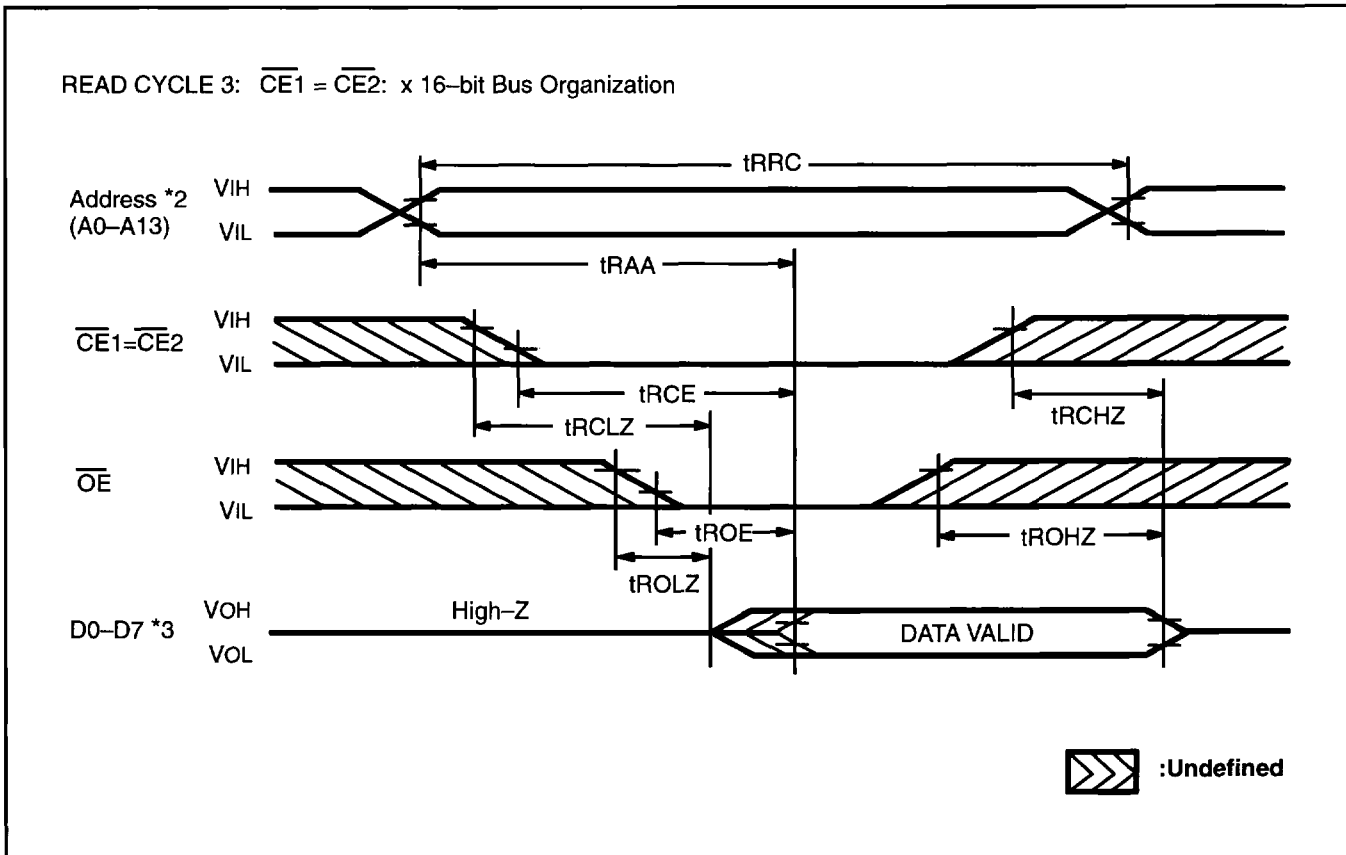
\*2 A0 = Either VIH or VIL during 16 bits bus organization.

\*3 H-level is output from D8 to D15.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY READ CYCLE TIMING DIAGRAM ( $\overline{WE} = VIH, \overline{REG} = VIL$ ) \*1



Notes \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

\*2 A0 = Either VIH or VIL.

\*3 H-level is output from D8 to D15.

## AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	tWR		10	ms
Address Setup Time	tAS	20		ns
Chip Enable Setup Time	tCS	0		ns
Output Enable Setup Time	tOES	20		ns
Write Pulse Width	tWP	100		ns
Address Hold Time	tAH	50		ns
Data Setup Time	tDS	50		ns
Data Hold Time	tDH	20		ns
Chip Enable Hold Time	tCH	0		ns
Output Enable Hold Time	tOEH	20		ns
Write Recovery Time	tRE	50		ns
End of Write to Output Time	tRBO		100	ns
Number of Write per Byte	N	10000		Times
Write Enable Hold Time	tWEH	10		ns

### ATTRIBUTE MEMORY WRITE CYCLE \*1

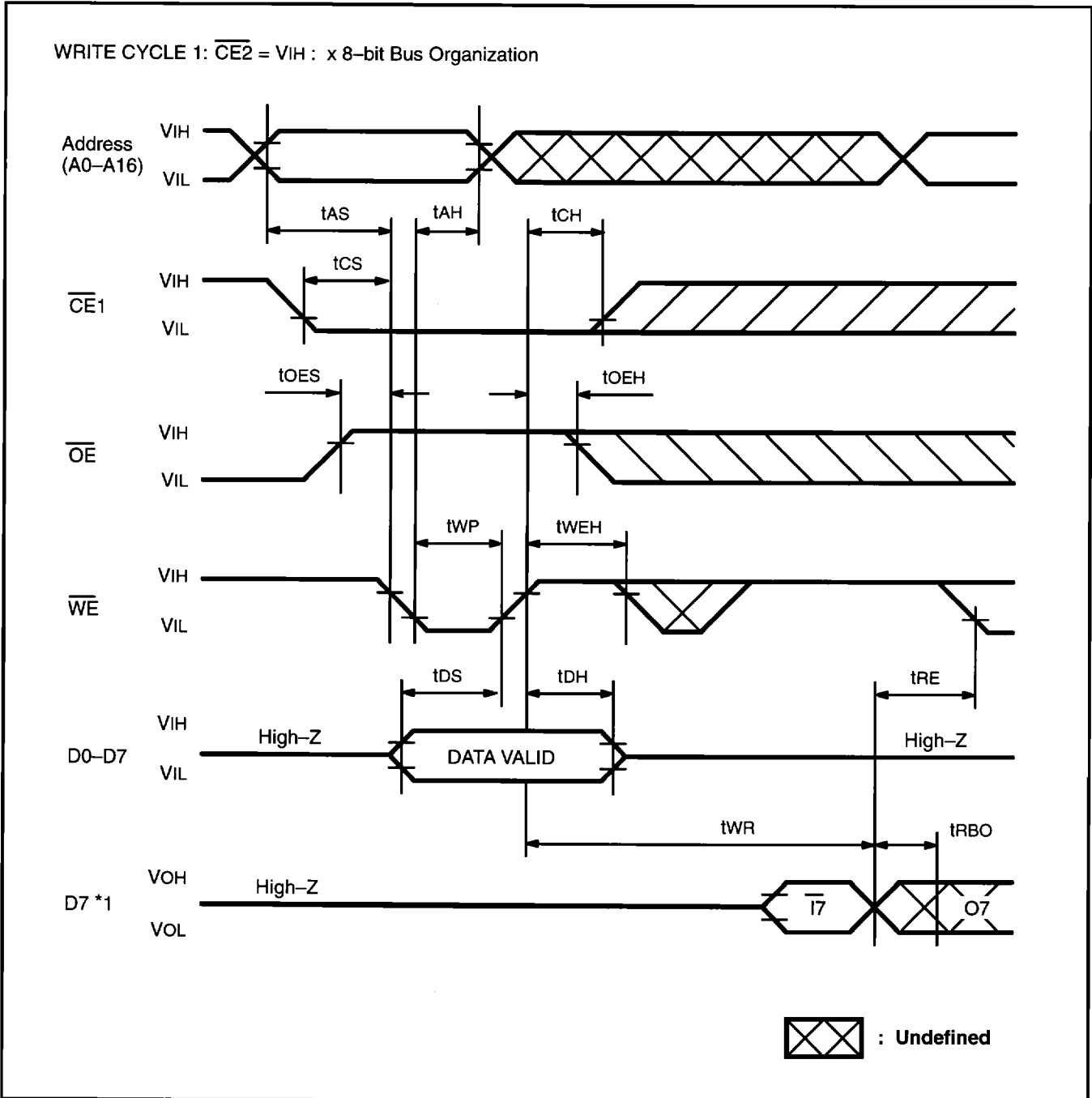
Parameter	Symbol	Min	Max	Unit
Write Cycle Time	tRWR		10	ms
Address Setup Time	tRAS	20		ns
Chip Enable Setup Time	tRCS	0		ns
Output Enable Setup Time	tROES	20		ns
Write Pulse Width	tRWP	100		ns
Address Hold Time	tRAH	50		ns
Data Setup Time	tRDS	50		ns
Data Hold Time	tRDH	20		ns
Chip Enable Hold Time	tRCH	0		ns
Output Enable Hold Time	tROEH	20		ns
Write Recovery Time	tRRE	50		ns
End of Write to Output Time	tRRBO		100	ns
Number of Write per Byte	N	10000		Times
Write Enable Hold Time	tRWEH	10		ns

Note: \*1 This parameter is for MB98A80403, 80503, 80603, and 80703.

# AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

## MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ -CONTROLLED, $\overline{REG} = V_{IH}$ )

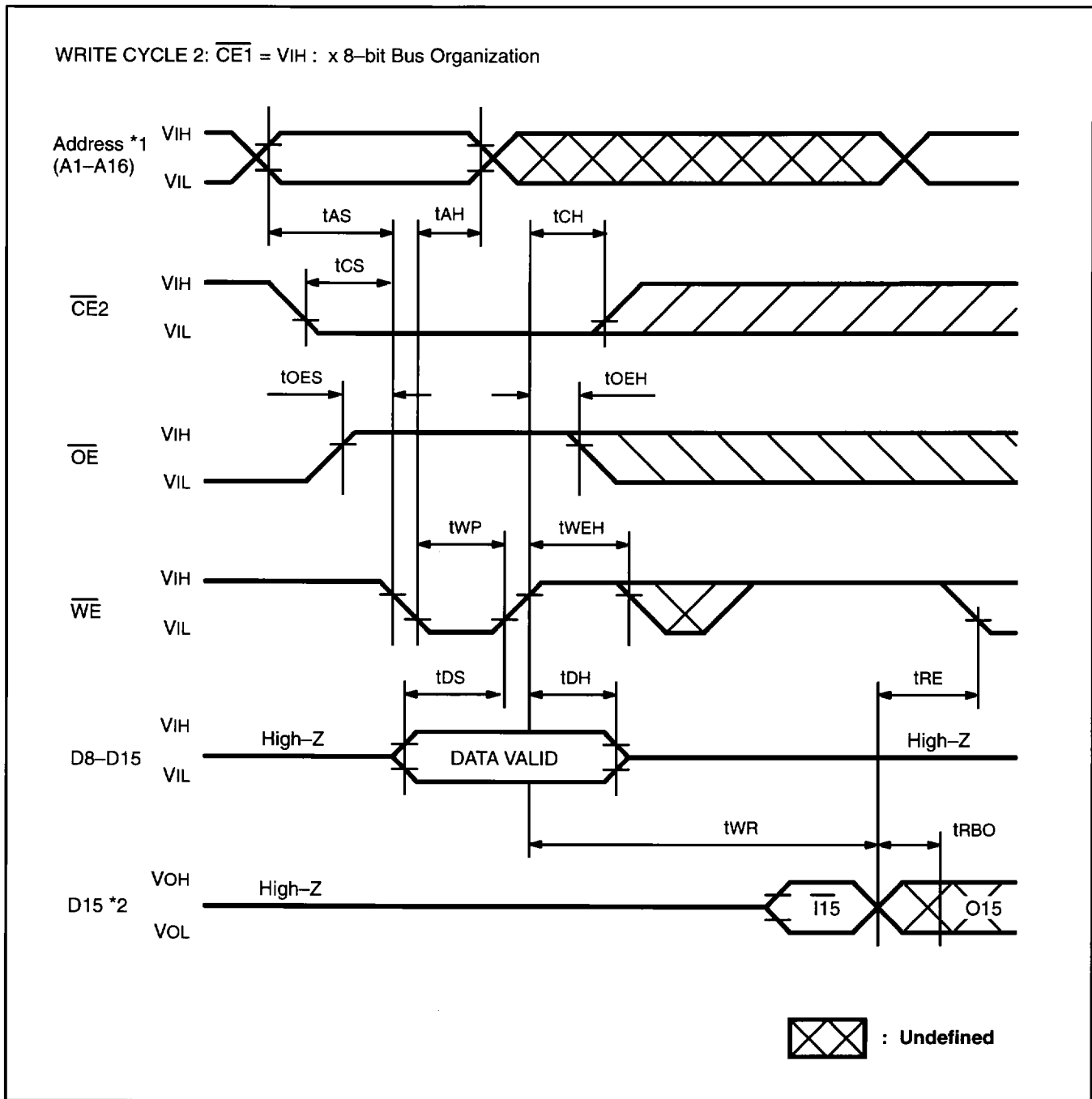


Note: \*1 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ -CONTROLLED, $\overline{REG} = V_{IH}$ )

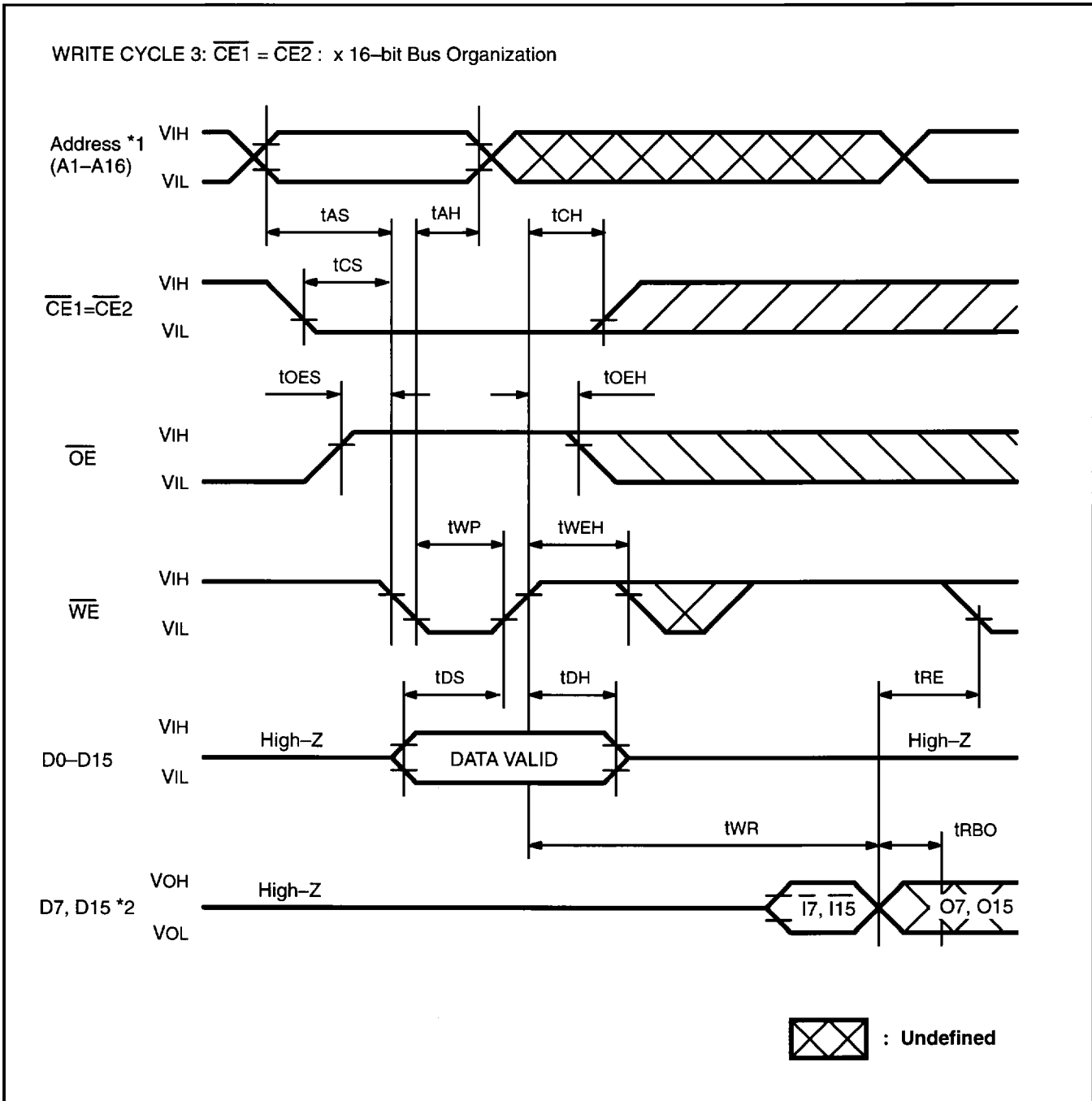


Notes: \*1 A0 = Either  $V_{IH}$  or  $V_{IL}$ .  
 \*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ -CONTROLLED, $\overline{REG} = V_{IH}$ )



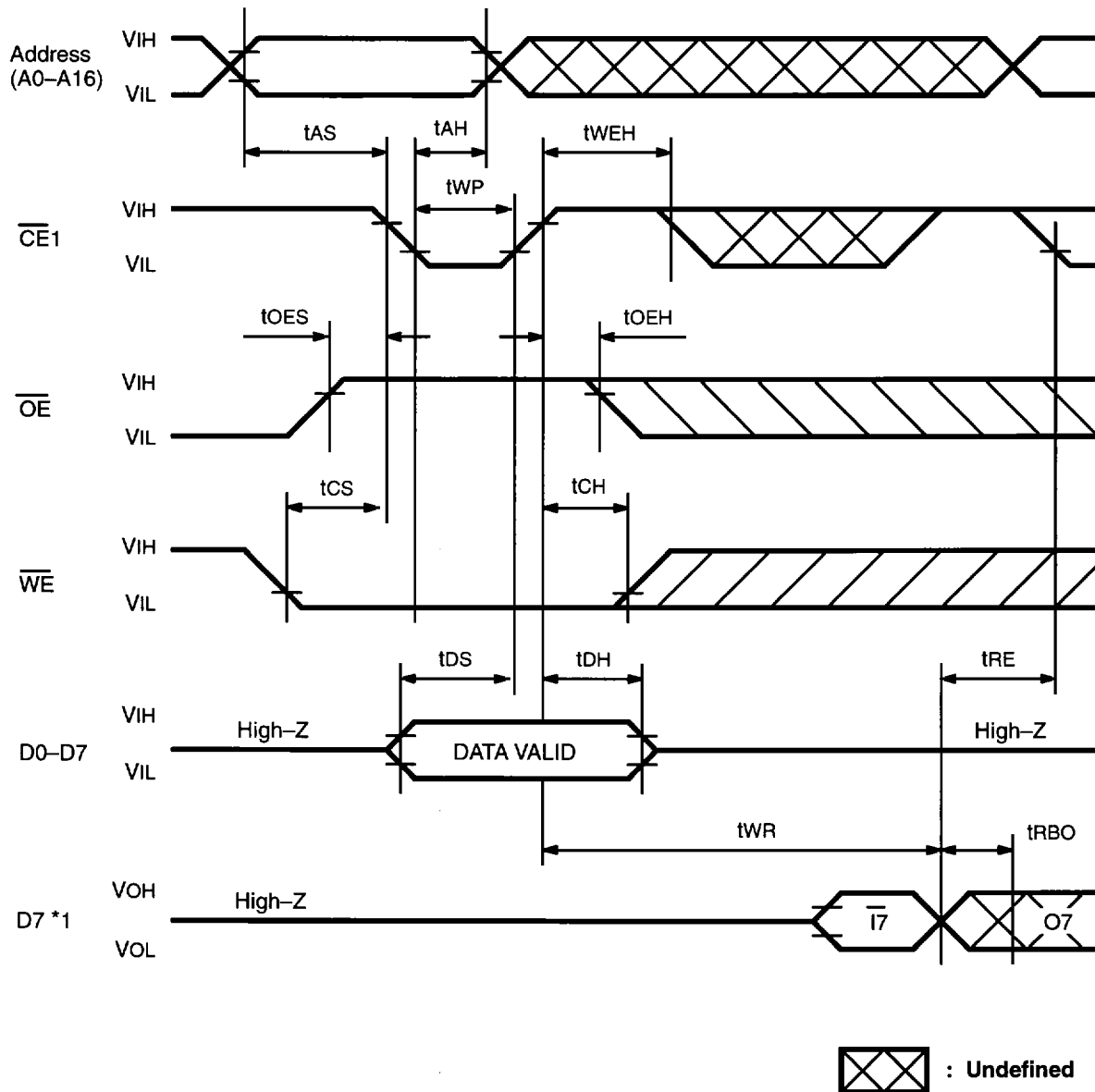
Notes: \*1 A0 = Either  $V_{IH}$  or  $V_{IL}$ .  
 \*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE}2$ -CONTROLLED, $\overline{REG} = V_{IH}$ )

WRITE CYCLE 4:  $\overline{CE}2 = V_{IH}$  : x 8-bit Bus Organization

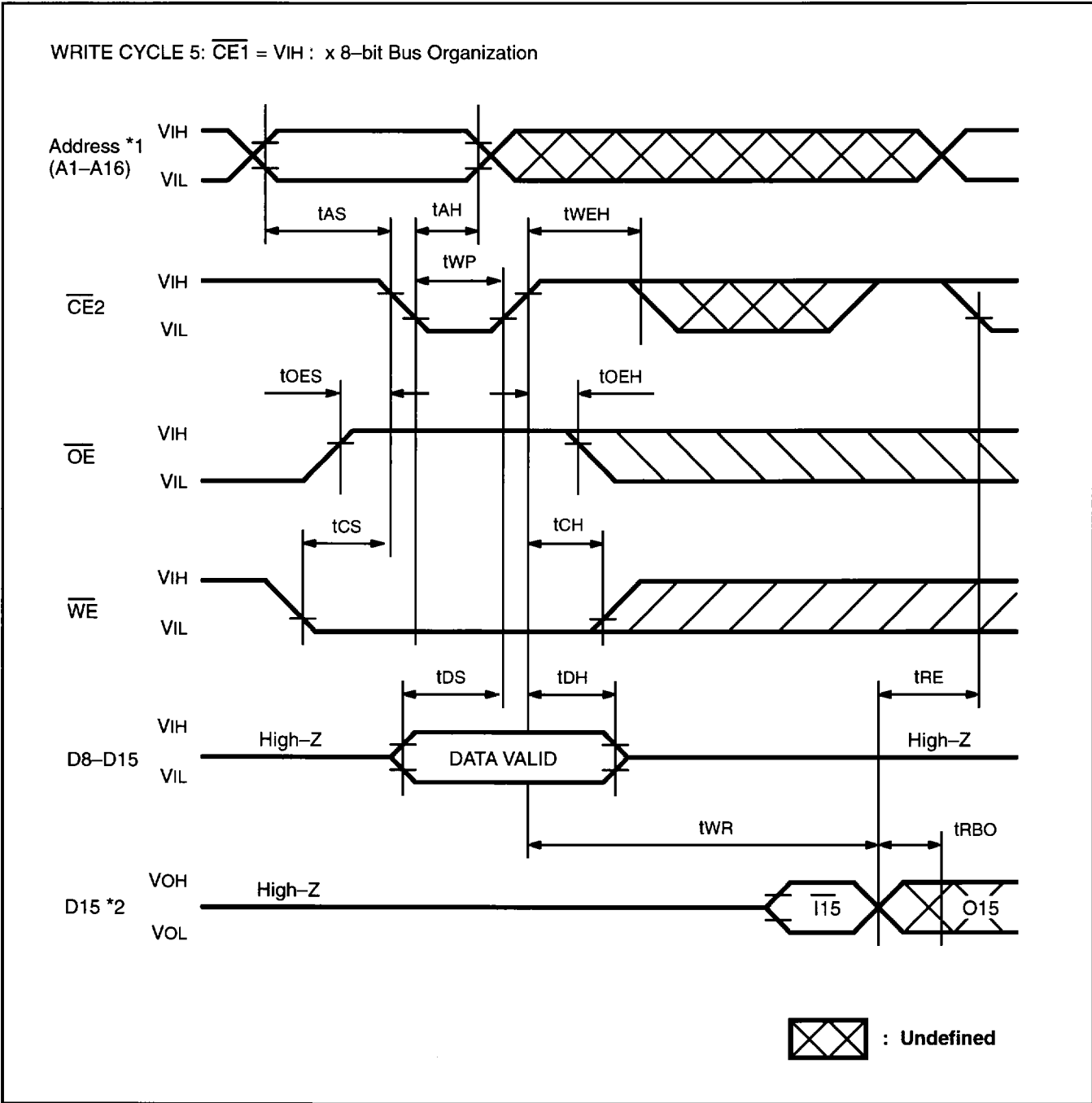


Note: \*1 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE1}$ -CONTROLLED, $\overline{REG} = V_{IH}$ )

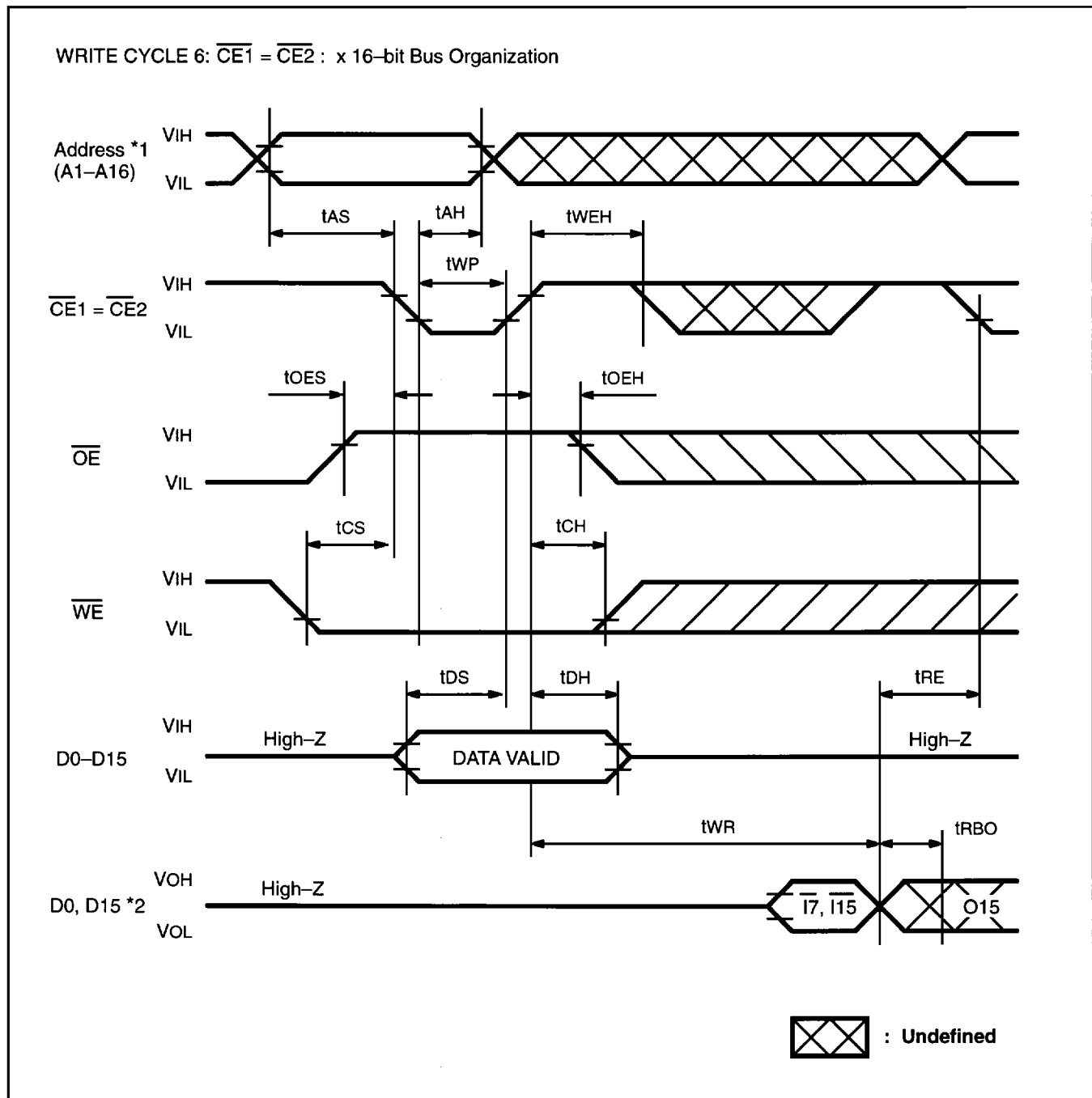


Notes: \*1  $V_0 = \text{Either } V_{IH} \text{ or } V_{IL}$ .  
 \*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### MAIN MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE} = \text{CONTROLLED}$ , $\overline{REG} = V_{IH}$ )



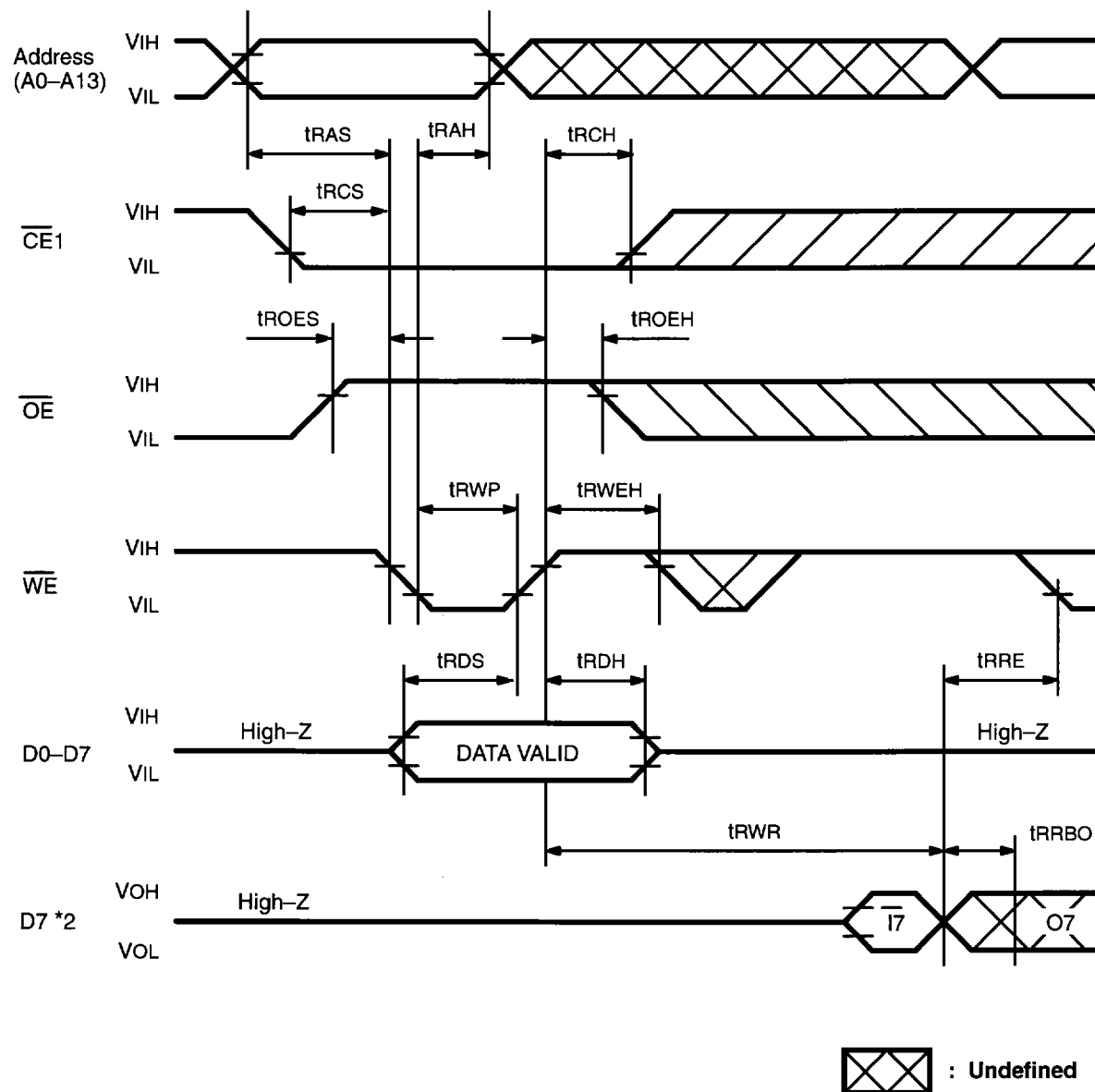
Notes: \*1 V0 = Either VIH or VIL.  
 \*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ -CONTROLLED, $\overline{REG} = V_{IL}$ ) \*1

WRITE CYCLE 1:  $\overline{CE2} = V_{IH}$  : x 8-bit Bus Organization



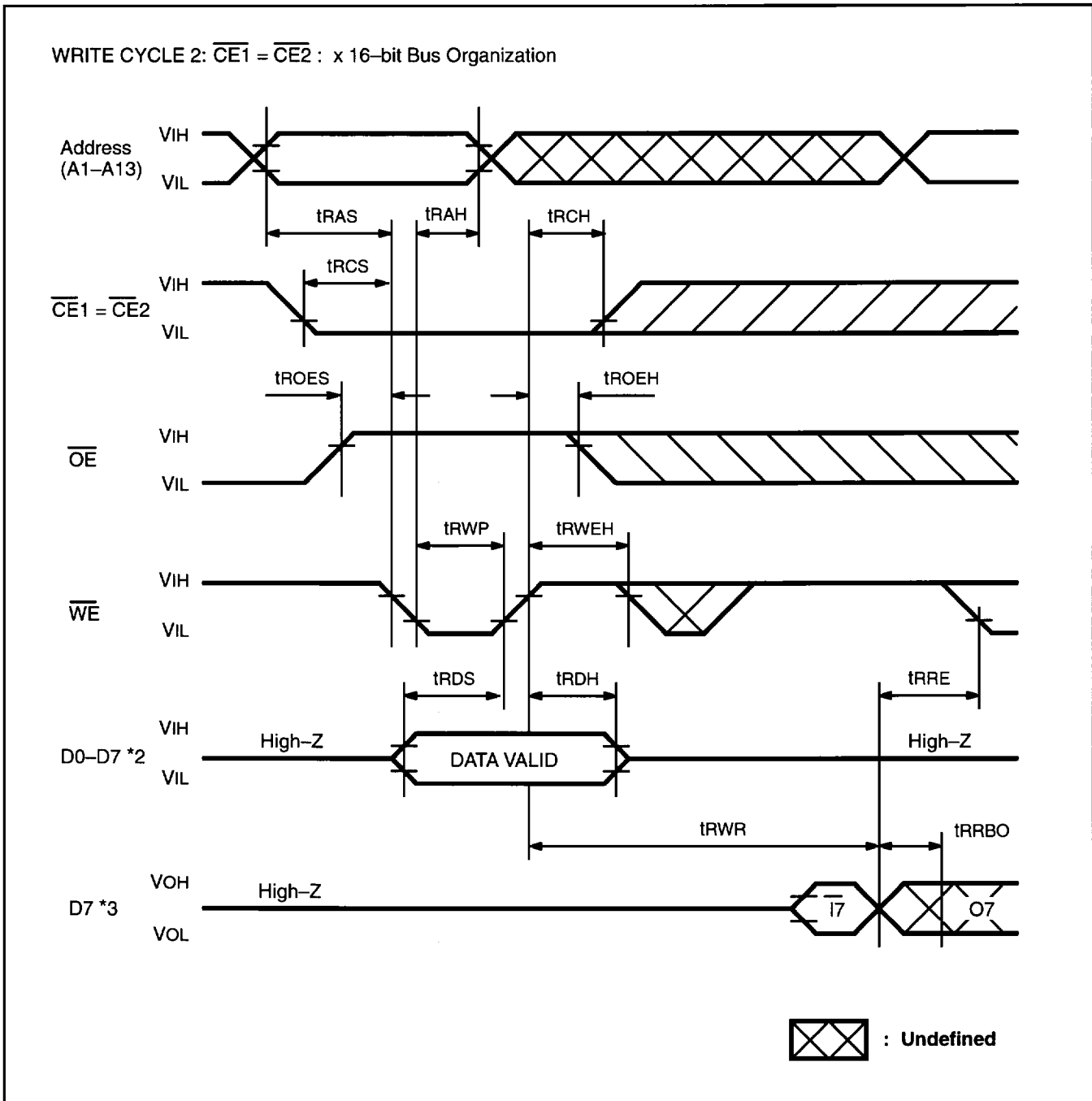
Notes: \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

\*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{WE}$ -CONTROLLED, $\overline{REG} = V_{IL}$ ) \*1



Notes: \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

\*2 Input data from D8 to D15 is invalid.

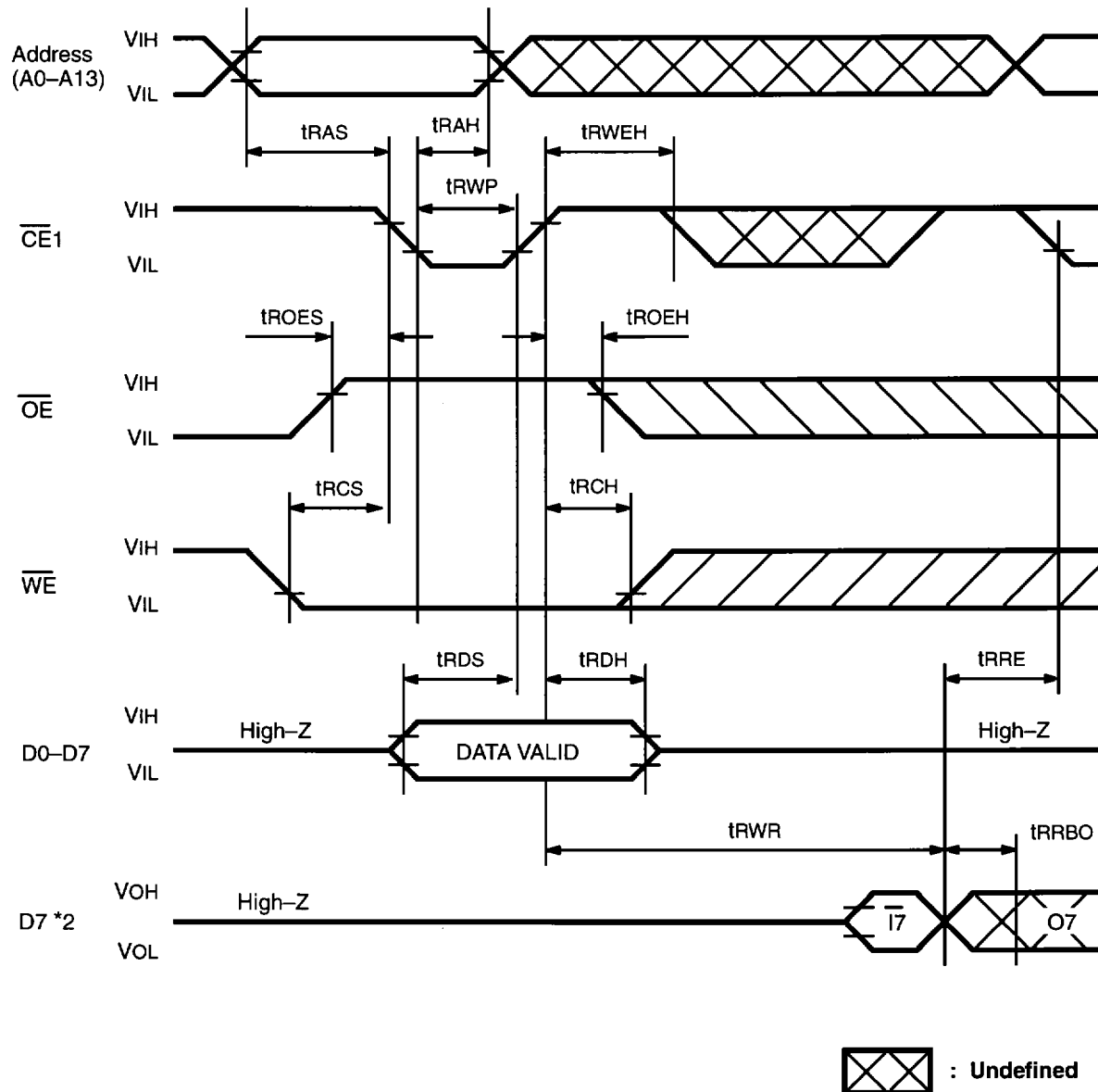
\*3 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

### ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE}2=VIH$ , $\overline{REG}=VIL$ ) \*1

WRITE CYCLE 3:  $\overline{CE}2 = VIH$  : x 8-bit Bus Organization



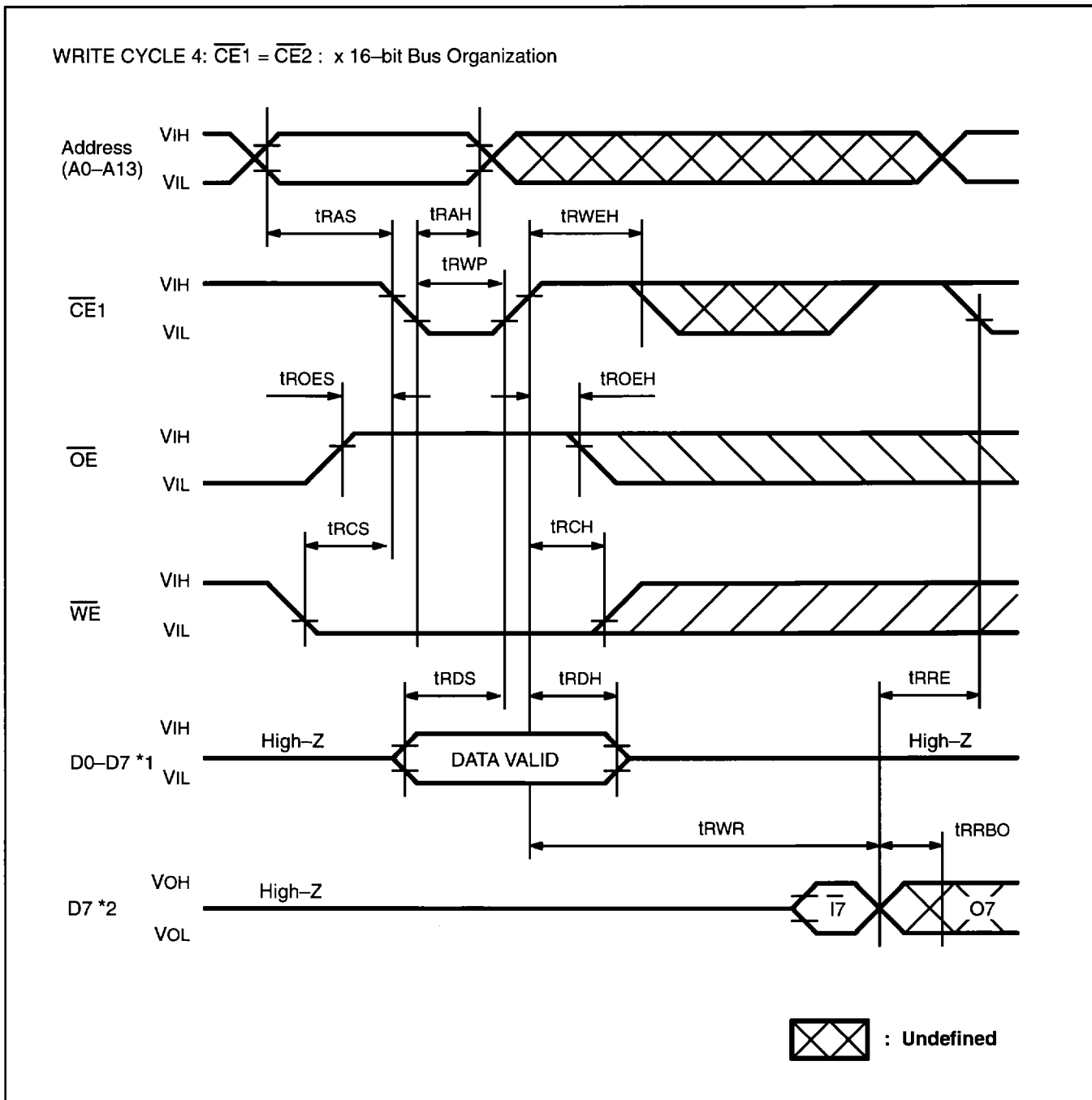
Notes: \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

\*2 Data polling operation.

## AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

ATTRIBUTE MEMORY WRITE CYCLE TIMING DIAGRAM ( $\overline{CE}$ =CONTROLLED,  $\overline{REG} = V_{IL}$ ) \*1



Notes: \*1 This timing diagram is for MB98A80403, 80503, 80603, and 80703. "FF" data is available on MB98A80402, 80502, 80602, and 80702 only.

\*2 Input data from D8 to D15 is invalid.

\*3 Data polling operation.

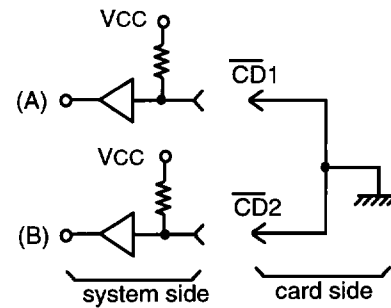
## UNIQUE FEATURES FOR EEPROM CARD

### 1. SPECIAL MONITORING PINS

#### 1.1 $\overline{CD1}$ , $\overline{CD2}$ : Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 4.)

When the memory card has been correctly inserted,  $\overline{CD1}$  and  $\overline{CD2}$  are detected by the system.  $\overline{CD1}$ ,  $\overline{CD2}$  are tied to ground on the card side as shown in Fig. 4.



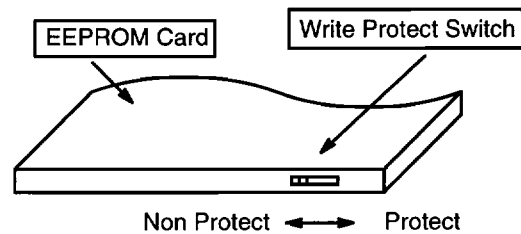
- Fig. 4 -

#### 1.2 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 5, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the "Non Protect" position and the WE pin low. L-level is output on the WP pin.

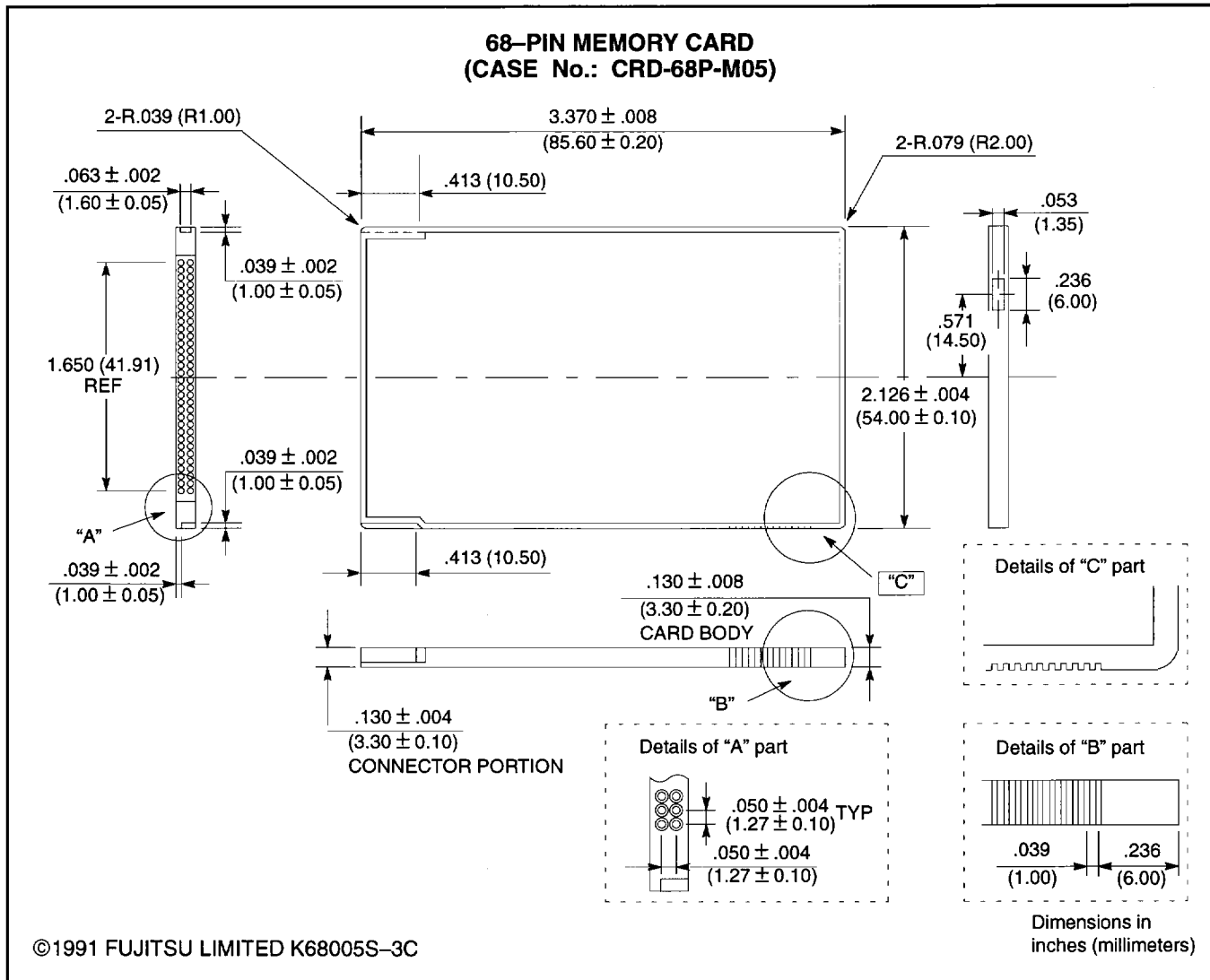
To prevent writing to the card, the switch must be turned to the "Protect" position. H-level is output on the WP pin.



- Fig. 5 -

WP Switch	WP
Protect	H
Non Protect	L

# PACKAGE DIMENSIONS



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