3357/F2847
Quad 80-Bit Static Shift Register

MOS Memory Products

Description

The 3357 and F2847 are single phase quad 80-bit static shift registers. Both have an on-chip clock generator that is driven by a single phase TTL clock. A multiplexer is provided to allow data to be entered from the input or recirculated from the output. A unique on-chip input pull-up circuit allows interfacing directly from TTL to all inputs without external components.

The 3357 and F2847 are manufactured with the p-channel Isoplanar process and are available in 16-pin ceramic or plastic dual in-line packages in the commercial temperature range.

- **4.0 MHz (33571), 3.0 MHz (F2847) AND 2.0 MHz (33572) GUARANTEED OPERATION**
- **ZERO DATA HOLD TIME**
- **TTL COMPATIBILITY**
- **SINGLE PHASE TTL CLOCK**
- **LOW CLOCK CAPACITANCE**
- **INPUT MULTIPLEXER**
- **16-PIN CERAMIC OR PLASTIC DUAL IN-LINE PACKAGE**
- **LOW POWER VERSION (F2847L)**

Pin Names

D_1-D_4	Data Inputs
REC_1-REC_4	Recirculate Inputs
CP	Clock Input
Q_1-Q_4	Data Outputs

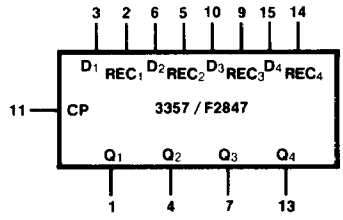
Absolute Maximum Ratings

V_{GG} and Inputs	−20 V to +0.3 V
V_{DD} and Outputs	−7.0 V to +0.3 V
Output Sink Current	10 mA
Storage Temperature	−55°C to +150°C
Operating Temperature	0°C to +70°C

All voltages with respect to V_{SS}.

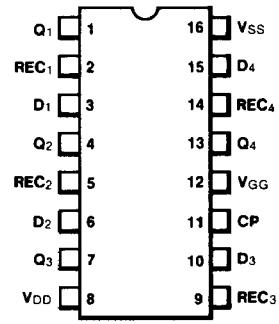
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Logic Symbol



V_{SS} = Pin 16
V_{DD} = Pin 8
V_{GG} = Pin 12

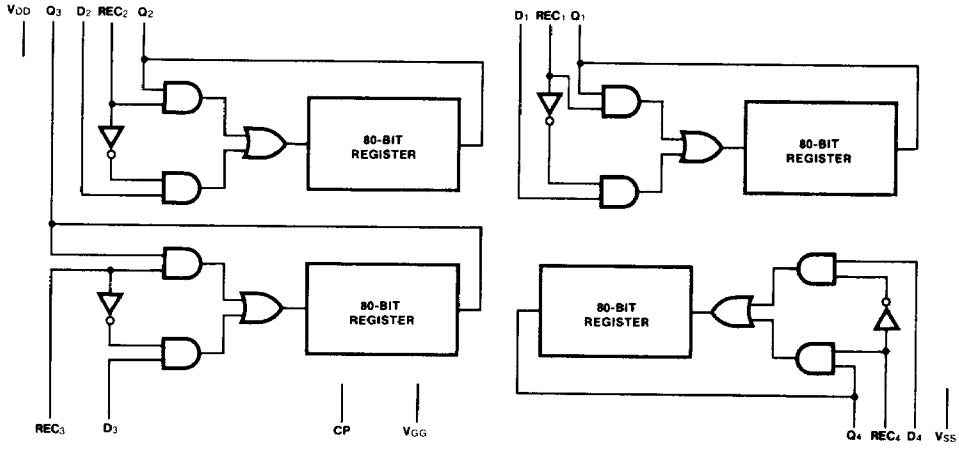
Connection Diagram 16-Pin DIP



(Top View)

Package	Outline	Order Code
Ceramic DIP	6Z	D
Plastic DIP	9B	P

Block Diagram



Functional Description

The 3357 and F2847 are single phase quad 80-bit static shift registers. Data is loaded into the register on the negative transition of the external clock. The Recirculate input loads new data from the input or recirculates old data from the output. A LOW on Recirculate loads data from the input, and a HIGH loads data from the output.

Output Characteristics

Each output will drive one unit TTL load (1.6 mA at 0.4 V) directly or another unit Shift Register load without any external components.

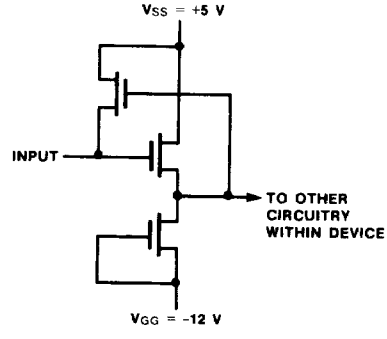
Active Pull-up Description

TTL compatibility on each input is achieved through the use of active pull-up circuits which raise the input voltage to a value meeting the V_{IH} specification, i.e., $V_{IH} \geq V_{SS} - 1.0$ V. Each of these pull-up circuits may be thought of as a switched variable impedance between the input and V_{SS} whose state is dependent upon the input voltage, V_{IN}. When V_{IN} is LOW, the input impedance is on the order of several megohms, causing the input current to look like a leakage current. As V_{IN} swings toward a TTL HIGH value, the input impedance decreases, providing a low impedance path to V_{SS}, pulling V_{IN} up to the proper V_{IH} level. Furthermore, at $V_{IN} \geq V_{IH}$, the input characteristics resemble those of a TTL device making it look like a normal TTL load.

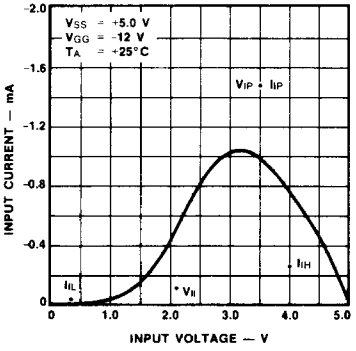
More specifically, the input current increases significantly when V_{IN} starts to exceed V_{II} (the Pull-up Initiation voltage). This current reaches a peak value of I_{IP} (the Input Barrier current) when $V_{IN} = V_{IP}$ (the Peak Input Current Voltage Point) after which it decreases as V_{IN} rises to its V_{IH} value. See Typical Input Characteristics.

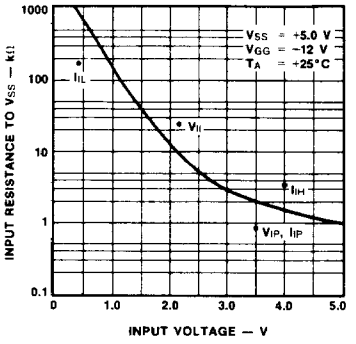
Although not usually necessary under low fan-out conditions, the active pull-up circuit on each input guarantees that the V_{IH} specification is met under all conditions where the 3357 or F2847 is driven by a TTL-like structure.

Input Buffer Stage With Active Pull-up



Typical Input Characteristics





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DC Requirements $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

Symbol	Characteristic	Min	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	$V_{SS} - 1$	$V_{SS} + 0.3$	V	Note
V_{IL}	Input LOW Voltage	V_{GG}	+0.8	V	Note

DC Characteristics $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

Symbol	Characteristic		Min	Max	Unit	Condition
V_{OH}	Output HIGH Voltage		$V_{SS} - 1$		V	$I_{OH} = -0.1$ mA
V_{OL}	Output LOW Voltage			0.4	V	$I_{OL} = 1.6$ mA
V_{II}	Input Pull-up Initiation Voltage			2.2	V	Note, $I_{IN} < -0.12$ mA
V_{IP}	Input Peak Current Voltage			$V_{SS} - 1.5$	V	Note
I_{IP}	Input Peak Current			−1.6	mA	Note
I_{IH}	Input HIGH Current		−0.22		mA	Note, $V_{IN} = V_{SS} - 1.0$ V
I_{IL}	Input LOW Current			−30	μA	Note, $V_{IN} = 0.4$ V
I_{DD}	V_{DD} Current	3357-1		−20	mA	Max Operating Frequency
		3357-2		−18	mA	
		F2847L		−20	mA	
		F2847		−35	mA	
I_{GG}	V_{GG} Current	3357-1		−15	mA	
		3357-2		−10.5	mA	
		F2847L		−12	mA	
		F2847		−15	mA	
P_D	Power Dissipation	3357-1		375	mW	
		3357-2		285	mW	
		F2847L		320	mW	
		F2847		455	mW	

Note
Applies to all inputs including Clock.

AC Requirements $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

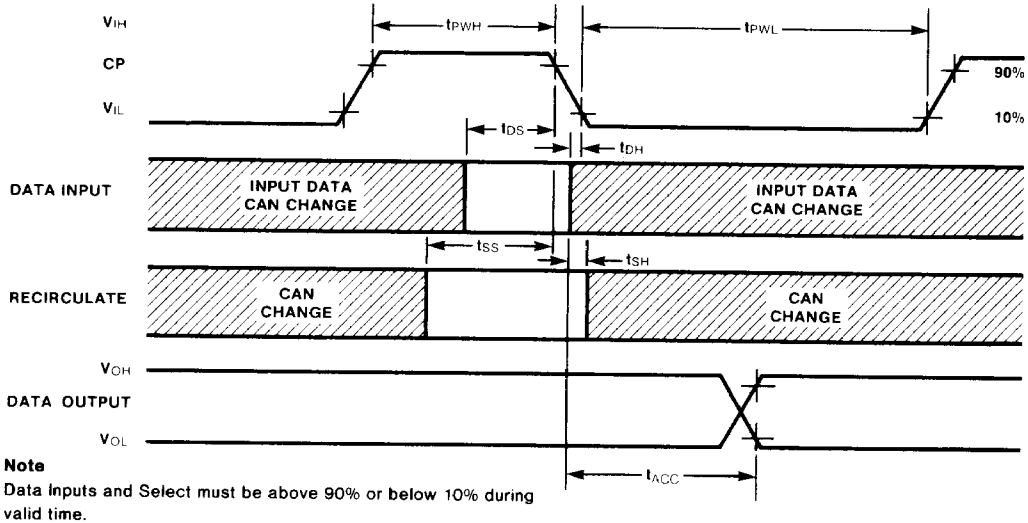
Symbol	Characteristic	3357-1		F2847-F2847L		3357-2		Unit	Condition
		Min	Max	Min	Max	Min	Max		
f	Operating Frequency	0	4.0	0	3.0	0	2.0	MHz	
t_{PWH}	Clock Pulse Width HIGH	0.095	100	0.14	100	0.25	100	μs	See Timing Diagram, Note
t_{PWL}	Clock Pulse Width LOW	0.135		0.14		0.25		μs	
t_{DS}	Data Set-up Time	25		120		40		ns	
t_{DH}	Data Hold Time	30		40		30		ns	
t_{SS}	Select Set-up Time	40		70		70		ns	
t_{SH}	Select Hold Time	10		10		10		ns	

AC Characteristics $T_A = 0°C$ to $+70°C$, $V_{SS} = +5.0\ V \pm 5\%$, $V_{DD} = 0\ V$, $V_{GG} = -12\ V \pm 5\%$

Symbol	Parameter		Min	Max	Unit	Condition
C_{IN}	Input Capacitance			5.0	pF	All inputs
C_{OUT}	Output Capacitance			5.0	pF	
t_{ACC}	Clock to Output Delay Time	3357-1		215	ns	See Timing Diagram
		3357-2		260		
		F2847L		200		
		F2847		200		

Note
t_r, t_f = Clock Transition Time = 0.5 μs.

Timing Diagram



Note
Data Inputs and Select must be above 90% or below 10% during valid time.