



Integrated Device Technology, Inc.

2 x 16K x 64 DATA/INSTRUCTION CACHE MODULE FOR GENERAL PURPOSE CPUs

IDT7MB6040

FEATURES:

- High-speed 256K-Byte CMOS static RAM module constructed to support general purpose CPUs as a complete data and instruction cache
- Supports operating frequencies of 12MHz, 16.7MHz, 20MHz, 25MHz and 33MHz
- Available in a high-density, low profile 128-pin QIP (quad in-line package)
- Surface mounted SO's on a multilayer epoxy substrate (FR-4)
- Multiple ground pins for maximum noise immunity
- TTL-compatible I/Os
- Single 5V ($\pm 10\%$) power supply

DESCRIPTION:

The IDT7MB6040 is a 256K-byte high-speed CMOS static RAM cache module constructed on a multilayer epoxy substrate (FR-4), using 32 (16K x 4) RAMs and 8 IDT74FCT373 latches.

The IDT7MB6040 is organized as two separate banks of 16K x 64 with the IDT74FCT373s being used as address latches. The two banks of RAM with their associated address latches share a common 14-bit ADDRESS bus and common 64-bit DATA bus. The chip select, write enable, RAM output enable and latch enable controls for the two banks are brought out separately to support interleaving access to the banks of RAM. Each bank of address latches reduce the capacitance loading on the outputs of the latches; thereby, enhancing CPU performance.

All inputs and outputs of the IDT7MB6040 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation.

PIN CONFIGURATION⁽¹⁾

GND	1	65 GND	Vcc	128	64	Vcc
D ₀	2	66 D ₁	D ₆₂	127	63	D ₆₃
D ₂	3	67 D ₃	D ₆₀	126	62	D ₆₁
D ₄	4	68 D ₅	D ₅₈	125	61	D ₅₉
D ₆	5	69 D ₇	D ₅₆	124	60	D ₅₇
D ₈	6	70 D ₉	GND	123	59	D ₅₅
WE ₁	7	71 OE ₁	WE ₄	122	58	OE ₄
CS ₁	8	72 GND	D ₅₄	121	57	CS ₁₄
CS ₅	9	73 D ₁₀	D ₅₃	120	56	CS ₁₈
WE ₅	10	74 OE ₅	WE ₈	119	55	OE ₈
D ₁₁	11	75 D ₁₂	D ₅₁	118	54	D ₅₂
D ₁₃	12	76 Vcc	GND	117	53	D ₅₀
A ₀	13	77 A ₁	A ₁₂	116	52	A ₁₃
A ₂	14	78 A ₃	A ₁₀	115	51	A ₁₁
A ₄	15	79 A ₅	A ₈	114	50	A ₉
D ₁₄	16	80 GND	A ₆	113	49	A ₇
CS ₂₁	17	81 LE ₁	LE ₂	112	48	CS ₂₂
CS ₂₃	18	82 LE ₃	LE ₄	111	47	CS ₂₄
D ₁₅	19	83 D ₁₆	GND	110	46	D ₄₉
D ₁₇	20	84 Vcc	D ₄₇	109	45	D ₄₈
D ₁₈	21	85 D ₁₉	D ₄₅	108	44	D ₄₆
D ₂₀	22	86 D ₂₁	D ₄₃	107	43	D ₄₄
WE ₂	23	87 OE ₂	WE ₇	106	42	OE ₇
CS ₂	24	88 GND	GND	105	41	CS ₁₇
CS ₆	25	89 D ₂₂	D ₄₂	104	40	CS ₁₃
WE ₆	26	90 OE ₆	WE ₃	103	39	OE ₃
D ₂₃	27	91 D ₂₄	D ₄₀	102	38	D ₄₁
D ₂₅	28	92 D ₂₆	Vcc	101	37	D ₃₉
D ₂₇	29	93 D ₂₈	D ₃₇	100	36	D ₃₈
D ₂₉	30	94 D ₃₀	D ₃₅	99	35	D ₃₆
D ₃₁	31	95 D ₃₂	D ₃₃	98	34	D ₃₄
Vcc	32	96 Vcc	GND	97	33	GND

QIP
TOP VIEW

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PIN NAMES

D ₀ - D ₆₃	Data Inputs/Outputs
A ₀ - A ₁₃	Address Inputs
LE ₁ - LE ₄	Latch Enables
CS ₁₁ - CS ₁₈	RAM Selects
CS ₂₁ - CS ₂₄	RAM Selects
WE ₁ - WE ₈	Write Enables
OE ₁ - OE ₈	Output Enables
GND	Ground
Vcc	Power

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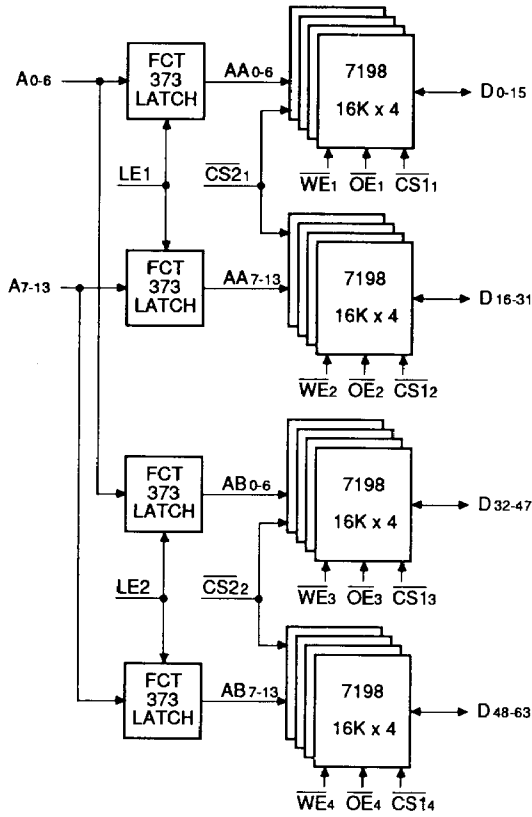
NOTE:

1. For module dimensions, please refer to module drawing M28 in the packaging section.

COMMERCIAL TEMPERATURE RANGE

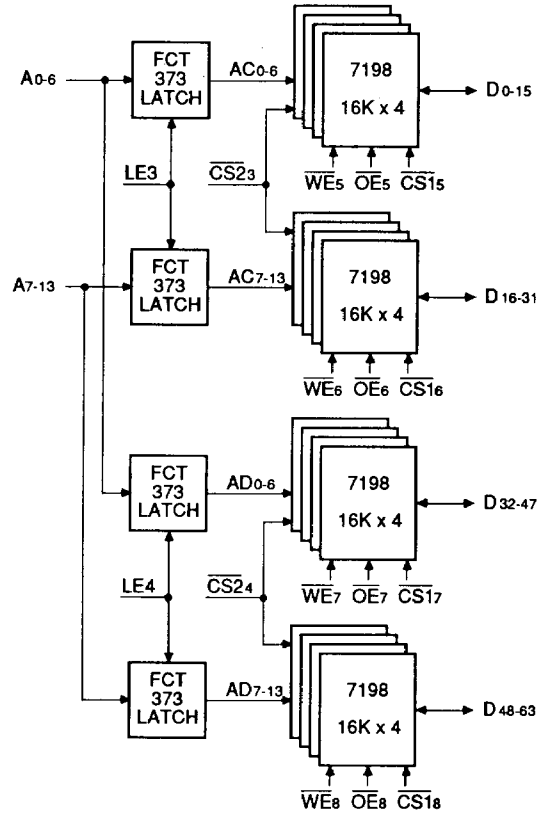
SEPTEMBER 1990

DATA CACHE



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INSTRUCTION CACHE



2743 drw 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	-10 to +85	°C
TSTG	Storage Temperature	-55 to +125	°C
IOUT	DC Output Current	50	mA

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NOTE:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V _{IH}	Input High Voltage	2.2	—	6.0	V
V _{IL}	Input Low Voltage	-0.5 ⁽¹⁾	—	0.8	V

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NOTE:

- V_{IL}(min.) = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	VCC
Commercial	0°C to +70°C	0V	5.0V ± 10%

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DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

Symbol	Parameter	Test Conditions	12MHz		16.7MHz		20MHz		25MHz		33MHz		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
I _{LI}	Input Leakage Current	VCC = Max. VIN = GND to VCC	—	20	—	20	—	20	—	20	—	20	µA
I _{LO}	Output Leakage Current	VCC = Max., CS = VIH, VOUT = GND to VCC	—	10	—	10	—	10	—	10	—	10	µA
I _{CC1}	Operating Current	f = 0, CS = VIL, VCC = Max., Outputs Open	—	3000	—	3000	—	3000	—	3600	—	4000	mA
I _{CC2}	Dynamic Operating Current	VCC = Max., CS = VIL, f = fMAX Outputs Open	—	3750	—	3750	—	4050	—	4500	—	4800	mA
I _{SB1}	Full Standby Supply Current	CS ≥ VCC - 0.2V, VIN ≥ VCC - 0.2V or ≤ 0.2V	—	450	—	450	—	450	—	600	—	960	mA
I _{SB}	Standby Power Supply Current	VCC = Max., CS = VIH, f = fMAX Outputs Open	—	1500	—	1500	—	1650	—	1800	—	2000	mA
VOH	Output High Voltage	VCC = Min., IOH = -4mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
VOL	Output Low Voltage	VCC = Min., IOL = 8mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V

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AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

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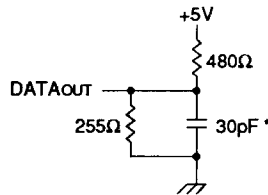
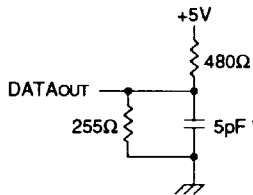


Figure 1. Output Load



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Figure 2. Output Load
(for toLZ, toHZ)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ± 10%, TA = 0°C to +70°C)

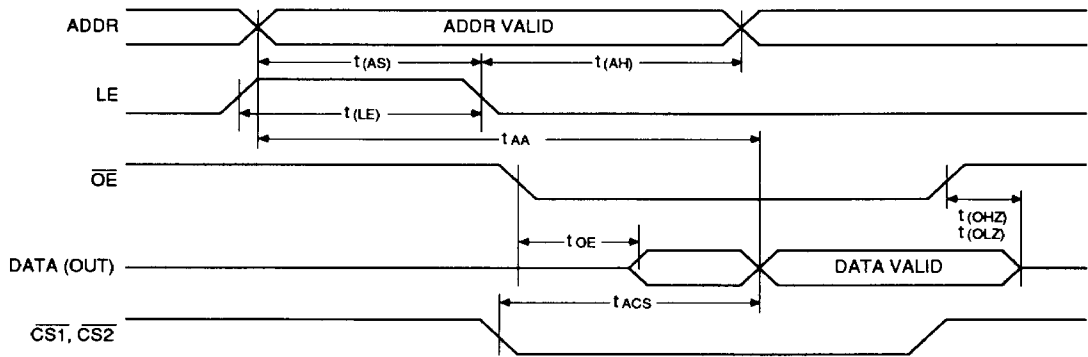
Symbol	Parameter	12MHz		16.6MHz		20MHz		25MHz		33MHz		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAA ⁽²⁾	Address Access Time	—	45	—	35	—	30	—	25	—	20	ns
tACS	Chip Select Time	—	40	—	30	—	25	—	20	—	15	ns
tOE	Output Enable Time	—	22	—	17	—	11	—	8	—	5	ns
toHZ ⁽¹⁾	Output Disable to Output in High Z	2	16	2	14	2	10	2	8	2	6	ns
toLZ ⁽¹⁾	Output Disable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tLE	Latch Enable Width	8	—	6	—	6	—	6	—	6	—	ns
tAS	Address Setup Time to LE	4	—	2	—	2	—	2	—	2	—	ns
tAH	Address Hold Time from LE	3	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
tAW ⁽²⁾	Address Valid to End of Write	40	—	30	—	25	—	23	—	20	—	ns
tCW	Chip Select to End of Write	35	—	25	—	20	—	18	—	15	—	ns
tWP	Write Pulse Width	30	—	25	—	20	—	17	—	12	—	ns
tDW	Data Valid to End of Write	20	—	13	—	13	—	11	—	8	—	ns
tDH	Data Hold Time	0	—	0	—	0	—	0	—	0	—	ns

NOTE:

1. This parameter is guaranteed by design but not tested.
2. LE already asserted.

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TIMING WAVEFORM OF READ CYCLE⁽¹⁾

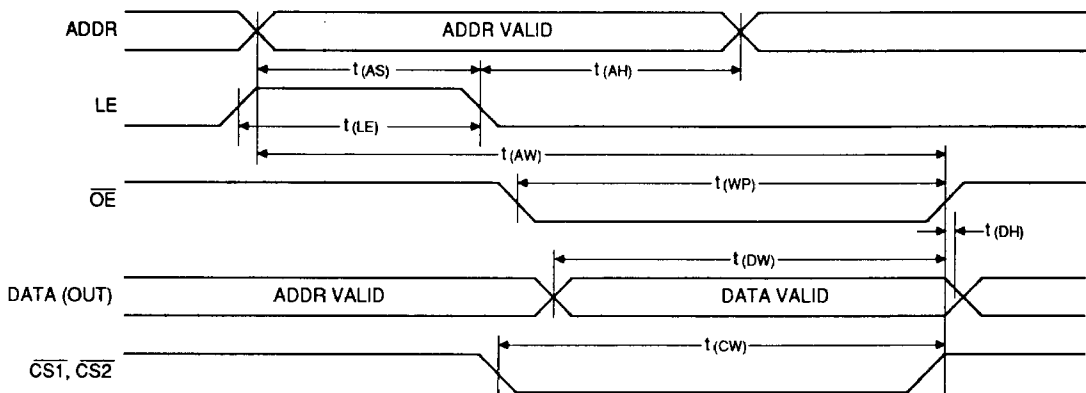


2743 drw 05

NOTES:

1. WE and CS must be High for all address transitions.
2. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF WRITE CYCLE⁽¹⁾



2743 drw 06

NOTE:

1. A write occurs (t_{wp}) during the overlap of a Low CS and WE and a High LE.

TRUTH TABLE

Mode	CS1	CS2	OE	WE	Output	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	H	X	X	High Z	Standby
Read	L	L	L	H	DOUT	Active
Read	L	L	H	H	High Z	Active
Write	L	L	X	L	DIN	Active

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CAPACITANCE⁽¹⁾ (TA = +25°C, f = 1.0MHz)

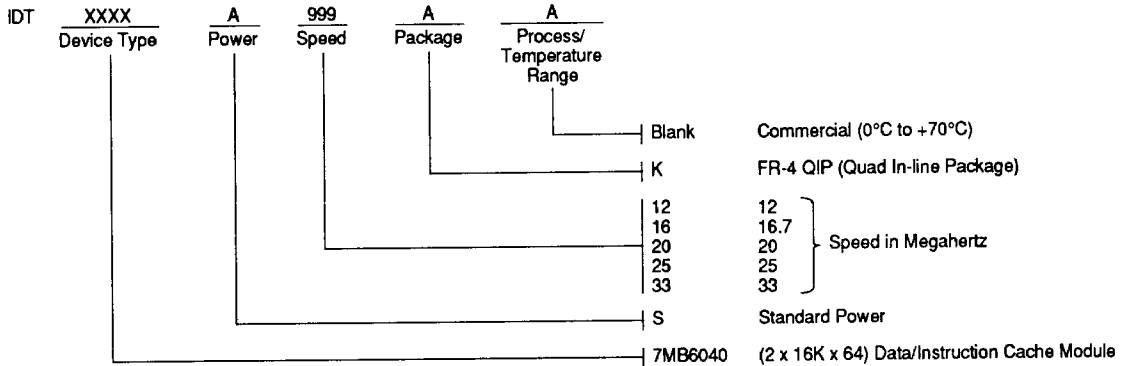
Symbol	Parameter	Conditions	Typ.	Unit
CIN	Input Capacitance	VIN = 0V	60	pF
COU	Output Capacitance	VOUT = 0V	20	pF

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NOTE:

1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



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