

74AC/ACT11379

Quad D-Type Flip-Flop w/ Data Enable

Preliminary Specification

ACL Products

FEATURES

- Output capability: ± 24 mA
- Edge-triggered D-type inputs
- Positive edge-triggered clock
- Common asynchronous Enable (\bar{E}) Input
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11379 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11379 provides four edge-triggered D-type flip-flops with individual Data inputs ($D_0 - D_3$) and Q and \bar{Q} outputs. The flip-flops load the data on the rising edge of the common clock (CP) providing that the common Enable (\bar{E}) is held Low. When the Enable is High, the flip-flops hold their previous state.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS $T_A = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n or \bar{Q}_n	$C_L = 50\text{pF}$	4.8	5.3	ns
C_{PD}	Power dissipation capacitance per flip-flop ¹	$f = 1\text{MHz}; C_L = 50\text{pF}$	38	38	pF
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jeduc JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	$C_L = 50\text{pF}$	165	165	MHz

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

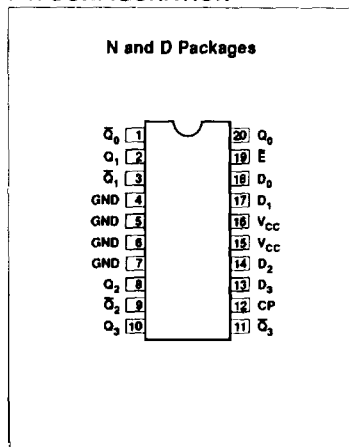
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

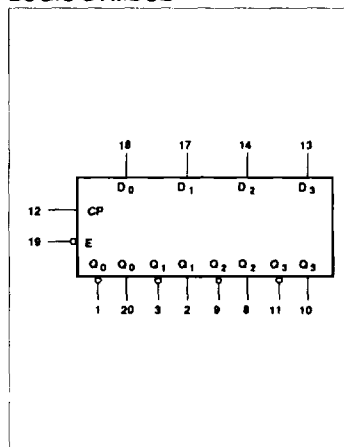
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11379N 74ACT11379N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11379D 74ACT11379D

PIN CONFIGURATION

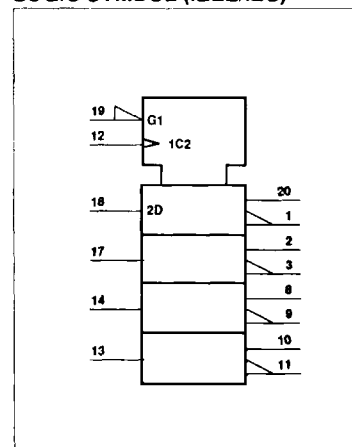


March 17, 1989

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Quad D-Type Flip-Flop w/Data Enable

74AC/ACT11379

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	$D_0 - D_3$	Data inputs
20, 2, 8, 10	$Q_0 - Q_3$	Data outputs
1, 3, 9, 11	$\bar{Q}_0 - \bar{Q}_3$	Data outputs (complements of Q_n outputs)
19	\bar{E}	Data enable input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\bar{E}	CP	D_n	Q_n	\bar{Q}_n
Disabled input (hold)	H	\uparrow	X	NC	NC
Load "1" (set)	L	\uparrow	h	H	L
Load "0" (reset)	L	\uparrow	l	L	H

H = High voltage level steady state

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level steady state

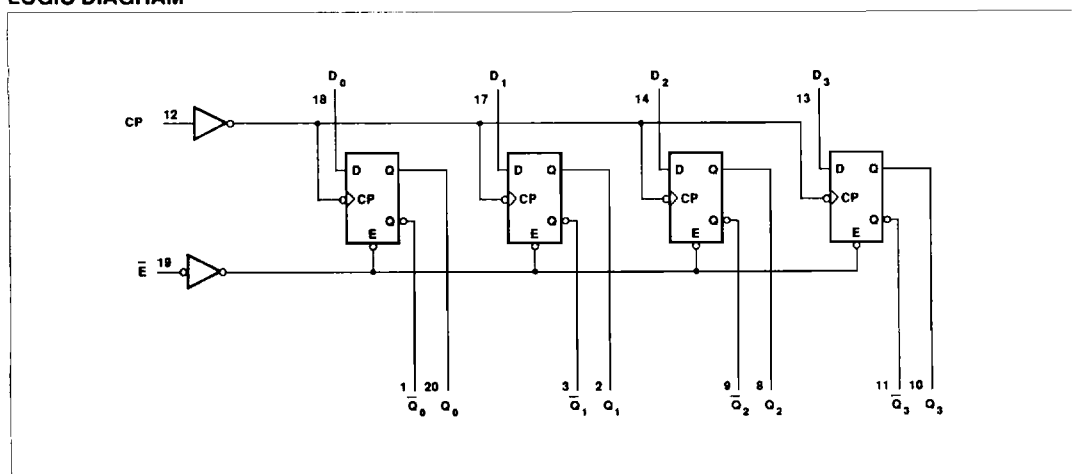
l = Low voltage level one set-up time prior to the Low-to-High clock transition

X = Don't care

NC = No Change

 \uparrow = Low-to-High clock transition

LOGIC DIAGRAM



Quad D-Type Flip-Flop w/Data Enable

74AC/ACT11379

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11379			74ACT11379			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0 ¹	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta V/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK} or V_I	DC input diode current ²	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to $V_{CC} + 0.5$	V
I_{OK} or V_O	DC output diode current ²	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to $V_{CC} + 0.5$	V
I_O	DC output source or sink current per output pin	$V_O = 0$ to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C: derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C: derate linearly by 6mW/K	400	

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Quad D-Type Flip-Flop w/Data Enable

74AC/ACT11379

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	V _{CC}	74AC11379				74ACT11379				UNIT	
				T _A = +25°C		T _A = -40°C T _O +85°C		T _A = +25°C		T _A = -40°C T _O +85°C			
				Min	Max	Min	Max	Min	Max	Min	Max		
V _{IH}	High-level input voltage		3.0	2.10		2.10						V	
			4.5	3.15		3.15		2.0		2.0			
			5.5	3.85		3.85		2.0		2.0			
V _{IL}	Low-level input voltage		3.0		0.90		0.90					V	
			4.5		1.35		1.35		0.8		0.8		
			5.5		1.65		1.65		0.8		0.8		
V _{OH}	High-level output voltage	V _I = V _{IL} or V _{IH}	I _{OH} = -50μA	3.0	2.9		2.9					V	
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I _{OH} = -4mA	3.0	2.58		2.48						
				4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
I _{OH} = -24mA	3.0												
I _{OH} = -75mA ¹	5.5			3.85				3.85					
V _{OL}	Low-level output voltage	V _I = V _{IL} or V _{IH}	I _{OL} = 50μA	3.0		0.1		0.1				V	
				4.5		0.1		0.1		0.1			0.1
				5.5		0.1		0.1		0.1			0.1
			I _{OL} = 12mA	3.0		0.36		0.44					
				4.5		0.36		0.44		0.36			0.44
				5.5		0.36		0.44		0.36			0.44
I _{OL} = 24mA	3.0												
	5.5				1.65				1.65				
I _{OL} = 75mA ¹	5.5												
I _I	Input leakage current	V _I = V _{CC} or GND	5.5		±0.1		±1.0		±0.1		±1.0	μA	
I _{CC}	Quiescent supply current	V _I = V _{CC} or GND, I _O = 0	5.5		8.0		80		8.0		80	μA	
ΔI _{CC}	Supply current, TTL inputs High ²	One input at 3.4V, other inputs at V _{CC} or GND	5.5						0.9		1.0	mA	

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Quad D-Type Flip-Flop w/Data Enable

74AC/ACT11379

AC ELECTRICAL CHARACTERISTICS AT 3.3V \pm 0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	130	155		130		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , \bar{Q}_n	1	1.5 1.5	5.0 8.3	7.1 10.4	1.5 1.5	7.7 11.2	ns
t_{S}	Setup time, High or Low D_n to CP	1	7.0			7.0		ns
t_{H}	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_{S}	Setup time, High or Low \bar{E} to CP	1	4.5			4.5		ns
t_{H}	Hold time, High or Low CP to \bar{E}	1	0.0			0.0		ns
t_{W}	Clock pulse width High or Low	1	4.0			4.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V \pm 0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11379					UNIT
			$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	140	165		140		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n , \bar{Q}_n	1	1.5 1.5	3.8 5.9	5.3 7.6	1.5 1.5	5.8 8.4	ns
t_{S}	Setup time, High or Low D_n to CP	1	5.0			5.0		ns
t_{H}	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_{S}	Setup time, High or Low \bar{E} to CP	1	3.0			3.0		ns
t_{H}	Hold time, High or Low CP to \bar{E}	1	0.5			0.5		ns
t_{W}	Clock pulse width High or Low	1	3.5			3.5		ns

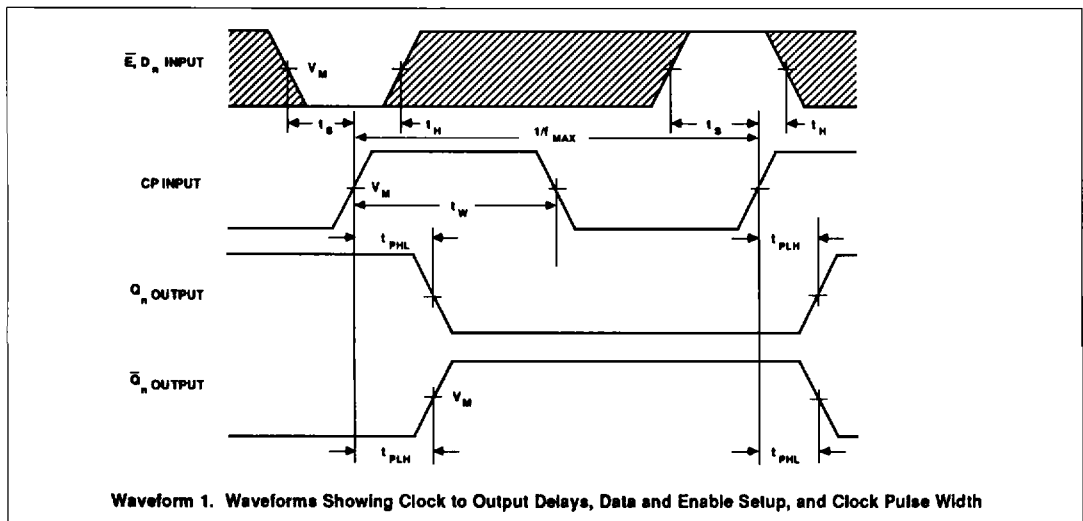
Quad D-Type Flip-Flop w/Data Enable

74AC/ACT11379

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11379					UNIT
			T _A = +25°C			T _A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum clock frequency	1	140	165		140		MHz
t _{PLH} t _{PHL}	Propagation delay CP to Q _n , Q _n	1	1.5 1.5	4.3 6.4	5.6 7.9	1.5 1.5	6.1 8.7	ns
t _S	Setup time, High or Low D _n to CP	1	4.5			4.5		ns
t _H	Hold time, High or Low CP to D _n	1	0.5			0.5		ns
t _S	Setup time, High or Low E to CP	1	3.0			3.0		ns
t _H	Hold time, High or Low CP to E	1	1.0			1.0		ns
t _W	Clock pulse width High or Low	1	3.5			3.5		ns

AC WAVEFORMS



Waveform 1. Waveforms Showing Clock to Output Delays, Data and Enable Setup, and Clock Pulse Width

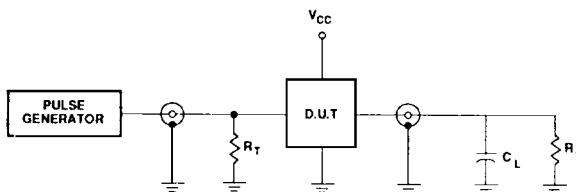
WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V _{IN} = GND to V _{CC} , V _M = 50% V _{CC}	V _{OUT} = V _{OL} to V _{OH}
ACT	V _{IN} = GND to 3.0V, V _M = 1.5V	V _M = 50% V _{CC}

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TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500 Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR \leq 10MHz

$t_r = t_f = 3ns$