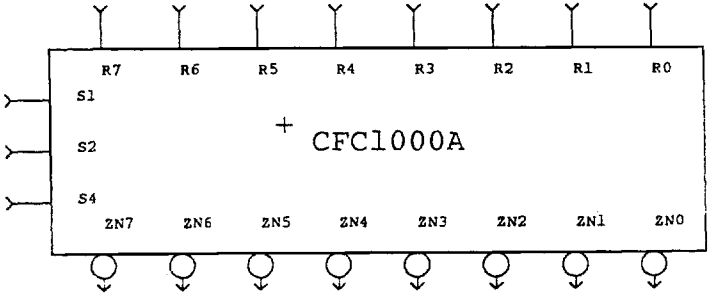
CFC1000A 8-bit Barrel Shifter

DESCRIPTION: CFC1000A performs an 8-bit end-around shift, or what is commonly known as a barrel shift. There are three control lines (S1, S2, and S4) to determine how many places to the left the 8-bit inputs (R7 through R0) will be shifted at the outputs (ZN7 through ZN0). All outputs are inverted.

The shifting is accomplished in three stages. Each stage contains 2 to 1 MUXs to select no shift or a shift of its inputs. The first stage selects no shift or a shift of one to the left from its inputs, depending on S1. The second stage selects no shift or a shift of two, depending on S2. Finally, S4 tells stage three to perform no shift or a shift of four to the left of its outputs.

LOGIC SYMBOL:



INPUTS (LOADING IN TRANSISTOR PAIRS):
R7(8),R6(8),R5(8),R4(8),R3(8),R2(8),R1(8),
R0(8),S1(4.5),S2(4.5),S4(4.5)

OUTPUTS (DRIVE IN #P,#N):
ZN7(2,2),ZN6(2,2),ZN5(2,2),ZN4(2,2),ZN3(2,2),
ZN2(2,2),ZN1(2,2),ZN0(2,2)

GATE COUNT: GATES USED = 79
AREA USED = 79

CFC1000A

TRUTH TABLE:

S4	S2	S1	ZN7	ZN6	ZN5	ZN4	ZN3	ZN2	ZN1	ZN0
0	0	0	RN7	RN6	RN5	RN4	RN3	RN2	RN1	RN0
0	0	1	RN6	RN5	RN4	RN3	RN2	RN1	RN0	RN7
0	1	0	RN5	RN4	RN3	RN2	RN1	RN0	RN7	RN6
0	1	1	RN4	RN3	RN2	RN1	RN0	RN7	RN6	RN5
1	0	0	RN3	RN2	RN1	RN0	RN7	RN6	RN5	RN4
1	0	1	RN2	RN1	RN0	RN7	RN6	RN5	RN4	RN3
1	1	0	RN1	RN0	RN7	RN6	RN5	RN4	RN3	RN2
1	1	1	RN0	RN7	RN6	RN5	RN4	RN3	RN2	RN1

AC CHARACTERISTICS:

PATH	10K TYP.DELAY(NS)
R(I) TO OUTPUT ZN(I)	5.8
S(I) TO OUTPUT ZN(I)	7.6

*ASSUMING OUTPUT LOADING OF 3