

## FEATURES

- SONET/SDH and ATM Compatible
- Seamless operation with PMC-Sierra PM5345 SUNI, VTI VNS67200 Quad UNI Processor, IgT WAC-013-B ATM UNI Processor and NEC  $\mu$ PD98402
- Supports clock and data recovery from 51.84 Mbit/s or 155.52 Mbit/s NRZ or NRZI data stream
- 155.52MHz clock multiplication from 19.44MHz source or 51.84MHz clock multiplication from 6.48MHz source
- Line Receiver Inputs: No external buffering needed
- Differential output buffering
- Link Status Indication
- Loop-back testing
- 100K ECL compatible I/O
- Single +5 volt power supply
- 28-pin SOIC
- Replacement for Cypress CY7B952
- Complies with Bellcore, ITU/CCITT and ANSI Specifications

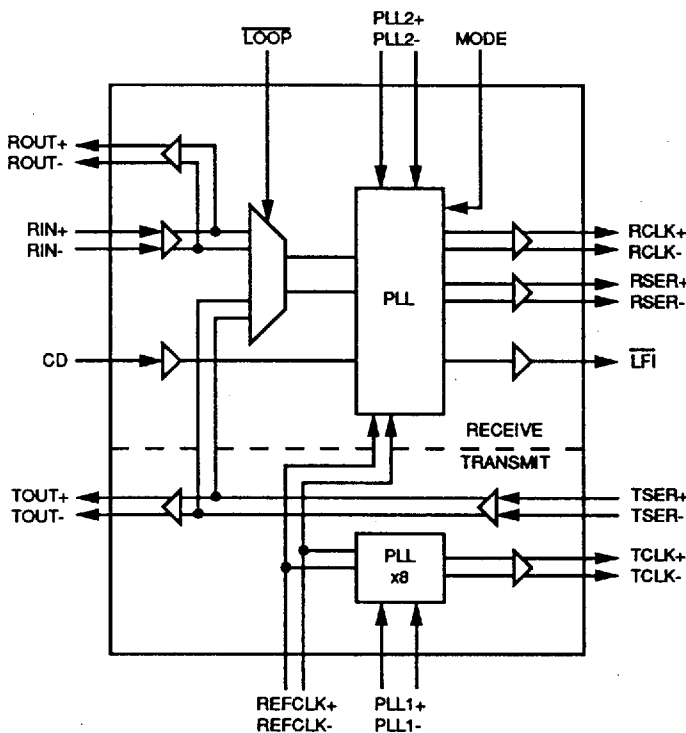
## DESCRIPTION

Synergy's SY69952 is designed to provide high performance clock recovery and generation for either 51.84 Mbit/s OC/STS-1 or 155.52 Mbit/s OC/STS-3 SONET/SDH and ATM applications. The SY69952 is ideally suited for SONET-based ATM applications, and is fabricated in Synergy's proprietary ASSET bipolar process.

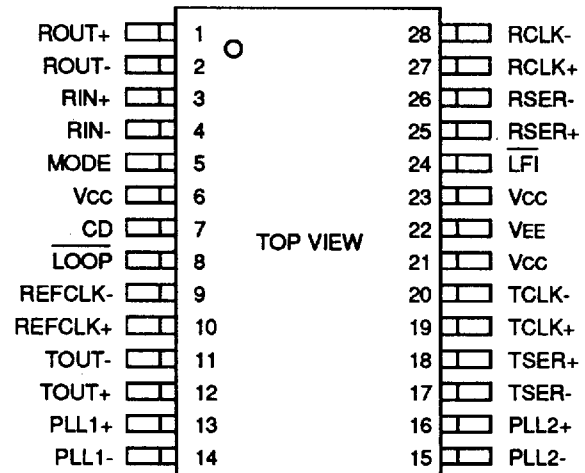
The SY69952 recovers clock and data information from a 51.84 Mbit/s or 155.52 Mbit/s, NRZ or NRZI, serial data stream. It also provides differential buffering for the transmit data.

Synergy's circuit design techniques coupled with ASSET technology result in high-performance, low-power products that achieve outstanding reliability in high volume production.

## FUNCTIONAL BLOCK DIAGRAM



## PINOUT



## PIN DESCRIPTIONS

### RIN± – Differential PECL Input

Receive Input. These built-in line receiver inputs are connected to the differential Receive serial input data stream. An internal Receive PLL recovers the embedded clock (RCLK±) and data (RSER±) information. The incoming data rate can be within one of two frequency ranges depending on the state of the MODE pin.

### ROUT± – Differential PECL Output

Receive Output. These Positive ECL 100K outputs (+5V referenced) represent the buffered version of the input data stream (RIN±). This output pair can be used for Receiver input data equalization in copper based systems, reducing the system impact of data dependent jitter. All PECL outputs can be powered down by connecting both outputs to Vcc or leaving them both unconnected.

### RSER± – Differential PECL Output

Recovered Serial Data. These Positive ECL 100K outputs (+5V referenced) represent the recovered data from the input data stream (RIN±). This recovered data is aligned with the recovered clock (RCLK±) with a sampling window compatible with most data processing devices.

### RCLK± – Differential PECL Output

Recovered Clock. These Positive ECL 100K outputs (+5V referenced) represent the recovered clock from the input data stream (RIN±). This recovered clock is used to sample the recovered data (RSER±) and has timing compatible with most data processing devices.

### CD – PECL/TTL Input

Carrier Detect. This input controls the recovery function of the Receive PLL and can be driven by the carrier detect output from optical modules or from external transition detection circuitry. When this input is at an ECL HIGH, the input data stream (RIN±) is recovered normally by the Receive PLL. When this input is at an ECL LOW, the Receive PLL no longer aligns to RIN±, but instead aligns with the REFCLKx8 frequency. Also, the Link Fault Indicator (LFI) will transition LOW, and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data stream inputs (RIN). When the CD input is at a TTL LOW ( $\leq 0.8V$ ), the internal transitions detection circuitry is disabled.

### LFI – TTL Output

Link Fault Indicator. This input indicates the status of the input data stream (RIN±). It is controlled by three functions; the Carrier Detect (CD) input, the internal Transition Detector, and the Out of Lock (OOL) detector. The Transition Detector determines if RIN± contains enough transitions to be accurately recovered by the Receive PLL. The Out of Lock detector determines if RIN± is within the frequency range of the Receive PLL. When CD is HIGH and RIN± has sufficient transitions and is within the frequency range of the Receive PLL, the LFI input will be high. If CD is at an ECL LOW or RIN± does not contain sufficient transitions or RIN± is outside the frequency range of the Receive PLL then the LFI output will be LOW. If CD is at a TTL LOW then the LFI output will only transition LOW when the frequency of RIN± is outside the range of the Receive PLL.

### TSER± – Differential PECL Input

Transmit Serial Data. These built-in line receiver inputs are connected to the differential Transmit serial input data stream. These inputs can receiver very low amplitude signals and are compatible with all PECL signaling levels.

### TOUT± – Differential PECL Output

Transmit Output. These Positive ECL 100K outputs (+5V referenced) represent the buffered version of the Transmit data stream (TSER±). This Transmit path is used to take weak input signals and rebuffer them to drive low impedance copper media.

### REFCLK± – Differential PECL/TTL Input

Reference Clock. This input is the clock frequency reference for the clock and data recovery Receive PLL. REFCLK is multiplied internally by eight and sets the approximate center frequency for the internal Receive PLL to track the incoming bit stream. This input is also multiplied by eight by the frequency multiplier Transmit PLL to produce the bit rate Transmit Clock (TCLK±). REFCLK can be connected to either a differential PECL or single-ended TTL frequency source. When either REFCLK+ or REFCLK- is at a TTL LOW, the opposite REFCLK signal becomes a TTL level input.

### TCLK± – Differential PECL Output

Transmit Clock. These Positive ECL 100K outputs (+5V referenced) provide the bit rate frequency source for external Transmit data processing devices. This output is synthesized by the Transmit PLL and is derived by multiplying the REFCLK frequency by eight.

**PIN DESCRIPTIONS (CONT'D)**

**LOOP – TTL Input**

Loop Back Select. This input is used to select the input data stream source that the Receive PLL used for clock and data recovery. When the LOOP input is HIGH, the Receive input data stream (RIN±) is used for clock and data recovery. When LOOP is LOW, the Transmit input data stream (TSER±) is used by the Receive PLL for clock and data recovery.

**MODE – TTL Input**

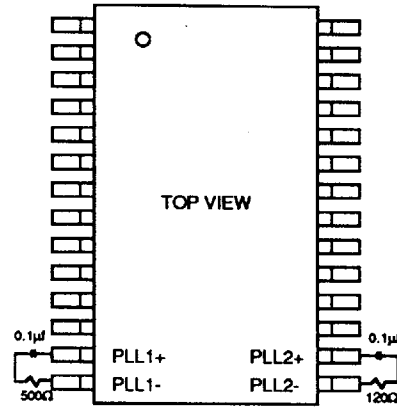
Frequency Mode Select. This input selects the frequency range for the clock and data recovery Receive PLL and the frequency multiplier Transmit PLL. When this input is held HIGH the two PLLs operate at the SONET (SDH) STS-3 (STM-1) line rate of 155.52MHz. When this input is held LOW the two PLLs operate at the SONET STS-1 line rate of 51.84MHz. The REFCLK± frequency in both operating modes is 1/8 the PLL operating frequency.

Vcc - Power (+5V)

VEE - Ground (0V)

**PLL1±, PLL2± – Loop Filter Inputs**

These pins are used to connect the external loop filters for the two on-board PLLs. See below:



**Figure 1. Suggested Loop Filter Values**

**DESCRIPTION**

**General**

The SY69952 Serial SONET/SDH Transceiver is used in SONET/SDH and ATM applications to recover clock and data information from a 155.52MHz or 51.84MHz NRZ (Non Return to Zero) or NRZI (Non Return to Zero Invert on ones) serial data stream. This device also provides a bit-rate Transmit clock, from a byte rate source through the use of a frequency multiplier PLL, and differential data buffering for the Transmit side of the system (see Figure 1). This device is compliant with all relevant SONET/SDH specifications including ANSI T1X1.6/91-022, ANSI T1X1.3/93-006R1 Draft and ITU/CCITT G958.

**Operating Frequency**

The SY69952 operates at either of two frequency ranges. The MODE input selects which of the two frequency ranges the Transmit frequency multiplier PLL and the Receive clock and data recovery PLL will operate. When MODE is connected to Vcc, the highest operating range of the device is selected. A 19.44MHz ± 1% source must drive the REFCLK input and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 155.52MHz ± 1%. When the MODE input is connected to ground (GND), the lowest operating range of the device is selected. A 6.48MHz ± 1% source must drive the REFCLK inputs and the two PLLs will multiply this rate by 8 to provide output clocks that operate at 51.84MHz ± 1%.

**Transmit Functions**

The transmit section of the SY69952 contains a PLL that takes a REFCLK input and multiplies it by 8 (REFCLKx8) to produce a PECL (Positive ECL) differential output clock (TCLK±). The transmitter has two operating ranges that are selectable with the three-level MODE pin as explained above. The SY69952 Transmit frequency multiplier PLL allows low-cost byte rate clock sources to be used to time the upstream serial data transmitter.

The REFCLK± input can be configured three ways. When both REFCLK+ and REFCLK- are connected to a differential 100K-compatible PECL source, the REFCLK input will behave as a differential PECL input. When either the REFCLK+ or the REFCLK- input is at a TTL LOW, the other REFCLK input becomes a TTL-level input allowing it to be connected to a low-cost TTL crystal oscillator. The REFCLK input structure, therefore, can be used as a differential PECL input, a single TTL input, or as a dual TTL clock multiplexing input.

The Transmit PECL differential input pair (TSER±) is buffered by the SY69952 yielding the differential data outputs (TOUT±). These outputs can be used to directly drive transmission media such as Printed Circuit Board (PCB) traces, optical drivers, twisted pair, or coaxial cable.

## DESCRIPTION (CONT'D)

### Receive Functions

The primary function of the receiver is to recover clock (RCLK $\pm$ ) and data (RSER $\pm$ ) from the incoming differential PECL data stream (RIN $\pm$ ) without the need for external buffering. These built-in line receiver inputs, as well as the TSER $\pm$  inputs mentioned above, have a wide common-mode range (2.5V) and the ability to receive signals with as little as 50mV differential voltage. They are compatible with all PECL signals and any copper media.

The clock recovery function is performed using an embedded PLL. The recovered clock is not only passed to the RCLK $\pm$  outputs, but also used internally to sample the input serial stream in order to recover the data pattern. The Receive PLL uses the REFCLK input as a byte-rate reference. This input is multiplied by 8 (REFCLKx8) and is used to improve PLL lock time and to provide a center frequency for operation in the absence of input data stream transitions. The receiver can recover clock and data in two different frequency ranges depending on the state of the MODE pin as explained earlier. To insure accurate data and clock recovery, REFCLKx8 must be within 1000 ppm of the transmit bit rate. The standards, however, specify that the REFCLKx8 frequency accuracy be within 20-100 ppm.

The differential input serial data (RIN $\pm$ ) is not only used by the PLL to recover the clock and data, but it is also buffered and presented as the PECL differential output pair ROUT $\pm$ . This output pair can be used as part of the transmission line interface circuit for base line wander compensation, improving system performance by providing reduced input jitter and increased data eye opening.

### Carrier Detect and Link Fault Indicator Functions

The Link Fault Indicator (LFI) output is a TTL-level output that indicates the status of the receiver. This output can be used by an external controller for Loss of Signal (LOS), Loss of Frame (LOF), or Out of Frame (OOF) indications. LFI is controlled by the Carrier Detect input, the internal Transitions Detector, and the PLL Out of Lock (OOL) circuitry.

The CD input may be driven by external circuitry that is monitoring the incoming data stream. Optical modules have CD outputs that indicate the presence of light on the optical fiber and some copper based systems use external threshold detection circuitry to monitor the incoming data stream. The CD input is a 100K PECL compatible signal that should be held HIGH when the incoming data stream is valid. When CD is pulled to a PECL LOW ( $\leq 2.5V$  max.), the LFI output will transition LOW and the Receiver PLL will align itself with the REFCLKx8 frequency and the recovered data outputs (RSER) will remain LOW regardless of the signal level on the Receive data-stream inputs (RIN).

In addition, the SY69952 has a built-in transitions detector that also checks the quality of the incoming data stream.

The absence of data transition can be caused by a broken transmission media, a broken transmitter, or a problem with the transmit or receive media coupling. The SY69952 will detect a quiet link by counting the number of bit times that have passed without a data transition. A bit time is defined as the period of RCLK $\pm$ . When 512 bit times have passed without a data transition on RIN $\pm$ , LFI will transition LOW. The receiver will assume that the serial data stream is invalid and, instead of allowing the RCLK $\pm$  frequency to wander in the absence of data, the PLL will lock to the REFCLKx8 frequency. This will insure that RCLK $\pm$  is as close to the correct link operating frequency as the REFCLK accuracy. LFI will be driven HIGH again and the receiver will recover clock and data from the incoming data stream when the transition detection circuitry determines that adequate transitions to ensure reliable clock and data recovery have been detected within 512 bit-times.

The Transition Detector can be turned off by pulling the CD input to a TTL LOW ( $\leq 0.8V$ ). When CD is pulled to a TTL LOW the LFI will only be driven LOW if the incoming data stream frequency is not within 1000 ppm of the REFCLKx8 frequency. LFI LOW in this will only indicate that the Receiver PLL is Out of Lock (OOL). When this pin is left unconnected, an internal pull-down resistor will pull this input to Ground.

### Loop Back Testing

The TTL level LOOP pin is used to perform loop-back testing. When LOOP is asserted (held LOW) the Transmitter serial input (TSER $\pm$ ) is used by the Receiver PLL for clock and data recovery. This allows in-system testing to be performed on the entire device except for the differential Transmit drivers (TOUT $\pm$ ) and the differential Receiver inputs (RIN $\pm$ ). For example, an ATM controller can present ATM cells to the input of the ATM cell processor and check to see that these same cells are received. When the LOOP input is deasserted (held HIGH) the Receive PLL is once again connected to the Receiver serial inputs (RIN $\pm$ ).

The LOOP feature can also be used in applications where clock and data recovery are to be performed from either of two data streams. In these systems the LOOP pin is used to select whether the TSER $\pm$  or the RIN $\pm$  inputs are used by the Receive PLL for clock and data recovery.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Symbol	Parameter	Rating	Unit
V <sub>CC</sub>	Power Supply (V <sub>EE</sub> = GND = 0V)	0 to +7	VDC
V <sub>I</sub>	Input Voltage (V <sub>EE</sub> = GND = 0V)	0 to V <sub>CC</sub>	VDC
I <sub>OUT</sub>	Output Current	Continuous	50
		Surge	100
T <sub>A</sub>	Operating Temperature Range	0 to +75	°C
T <sub>STG</sub>	Storage Temperature Range	-65 to +150	°C

**NOTE:**

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATING conditions for extended periods may affect device reliability.

**DC ELECTRICAL CHARACTERISTICS — PECL**

V<sub>CC</sub> = +5V ±10%; V<sub>EE</sub> = GND = 0V, T<sub>A</sub> = 0°C to +75°C

Symbol	Parameter	T <sub>A</sub> = 0°C		T <sub>A</sub> = +25°C		T <sub>A</sub> = +75°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
V <sub>OH</sub>	Output HIGH Voltage	3.975	4.120	3.975	4.120	3.975	4.120	V
V <sub>OL</sub>	Output LOW Voltage	3.190	3.380	3.190	3.380	3.190	3.380	V
V <sub>IH</sub>	Input HIGH Voltage	3.835	4.120	3.835	4.120	3.835	4.120	V
V <sub>IL</sub>	Input LOW Voltage	3.190	3.525	3.190	3.525	3.190	3.525	V
I <sub>IH</sub>	Input HIGH Current	—	225	—	175	—	175	μA
I <sub>IL</sub>	Input LOW Current	0.5	—	0.5	—	0.5	—	μA

**DC ELECTRICAL CHARACTERISTICS — TTL**

V<sub>CC</sub> = +5V ±10%; V<sub>EE</sub> = GND = 0V, T<sub>A</sub> = 0°C to +75°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V <sub>OH</sub>	Output HIGH Voltage	2.4	—	—	V	I <sub>OH</sub> = -2mA
V <sub>OL</sub>	Output LOW Voltage	—	—	0.5	V	I <sub>OL</sub> = 8mA
I <sub>OS</sub>	Output Short Circuit Current	-150	—	-60	mA	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>IH</sub>	Input HIGH Voltage	2.0	—	—	V	
V <sub>IL</sub>	Input LOW Voltage	—	—	0.8	V	

**DC ELECTRICAL CHARACTERISTICS**

V<sub>CC</sub> = +5V ±10%; V<sub>EE</sub> = GND = 0V, T<sub>A</sub> = 0°C to +75°C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
I <sub>EE</sub>	Internal Operating Current	—	140	—	mA	
I <sub>OUT</sub>	Termination Output Current	—	13	—	mA	50Ω to V <sub>CC</sub> -2, 50% duty cycle

**NOTES:**

1. To calculate total power supply current into the V<sub>CC</sub> pins: I<sub>CC</sub> = (n \* I<sub>OUT</sub>); where n = number of ECL output pins used (ie, terminated).
2. To calculate total device power dissipation; P<sub>D</sub> = [I<sub>EE</sub> \* (V<sub>CC</sub> - V<sub>EE</sub>)] + [n \* I<sub>OUT</sub> \* 1.33]<sup>(2)</sup>.
3. Average ECL output voltage is calculated as V<sub>OAVG</sub> = (V<sub>OH(MAX)</sub> + V<sub>OH(MIN)</sub> + V<sub>OL(MAX)</sub> + V<sub>OL(MIN)</sub>) / 4 = 1.33V.

## AC ELECTRICAL CHARACTERISTICS

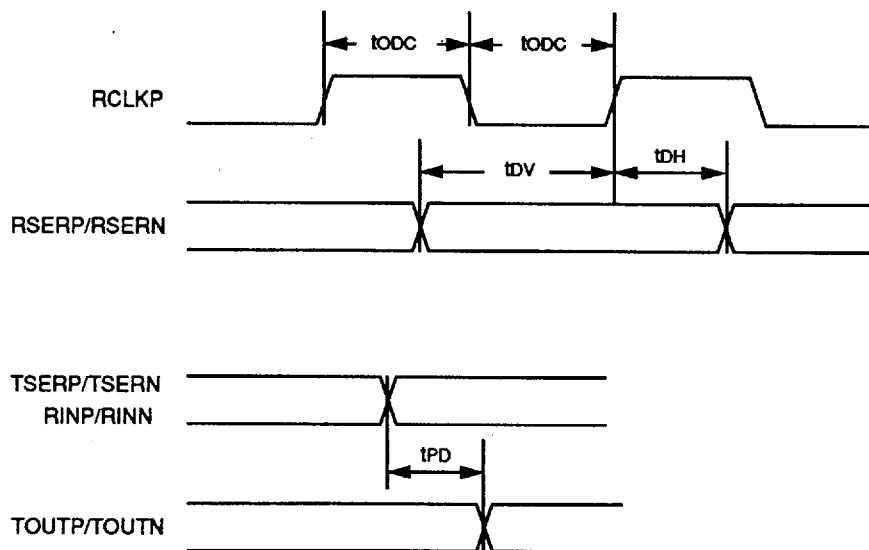
VCC = +5V ±10%; VEE = GND = 0V, TA = 0°C to +75°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Condition
fREF	Reference Frequency	6.41 19.24	6.48 19.44	6.55 19.64	MHz MHz	MODE = 0 MODE = 1
fb	Bit Time <sup>(1)</sup>	19.5 6.50	19.3 6.43	19.1 6.40	ns ns	MODE = 0 MODE = 1
tPE	Receiver Static Phase Error <sup>(2)</sup>	— —	— —	100 200	ps ps	MODE = 0 MODE = 1
tODC	Output Duty Cycle <sup>(2)</sup> (TCLK±, RCLK±)	48	—	52	%	
tRF	ECL Output Rise/Fall Time <sup>(2)</sup>	0.4	—	1.2	ns	5pf load, 50Ω to Vcc -2
tLOCK	PLL Lock Time	—	—	0.5	ms	RIN transition density 25%
tRPWH	REFCLK Pulse Width High	3.3 10	— —	— —	ns ns	MODE = 0 MODE = 1
tRPWL	REFCLK Pulse Width Low	3.3 10	— —	— —	ns ns	MODE = 0 MODE = 1
tDV	Data Valid	3	—	—	ns	Prior to RCLK+ rising edge
tDH	Data Hold	1	—	—	ns	After RCLK+ falling edge
tPD	Propagation Delay <sup>(3)</sup> (RIN to ROUT, TSER to TOUT)	—	—	10	ns	
Jgen	Jitter Generation of RX PLL	—	—	0.01	UI	RMS
f-3dB	-3dB Gain Bandwidth of RX PLL (Jitter Xfer BW)	—	—	130	KHZ	
Gpeak	Maximum Peaking of RX PLL	—	—	0.1	dB	

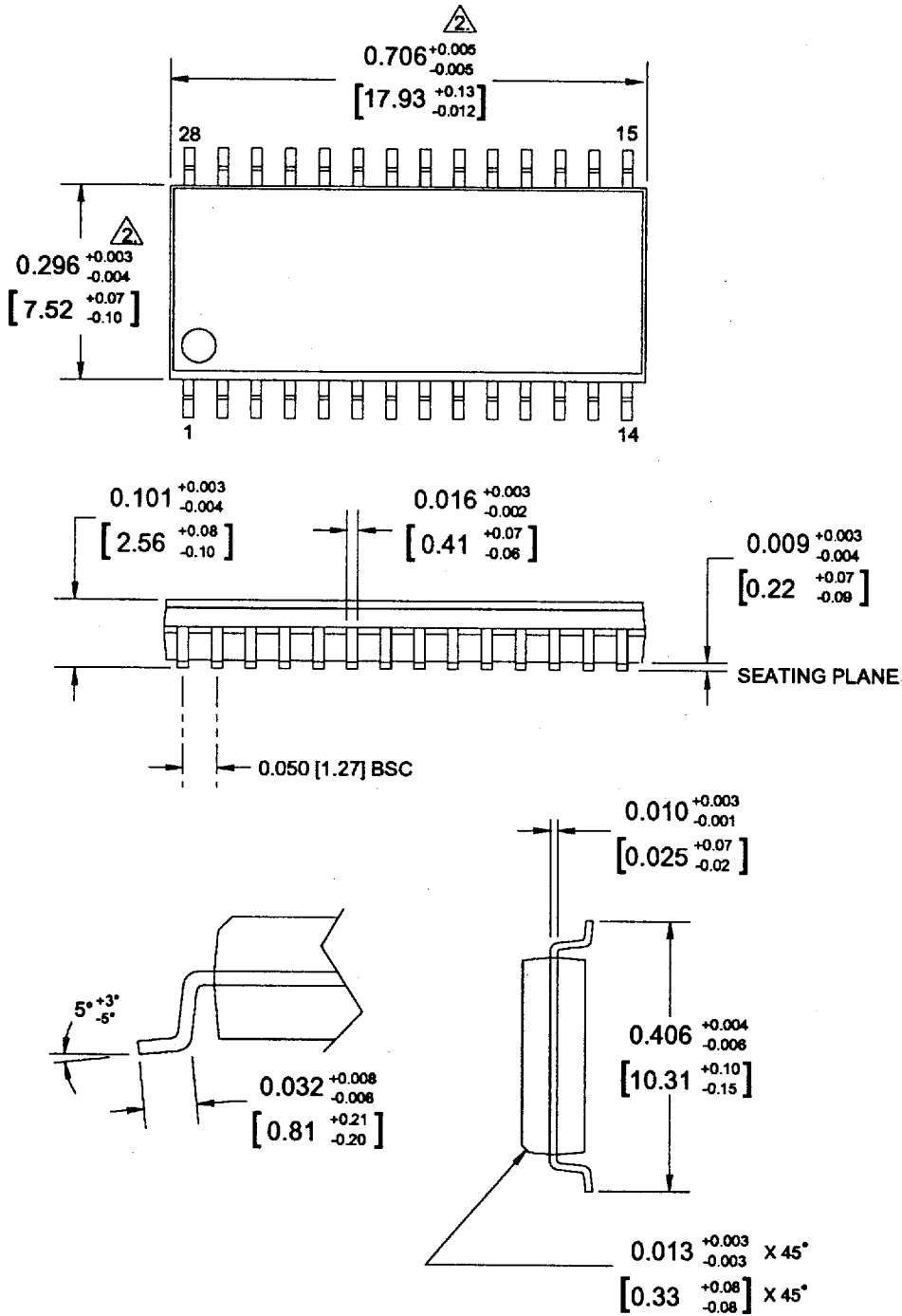
NOTES:

- fb is calculated as 1/(fREF \* 8).
- Tested initially and after any design or process changes that may affect these parameters.
- The ECL switching threshold is the differential zero crossing (ie, the point where + and - signals cross).

## TIMING WAVEFORMS



**28 LEAD PLASTIC SOIC (Z28-1)**



NOTES:

1. DIMENSIONS ARE IN INCHES AND [MILLIMETERS].

2. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH WHICH MAY BE AS MUCH AS 0.010 [0.25] PER SIDE.