64K (8K X 8) ROM

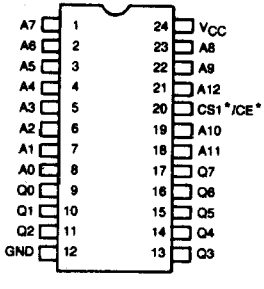
2364/65

- 2364/65 ..... Non-Power Down
- 2364S/65S ..... Automatic Power Down
- Fully Static Operation
- Silicon Gate NMOS Technology
- Maximum Access Time
  - 2364/65-20 ..... 200ns
  - 2364/65-25 ..... 250ns
  - 2364/65-30 ..... 300ns
- Programmable Chip Selects
- 3-State Outputs
- Fully TTL Compatible
- Single ± 10% 5 Volt Supply
- Pin Compatible with 2564 EPROM's
- Available in 3 Temperature Ranges
  - 2364/65 (Commercial) ..... 0°C to 70°C
  - 2364I/65I (Industrial) ..... −40°C to 85°C
  - 2364HR/65HR (Military) ..... −55°C to 125°C

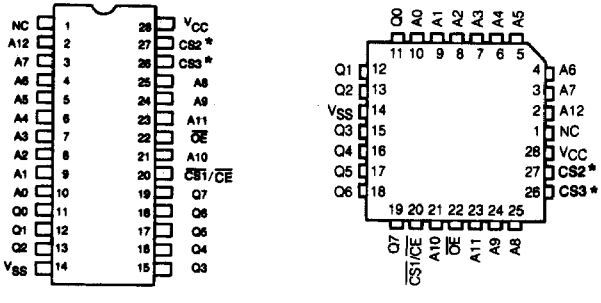
The NCR 2364 and 2365 are mask programmable read-only-memories with 8K word by 8 bit organizations. Designed for ease of use, these devices require only a 5-volt supply, are TTL compatible, and because of their totally static (asynchronous) operation require no clock. These memory devices are available in two versions. The 2364 and 2365 are non-power down versions where the active level of chip selects CS1 (on the 2364), and CS2 and CS3 (on the 2365) are programmable and defined by the user to facilitate system memory expansion. The 2364S and 2365S are standby versions offering an automatic power-down feature controlled by the chip enable CE input. When CE goes high, the device automatically powers down and remains in a low power standby mode as long as CE remains high. Also to provide easier system implementation, the active level of chip enable CE (on the 2364S), and chip selects CS2 and CS3 (on the 2365S) is programmable. The NCR 2364 is packaged in a 24 pin DIP, and the 2365 is packaged in a 28 pin DIP, both with industry standard byte-wide JEDEC pin-outs. Optionally, the 2365 is available in a space saving 28 pin surface mounted plastic leaded chip carrier.

PIN CONFIGURATION

NCR 2364/S



NCR 2365/S



* Active Level (Hi, Low or Don't Care) defined by user.

PIN NAMES

A0 - A12	Address Inputs
Q0 - Q7	Data Outputs
CS1, $\overline{CS1}$ CS2, CS3	Programmable Chip Select
CE, $\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	5V ± 10% Supply Voltage

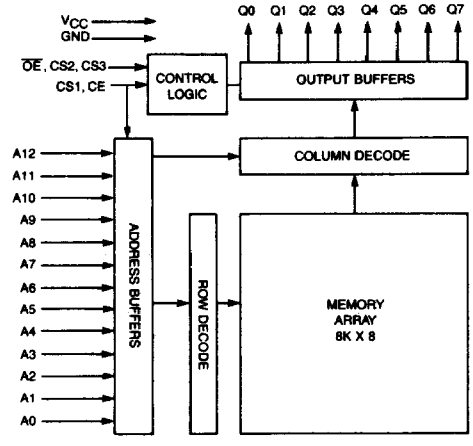
MEMORY PRODUCTS

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin with respect to ground ..... −0.5 to +7V
Storage temperature ..... −65 °C to 150 °C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operating conditions stipulated elsewhere in this specification is not implied.

FUNCTIONAL BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	2364/65			2364I/65I			2364HR/65HR			Units
		Min.	Typ.	Max.	Min.	Typ.	Max	Min.	Typ.	Max	
V_{CC}	Supply voltage*	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	Volts
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.2		V_{CC}	Volts
V_{IL}	Input low level voltage	−0.5		0.8	−0.5		0.8	−0.5		0.8	Volts
T_A	Operating ambient temperature	0		70	−40		85	−55		125	°C

* V_{CC} must be applied at least 100μs before proper device operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS[1] (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{IN}	Input leakage current	V_{IN} = 0V to V_{CC} max			10	μA
I_O	Output leakage current	V_O = 0.2 to V_{CC} max, Chip Deselected			±10	μA
V_{OH}	Output high voltage	I_{OH} = −200μA	2.4			Volts
V_{OL}	Output low voltage	I_{OL} = 3.2mA			0.4	Volts
I_{CC}	Supply current - active	Outputs Open			60	mA
I_{SB}*	Supply current - standby	Chip Deselected			10	mA

* Applies to 2364S/65S power down versions only

CAPACITANCE,[1] T_A = 25 °C, f = 1 MHz

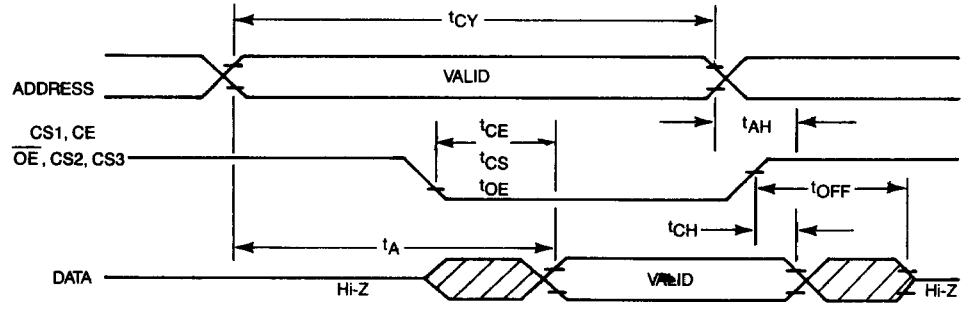
Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
C_{IN}	Input capacitance	All pins except pin under			7	pF
C_O	Output capacitance	test are tied to ground			12.5	pF

Note: 1. Characteristics are the same for all operating temperature ranges.

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

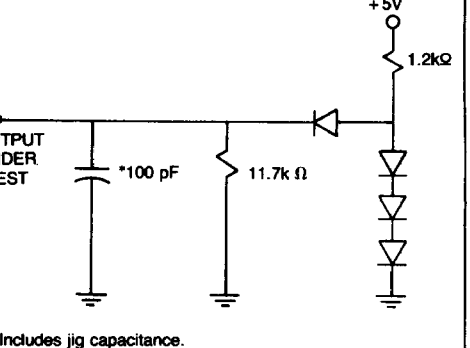
Symbol	Parameter	2364/65-20, 2364I/65I-20, 2364HR/65HR-20			2364/65-25, 2364I/65I-25, 2364HR/65HR-25			2364/65-30, 2364I/65I-30, 2364HR/65HR-30			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{CY}	Cycle time	200			250			300			ns
t_A	Address access time			200			250			300	ns
t_{CE}	Chip enable access time	200			250			300			ns
t_{CS}	Chip select access time			100			120			150	ns
t_{OFF}	Chip select to data off (Hi Z)			100			120			150	ns
t_{CH}	Data hold time from control	0			0			0			ns
t_{AH}	Data hold time from address	0			0			0			ns

AC WAVEFORMS



The chip select line is assumed to be active low.

AC TEST LOAD CIRCUIT



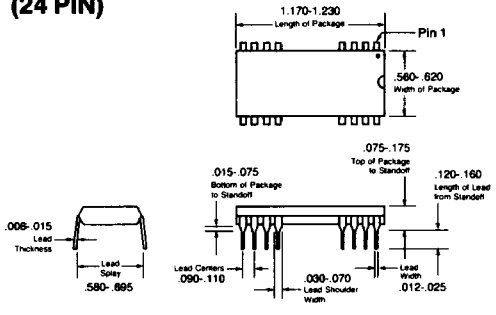
* Includes jig capacitance.
All diodes 1N3064 or equivalent.

A.C. CONDITION OF TESTS

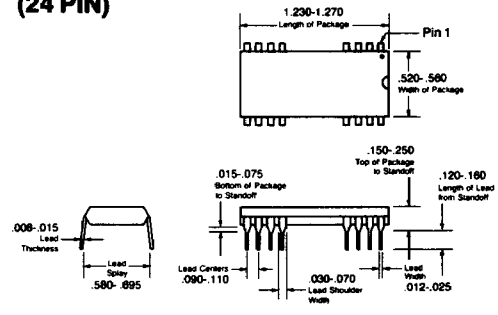
Input Pulse Levels ..... 0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times ..... 10 ns
Output Timing Levels ..... 0.8 Volts to 2.0 Volts

MECHANICAL DATA

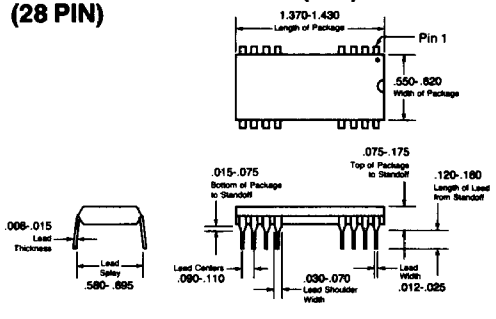
CERAMIC DUAL IN LINE (DIP) (24 PIN)



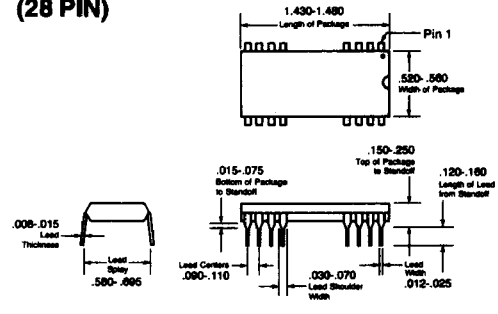
PLASTIC DUAL IN LINE (DIP) (24 PIN)



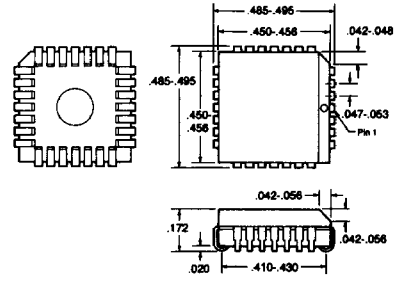
CERAMIC DUAL IN LINE (DIP) (28 PIN)



PLASTIC DUAL IN LINE (DIP) (28 PIN)



PLASTIC LEADED CHIP CARRIER (PLCC) (28 PIN)



All dimensions are in inches.