

SP9756

T-51-10-07

6-BIT HIGH SPEED, HIGH ACCURACY ADC

The Plessey SP9756 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit, reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 110MHz, with a wide analog bandwidth and good dynamic performance.

A choice of accuracy is available: the accuracy of the SP9756-8 is typically $\pm 1/8$ LSB at 2V input and therefore it is ideally suited for use in systems that incorporate expansion to higher resolutions. Alternatively the SP9756-6 is guaranteed to be accurate to $\pm 1/2$ LSB for inputs between 1V and 2V in cost conscious designs.

FEATURES

- $\pm 1/2$ or $\pm 1/8$ LSB Accuracy (-6 and -8 versions)
- Monotonic over the Full Frequency Range
- 110MHz Conversion Rate (130MHz Typ.)
- 250MHz Full Power Bandwidth (To -3dB) at 1V Input
- 50MHz Bandwidth with typically $\pm 1/2$ LSB Accuracy
- Operates on a Single -5.2V Supply
- Internally Latched 6-Bit ECL Outputs (7ns Minimum Valid Data at 100MHz)
- Operating Temperature Range: -40°C to +85°C Industrial
- On-Chip Band-Gap Reference for Good Temperature Stability
- Internal Clock Buffer
- No External Sample and Hold Needed
- On-Chip Reference Chain
- Sense Outputs for Precise Setting of Reference Voltages
- Mode Input to Program Over-Range Condition
- Low Propagation Delay (3ns Typ.)

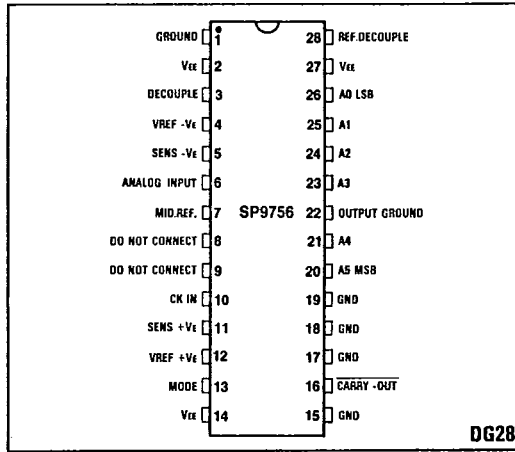


Fig.1 Pin connections - top view

APPLICATIONS

- Instrumentation
- Nucleonics Research
- Video Printers
- Radar Video Digitising
- Medical Electronics

ORDERING INFORMATION

SP9756-6 DG (Industrial - Ceramic DIL package)
SP9756-8 DG (Industrial - Ceramic DIL package)

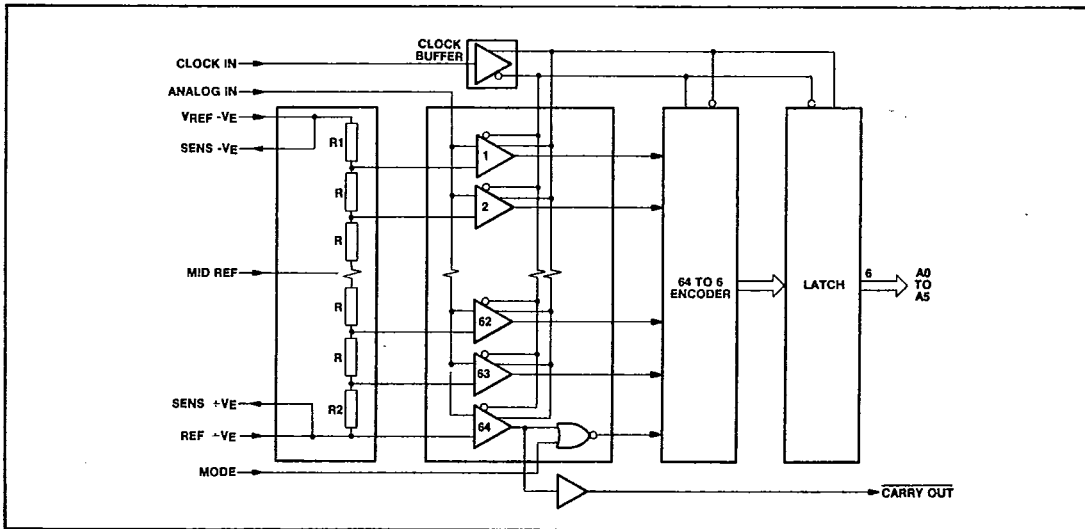


Fig.2 SP9756 functional block diagram

ELECTRICAL CHARACTERISTICS
Test conditions (unless otherwise stated):
T_{amb} = +25°C, V_{EE} = -5.2V ± 0.25V

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Characteristic	Pin	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply current, I _{EE}	2	-4.5	-170	-250	mA	Excludes ECL O/P & ref. currents
Supply voltage, V _{EE}				-5.5	V	
Dynamic range					2.20	
Analog input capacitance			22		pF	Degrades below -30°C (V _{EE} = -5.20V)
Analog input current				2.2	mA	
Minimum reference bit size			8		mV	
Power dissipation			1.2	1.7	W	Outputs loaded
Differential linearity SP9756-8 at 7kHz input			±0.125	±0.188	LSB	2V p-p input, 100MHz clock, measured using histogram test. See Figs.7 to 9 and reference 1 measurement techniques.
at 50MHz input			±0.5		LSB	
Integral linearity SP9756-8 at 7kHz input				±0.25	LSB	
at 50MHz input			±0.5		LSB	
Differential linearity SP9756-6 at 7kHz input				±0.5	LSB	1V p-p input, 100MHz clock, measured using histogram test. See Figs.10 and 11 and reference 1 measurement techniques.
at 50MHz input				±0.75	LSB	
Integral linearity SP9756-6 at 7kHz input				±0.5	LSB	
at 50MHz input				±0.5	LSB	
Aperture jitter			25		ps	
Full power 3dB bandwidth			250		MHz	
S/N ratio (RMS) at 50MHz analog, 101MHz sample rate		32			dB	
Data out A ₆ to A ₅	20-21, 2326					
O/P V _{HIGH}			-0.9		V	
O/P V _{LOW}			-1.8		V	
R _{Chan}	3,12		25		Ω	
V _{mode High}	13	-50		+100	mV	All zero's over-range
V _{mode LOW}	13	-3.5		-0.500	V	All one's over-range
Sample rate	10	110	130		MHz	No missing codes
T _{data}		7			ns	
T _{prop}			3		ns	
t _t				1.5	ns	
t _{sto}			1.2		ns	
t _{co}			2.0		ns	

ABSOLUTE MAXIMUM RATINGS

Clock & Mode input	0V to -3.5V
Supply voltage	-7V
Maximum junction temperature	175°C
Storage temperature range	-55°C to +150°C
Thermal characteristics:-	
θ _{JA}	40 deg C/W (typ)
θ _{JC}	15 deg C/W (typ)
T _{amb}	-40°C to +70°C (still air)
T _{amb}	-55°C to +125°C

(in 500LFPM of air across package)

OPERATING NOTES

Analog Input

The input voltage range is 0.0V to -2.2V. Optimum performance is achieved with an input of 2V p-p i.e. DC offset to -1.0V for symmetrical limiting. At temperatures below -30°C this input range may degrade to 1.8V p-p.

The input capacitance is of the order of 22pF therefore the source impedance should be low. The device is specified using an input drive from a 50Ω generator into a 50Ω termination resistor, i.e. 25Ω looking out of the device. This 25Ω source impedance should be considered as a maximum.

Reference Voltage

For optimum performance REF +VE (pin 12) should be connected to 0V (analog GND) and REF -VE (pin 4) to -2V supply. This supply should be decoupled with a good quality, high frequency capacitor to the analog GND. The minimum voltage across the reference is 0.5V, below this the linearity of the device will be adversely affected.

An input signal above $V_{REF} +VE$ will give an 'all ones' output provided that pin 13 is connected to a -2V supply (see mode input).

Sense pins (SENS +VE, pin 11 and SENS -VE, pin 5) are available on both REF +VE and REF -VE. These allow Kelvin applied voltages to be used for precision setting of the reference chain.

The reference chain can be used dynamically for applications using ACG on non-linear coding (see Fig.6).

Clock Input

As the SP9756 features an internal differential clock driver, a single ended ECL clock signal is suitable.

The aperture uncertainty of the device is in the order of 25ps, therefore the clock signal should have low edge jitter to be compatible.

Clock Timing

The first sample of the analog input is taken approximately 1.2ns after the rising edge of the clock. The input comparators then latch, holding their state until the falling edge.

When the SP9756 receives the first falling edge the device commences decoding and the input comparators are released. The binary data becomes available at the outputs 3.5ns after the second rising edge of the clock.

The SP9756 incorporates an output D-type latch. The data out from this latch is valid for over 70% of the clock cycle, at 100MHz. This greatly simplifies data acquisition of the binary information, as timing is not so critical as with many other ADCs.

Mode Input

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The MODE input (pin 13) selects the output code when V_{IN} is higher than REF +VE. For normal operation this pin should be connected to -2V. The SP9756 will then give an all ones output for any input greater than REF +VE. If the mode input is tied to GND the device will give all zeros when the input is higher than REF +VE.

The mode pin must not be left open circuit.

CIRCUIT BOARD LAYOUT

As with most PCB layouts for analog-to-digital conversion, the best performance from the SP9756 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 100Ω load to a -2V supply.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP9756 close to the device supply pins with good quality high frequency capacitors. It is also advisable to direct the current returned from the output load towards pin 22 and away from other digital grounds. One way of achieving this is by creating a second digital ground plane which should connect to the main digital ground at pin 22 of the device, the ground connection between the ADC and the device acquiring the data is then made to this second digital ground plane.

The following should be referred to the digital GND: V_{EE} , REF decouple (pin 28), -2V supply for output termination, clock termination, device GND, pins 1, 15 and 22.

The following should be referred to the analog GND: Ref +VE, REF -VE, input termination or buffer.

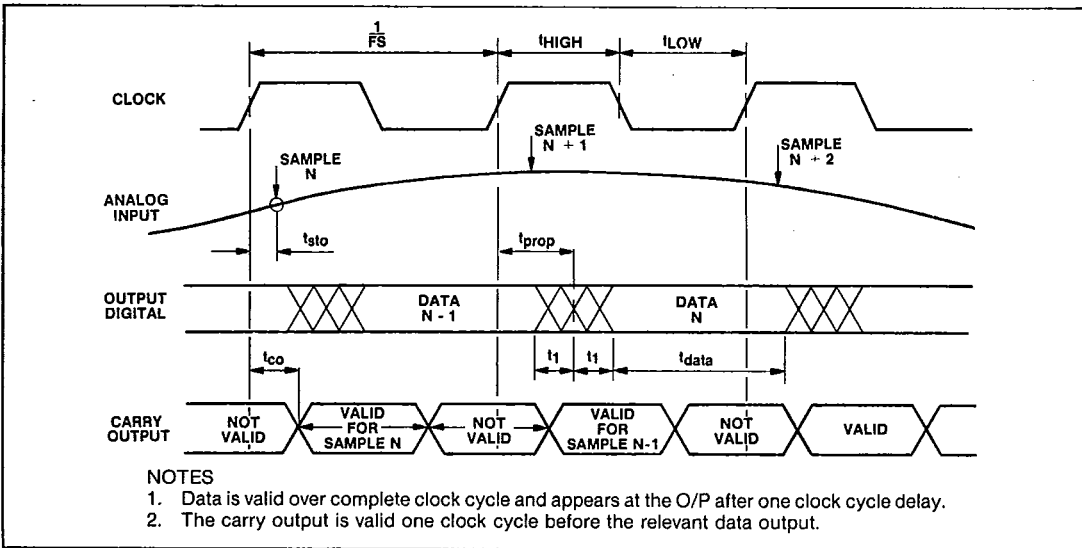


Fig.3 Timing diagram

SUBBRANGING

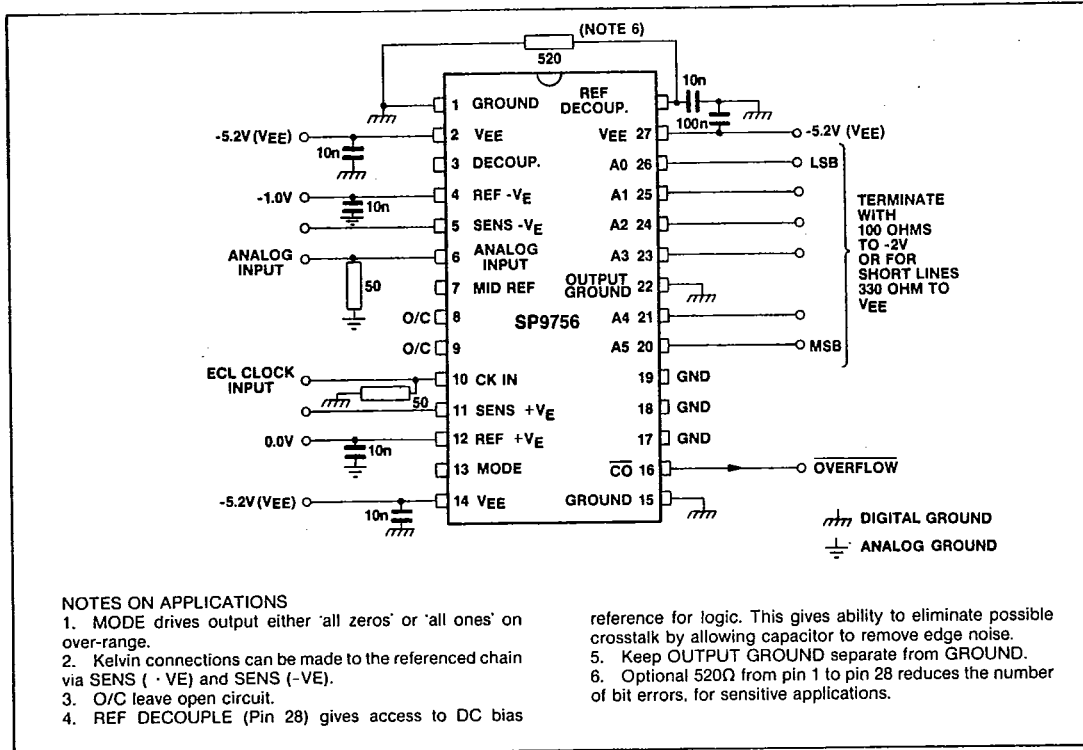
The subbranging system uses a two rank method for coarse then fine digitisation of the input signal. The SP9756-8 is ideally suited for subbranging systems as the accuracy of the first rank conversion defines the total system accuracy. Systems with 8 bits $\pm \frac{1}{2}$ LSB accuracy can be realised (see Fig.5).

NON LINEAR CODING (REF.3)

By simply feeding the reference with a proportion of the analog input (as shown in Fig.6) non-linear coding can be produced. The accuracy of the Plessey SP9756-8 allows expansion factors of 4:1 whilst maintaining $\frac{1}{2}$ LSB accuracy. This gives a dynamic range of 49.8 dB from a single six-bit device.

REFERENCES

1. *Dynamic Performance of A to D Converters*, Hewlett Packard Product Note 5180A-2
2. *A Complete 100MHz A/D - D/A Evaluation System*, Plessey P.S.2048.
3. *Cern-EP/79-133*, B. Hallgren & H. Verweij.



NOTES ON APPLICATIONS

1. MODE drives output either 'all zeros' or 'all ones' on over-range.
2. Kelvin connections can be made to the referenced chain via SENS (+VE) and SENS (-VE).
3. O/C leave open circuit.
4. REF DECOUPLE (Pin 28) gives access to DC bias

- reference for logic. This gives ability to eliminate possible crosstalk by allowing capacitor to remove edge noise.
5. Keep OUTPUT GROUND separate from GROUND.
6. Optional 520Ω from pin 1 to pin 28 reduces the number of bit errors, for sensitive applications.

Fig.4 Test and applications circuit

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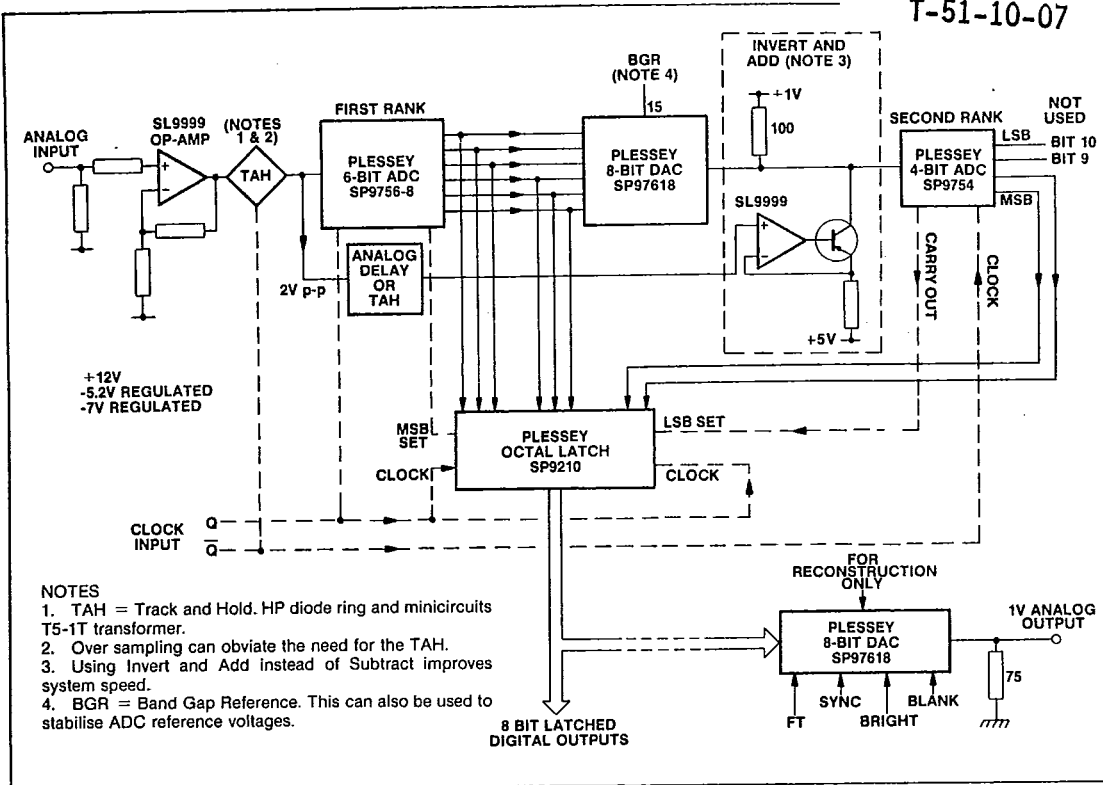


Fig.5 Block diagram of low cost high speed 8-bit A-D converter using SP9756-8

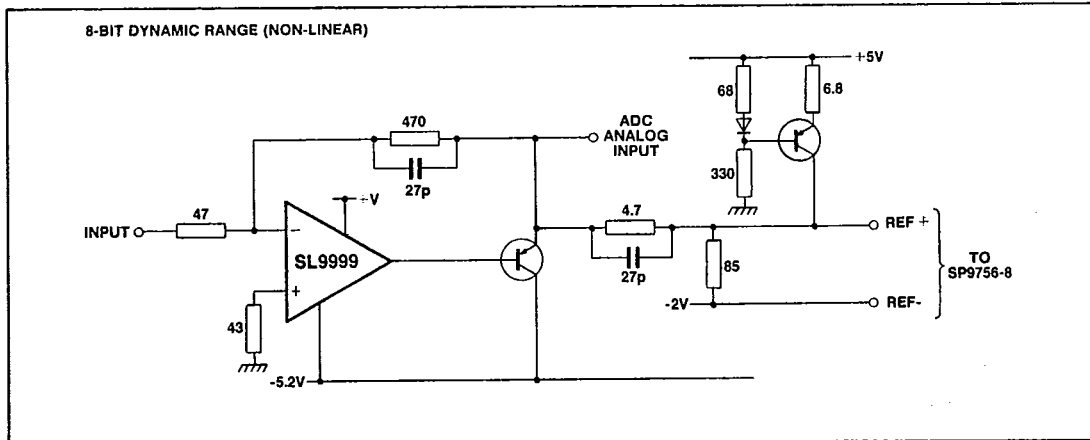


Fig.6 SP9756-8 with 4:1 expansion in dynamic range (non-linear)

TYPICAL ACCURACY DATA

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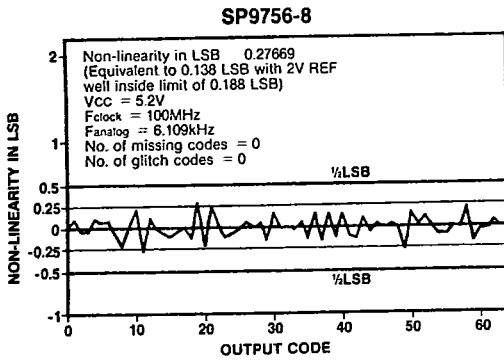


Fig.7 Device measured at 1V on REF with 6kHz analog and 100MHz clock

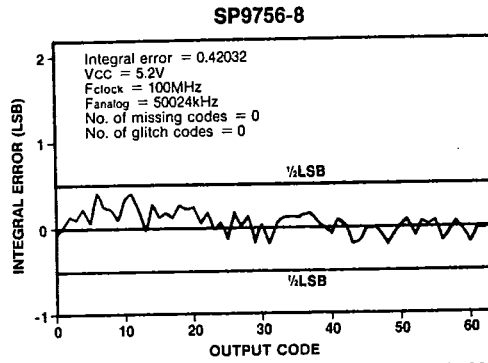


Fig.8 Measured with 2V REF at 50MHz analog and 100MHz clock proves ±0.5 LSB integral spec and ±0.5 LSB differential spec

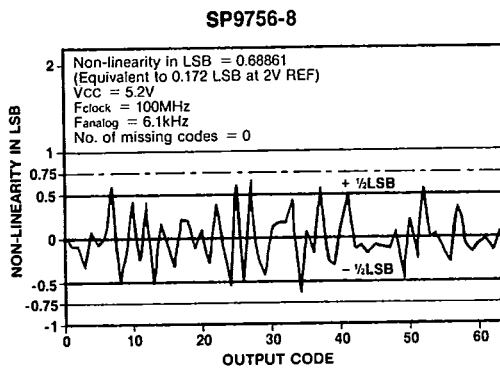


Fig.9 Measured at 0.5V REF
0.75 LSB limit at 0.5V REF ≡ 0.1875 LSB at 2V REF
0.5 LSB limit at 0.5V REF ≡ 0.125 LSB at 2V REF

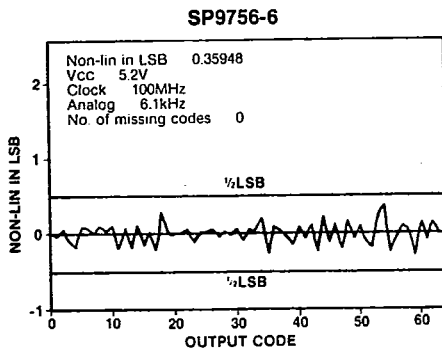


Fig.10 Differential linearity in LSB

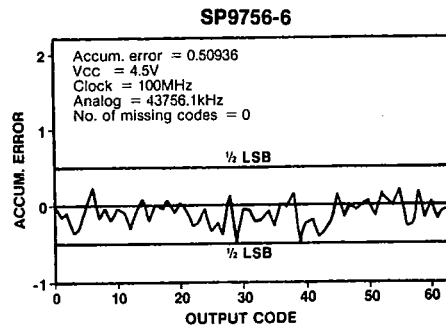


Fig.11 End point integral linearity (near Nyquist input frequency)