

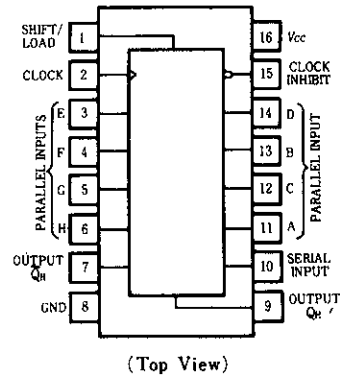
HD74LS165A

Parallel-Load 8-bit Shift Register

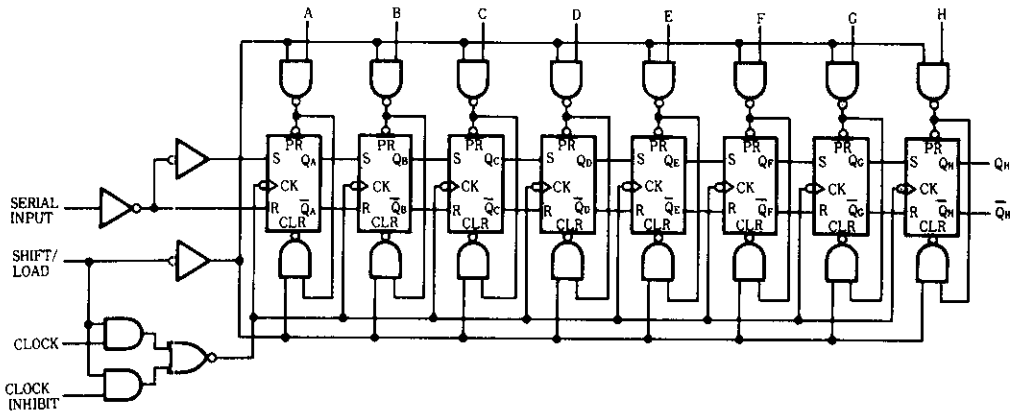
The LS165A are 8-bit serial shift registers that shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs that are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the shift/load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input independently of the levels of the clock, clock inhibit, or serial inputs.

PIN ARRANGEMENT



BLOCK DIAGRAM



FUNCTION TABLE

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . H	Q_A	Q_B	
L	X	X	X	a . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Cn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

- Notes) 1. H; high level, L; low level, X; irrelevant
2. ↑; transition from low to high level
3. a ~ h; the level of steady-state input at inputs A to H respectively
4. $Q_{A0} \sim Q_{H0}$; the level of Q_A to Q_H , respectively, before the indicated steady-state input conditions were established.
5. $Q_{An} \sim Q_{Gn}$; the level of Q_A to Q_G , respectively, before the most recent ↓ transition of the clock.

RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output current	I_{OH}	—	—	—400	μA
Low level output current	I_{OL}	—	—	8	mA
Clock frequency	f_{clock}	0	—	25	MHz
Clock pulse width	t_w (clock)	25	—	—	ns
Load pulse width	t_w (load)	15	—	—	ns
Clock-enable Setup time	t_{su}	30	—	—	ns
Parallel-input Setup time	t_{su}	10	—	—	ns
Serial input setup time	t_{su}	20	—	—	ns
Shift setup time	t_{su}	45	—	—	ns
Hold time at only input	t_h	0	—	—	ns

ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ C$)

Item		Symbol	Test Conditions	min	typ*	max	Unit
Input voltage		V_{IH}		2.0	—	—	V
		V_{IL}		—	—	0.8	V
Output voltage		V_{OH}	$V_{CC} = 4.75V$, $V_{IH} = 2V$, $V_{IL} = 0.8V$, $I_{OH} = -400\mu A$	2.7	—	—	V
		V_{OL}	$V_{CC} = 4.75V$, $V_{IH} = 2V$	—	—	0.4	V
			$V_{IL} = 0.8V$	—	—	0.5	V
Input current	Shift/Load	I_I	$V_{CC} = 5.25V$ $V_I = 7V$	—	—	0.3	mA
	Other inputs			—	—	0.1	mA
High level input current	Shift/Load	I_{IH}	$V_{CC} = 5.25V$ $V_I = 2.7V$	—	—	60	μA
	Other inputs			—	—	20	μA
Low level input current	Shift/Load	I_{IL}	$V_{CC} = 5.25V$ $V_I = 0.4V$	—	—	1.2	mA
	Other inputs			—	—	—0.4	mA
Short-circuit output current		I_{OS}	$V_{CC} = 5.25V$	—20	—	—100	mA
Supply current**		I_{CC}	$V_{CC} = 5.25V$	—	—	36	mA
Input clamp voltage		V_{IK}	$V_{CC} = 4.75V$, $I_{IN} = -18mA$	—	—	1.5	V

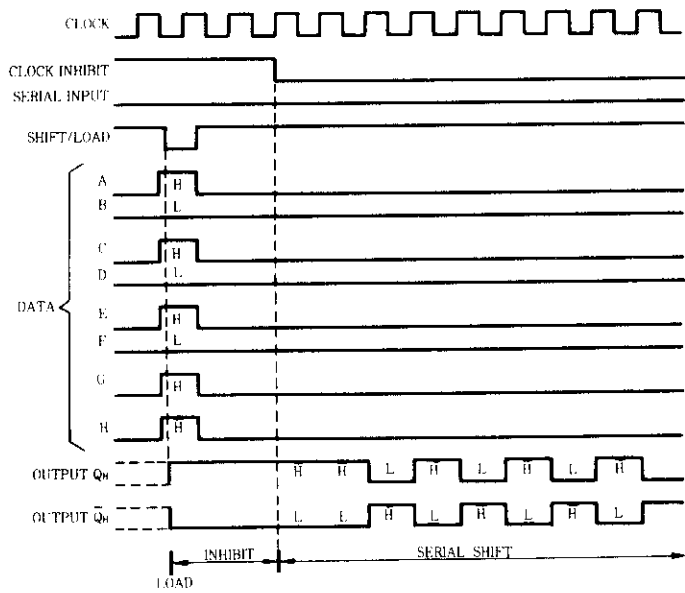
* $V_{CC} = 5V$, $T_a = 25^\circ C$

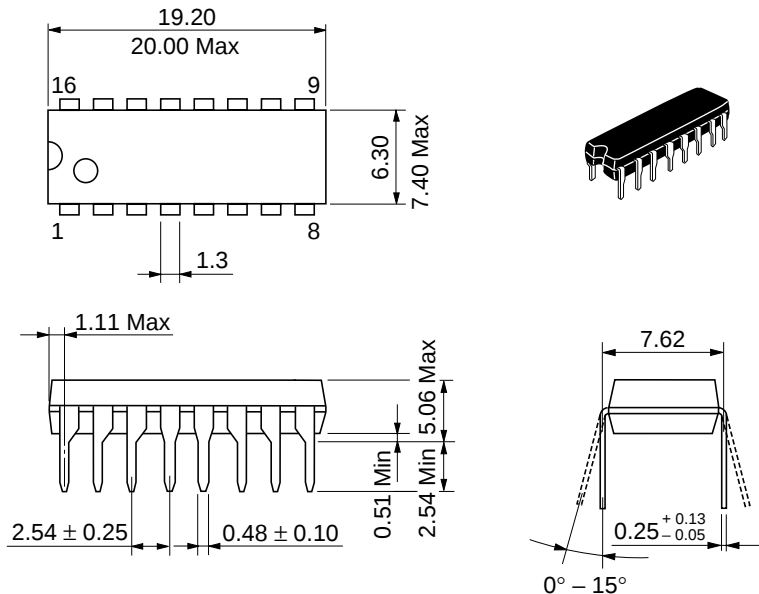
** With the outputs open, clock inhibit and clock at 4.5V, and a clock pulse applied to the shift/load, I_{CC} is measured with the parallel inputs at 4.5V, then with the parallel inputs grounded.

SWITCHING CHARACTERISTICS ($V_{CC} = 5V$, $T_a = 25^\circ C$)

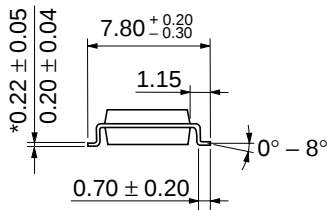
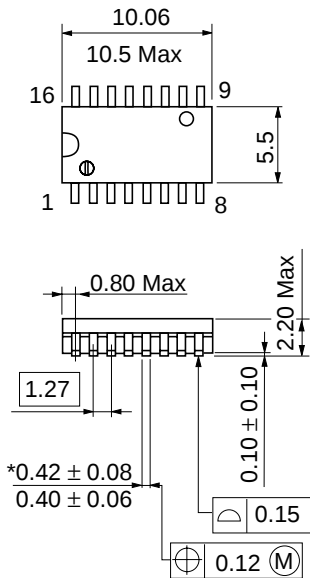
Item	Symbol	Input	Output	Test Conditions	min	typ	max	Unit
Maximum Clock frequency	f_{max}			$C_L = 15\text{pF}$ $R_L = 2\text{k}\Omega$	25	35	---	MHz
Propagation Delay time	t_{PHL}	Load	Any		—	21	35	ns
	t_{PLH}				—	26	35	ns
	t_{PHL}				Clock	Any	—	14
	t_{PLH}	—	16				25	ns
	t_{PHL}	H	Q_H				—	13
	t_{PLH}				—	24	30	ns
	t_{PHL}				H	Q_H	—	19
	t_{PLH}	—	17				25	ns
	t_{PHL}							

TYPICAL SHIFT, LOAD AND INHIBIT SEQUENCES



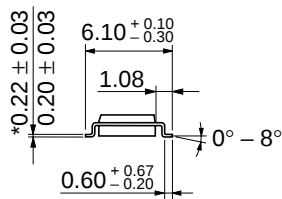
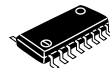
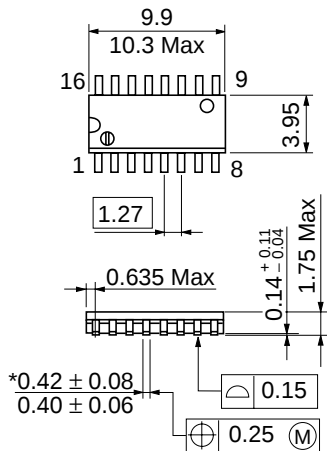


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.
2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.
3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.
4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.
5. This product is not designed to be radiation resistant.
6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.
7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL	NorthAmerica	: http://semiconductor.hitachi.com/
	Europe	: http://www.hitachi-eu.com/hel/ecg
	Asia (Singapore)	: http://www.has.hitachi.com.sg/grp3/sicd/index.htm
	Asia (Taiwan)	: http://www.hitachi.com.tw/E/Product/SICD_Frame.htm
	Asia (HongKong)	: http://www.hitachi.com.hk/eng/bo/grp3/index.htm
	Japan	: http://www.hitachi.co.jp/Sicd/indx.htm

For further information write to:

Hitachi Semiconductor (America) Inc. 179 East Tasman Drive, San Jose, CA 95134 Tel: <1> (408) 433-1990 Fax: <1> (408) 433-0223	Hitachi Europe GmbH Electronic components Group Dornacher Straße 3 D-85622 Feldkirchen, Munich Germany Tel: <49> (89) 9 9180-0 Fax: <49> (89) 9 29 30 00 Hitachi Europe Ltd. Electronic Components Group. Whitebrook Park Lower Cookham Road Maidenhead Berkshire SL6 8YA, United Kingdom Tel: <44> (1628) 585000 Fax: <44> (1628) 778322
--	---

Hitachi Asia Pte. Ltd. 16 Collyer Quay #20-00 Hitachi Tower Singapore 049318 Tel: 535-2100 Fax: 535-1533 Hitachi Asia Ltd. Taipei Branch Office 3F, Hung Kuo Building, No.167, Tun-Hwa North Road, Taipei (105) Tel: <886> (2) 2718-3666 Fax: <886> (2) 2718-8180
--

Hitachi Asia (Hong Kong) Ltd. Group III (Electronic Components) 7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Tsim Sha Tsui, Kowloon, Hong Kong Tel: <852> (2) 735 9218 Fax: <852> (2) 730 0281 Telex: 40815 HITEC HX
--

Copyright ' Hitachi, Ltd., 1999. All rights reserved. Printed in Japan.