BiCMOS Cold Cathode Fluorescent Lamp Driver Controller

FEATURES

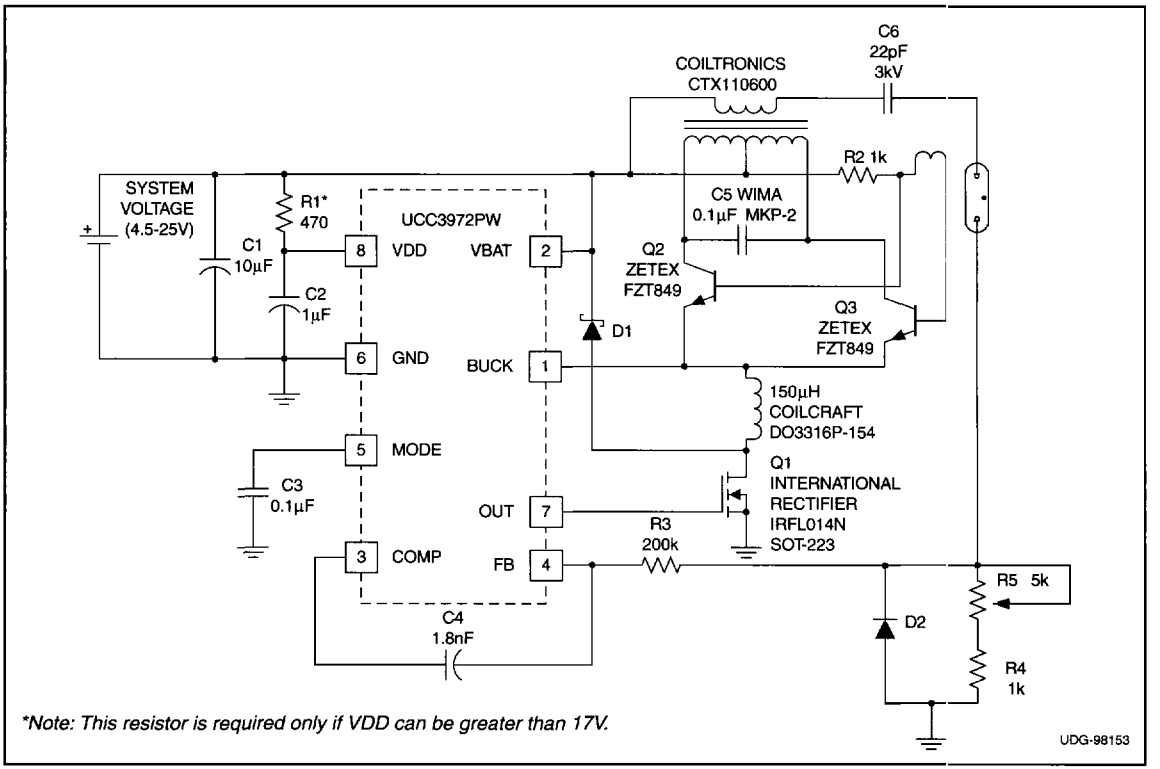
- 1mA Typical Supply Current
- Accurate Lamp Current Control
- Analog or Low Frequency Dimming Capability
- Open Lamp Protection
- 4.5 to 25V Operation
- PWM Frequency Synchronized to External Resonant Tank
- 8 Pin TSSOP and SOIC Packages Available

DESCRIPTION

Design goals for a Cold Cathode Fluorescent Lamp (CCFL) converter used in a notebook computer or portable application include small size, high efficiency, and low cost. The UCC3972 CCFL controller provides the necessary circuit blocks to implement a highly efficient CCFL backlight power supply in a small footprint 8 pin TSSOP package. The BiCMOS controller typically consumes less than 1mA of operating current, improving overall system efficiency when compared to bipolar controllers requiring 5 to 10mA of operating current.

External parts count is minimized and system cost is reduced by integrating such features as a feedback controlled PWM driver stage, open lamp protection, and synchronization circuitry between the buck and push-pull stages. The UCC3972 includes an internal shunt regulator, allowing the part to operate with input voltages from 4.5V up to 25V. The part supports both analog and low frequency dimming modes of operation.

TYPICAL APPLICATION CIRCUIT



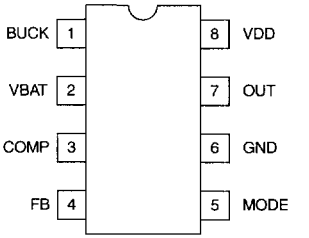
ABSOLUTE MAXIMUM RATINGS

VBAT . . . . . +27V
VDD Maximum Forced Current 30mA
Maximum Forced Voltage 17V
BUCK . . . . . –5V to VBAT
MODE . . . . . –0.3V to 3.2V
Operating Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

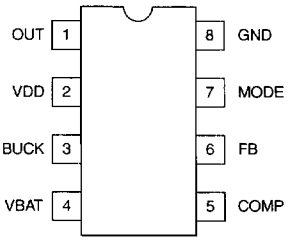
Unless otherwise indicated, currents are positive into, negative out of the specified terminal. Pulse is defined as less than 10% duty cycle with a maximum duration of 500µs. Consult Packaging Section of Databook for thermal limitations and considerations of packages. All voltages are referenced to GND.

CONNECTION DIAGRAMS

TSSOP-8 (TOP VIEW)
PW Package



DIL-8 (TOP VIEW)
D, J, N Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications hold for T_A=0°C to +70°C for the UC3972, –40°C to +85°C for the UC2972, and –55°C to +125°C for the UC1972; T_A=T_J; VDD=VBAT=VBUCK=12V; MODE=OPEN. For any tests with VBAT>17V, place a 1K resistor from VBAT to VDD.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input supply					
VDD Supply Current	VDD = 12V		1	1.5	mA
	VBAT = 25V		7	10.5	mA
VBAT Supply Current	VBAT = 12V		30	60	µA
	VBAT = 25V		70	140	µA
VDD Regulator Turn-on Voltage	I_{SOURCE} = 2mA to 10mA	17	18	19	V
VDD UVLO Threshold	Low to high		4	4.4	V
UVLO Threshold Hysteresis		100	200	300	mV
Output Section					
Pull Down Resistance	I_{SINK} = 10mA to 100mA		50	75	Ω
Pull Up Resistance	I_{SOURCE} = 10mA to 100mA		50	75	Ω
Output Clamp Voltage	VBAT = 25V, Shunt Regulator on		16	18	V
Output Low	MODE = 0.5V, I_{SINK} = 1mA		0.05	0.2	V
Rise Time	CL = 1nF, Note 1		200		ns

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PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time	CL = 1nF, Note 1		200		ns
Oscillator					
Minimum Frequency	BUCK = VBAT – 2	52	66	80	kHz
Maximum Synchronizable Frequency	BUCK = VBAT	160	200	240	kHz
Voltage Stability	BUCK = VBAT = 12V to 25V		5	7	%
Maximum Duty Cycle	FB = 1V	92	95		%
Minimum Duty Cycle	FB = 2V			0	%
BUCK Input Bias Current	BUCK = VBAT = 12V		40	90	µA
Zero Detect Threshold	Measured at BUCK w/respect to VBAT	–0.95	–0.75	–0.55	V
Error Amplifier					
Input Voltage	COMP = 2V	1.465	1.5	1.535	V
Input Bias Current		–500	–100		nA
Open Loop Gain	COMP = 0.5 to 3.0V	60	80		dB
Output High Voltage	FB = 1V	3.3	3.7	4.1	V
Output Low Voltage	FB = 2V		0.15	0.35	V
Output Source Current	FB = 1V, COMP = 2V		–1.2	–0.4	mA
Output Sink Current	FB = 2V, COMP = 2V	45	90		µA
Output Source Current	FB = 1V, COMP = 2V, MODE = 0.5V	–1		1	µA
Output Sink Current	FB = 2V, COMP = 2V, MODE = 0.5V	–1		1	µA
Unity Gain Bandwidth	YJ = 25C, Note 1		2		MHz
Mode Select					
Output Enable Threshold		0.85	1	1.15	V
Open Lamp Detect Enable Threshold		2.75	3	3.25	mV
Mode Output Current	MODE = 0.5V	15	20	25	µA
MODE Clamp Voltage	MODE = OPEN	3.3	3.7	4	V
DIM					
Open Lamp Detect Threshold	Measured at BUCK with respect to VBAT	–12	–10	–8	V

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PIN DESCRIPTIONS

BUCK: Senses the voltage on the top side of the inductor feeding the resonant tank. The voltage at this point is used to synchronize the internally generated ramp, and is also used to detect whether an open lamp condition exists. An open lamp condition exists when this voltage is below the specified threshold for seven clock cycles. If the MODE pin is held below the open lamp detect enable threshold, this protective feature is disabled.

COMP: Output of the error amplifier. Compensation components set the bandwidth of the entire system and are normally connected between COMP and FB. The error amplifier averages lamp current against a fixed internal reference. The resulting voltage on the COMP pin is compared to an internally generated ramp, setting the PWM duty cycle. During UVLO, this pin is actively pulled low.

FB: This pin is the inverting input to the error amplifier.

GND: Ground reference for the IC.

MODE: The voltage on this pin is used to control start-up and various modes of operation for the part (refer to the table in the block diagram).

When the voltage is below 1V, OUT is forced low, open lamp detection is disabled and the error amplifier is tri-stated.

When the voltage is between 1V and 3V, OUT is enabled and the error amplifier output is connected to COMP. Open lamp detection is still disabled and a constant 20µA cur-

PIN DESCRIPTIONS (cont.)

rent is sourced from this pin. Placing an appropriate value external capacitor between this pin and ground allows the user to disable open lamp detection for a set period of time at start-up to allow the lamp to strike.

When MODE reaches 3V, open lamp detection is enabled and normal operation is activated.

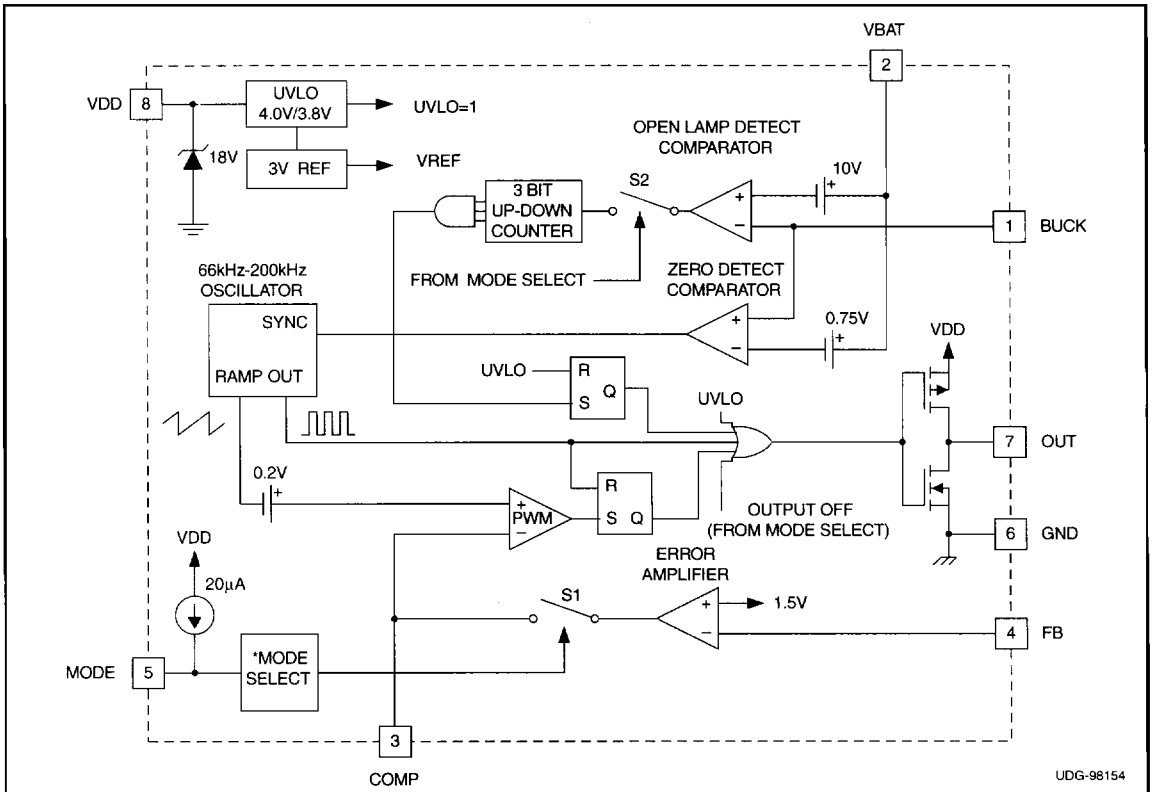
A square wave can be applied to this pin allowing a low frequency dimming technique to be implemented.

OUT: Drives the buck regulator N-channel MOSFET. OUT turn-on is synchronized to twice the tank resonant frequency. OUT is actively pulled low when in UVLO, an open lamp condition has been detected or MODE is less than 1V.

VBAT: Positive input supply to power stage. This voltage is required by internal control circuitry to provide open-lamp detection and synchronization. Operating range is from 4.5V to 25V.

VDD: This pin connects to the battery voltage from which the CCFL inverter will operate. If the potential on VBAT can exceed 18V in the application, a series resistor must be placed between VBAT and this pin (see applications section). The voltage at the VDD pin will then be regulated

BLOCK DIAGRAM



*MODE	Output	Open Lamp Detection	S2	Error Amplifier Output	S1
<1V	OFF	DISABLED	OPEN	DISCONNECTED FROM COMP	OPEN
1V< MODE< 3V	ON	DISABLED	OPEN	CONNECTED TO COMP	CLOSED
>3V	ON	ENABLED	CLOSED	CONNECTED TO COMP	CLOSED

APPLICATION INFORMATION (cont.)

Introduction

Cold Cathode Fluorescent Lamps (CCFL) are frequently used as the backlight source for Liquid Crystal Displays (LCDs). These displays are found in numerous applications such as notebook computers, portable instrumentation, automotive displays, and retail terminals. Fluorescent lamps provide superior light output efficiency, making their use ideal for power sensitive portable applications where the backlight circuit can consume a significant portion of the battery's capacity. The backlight converter must produce the high voltage needed to strike and operate the lamp. Although CCFLs can be operated with a DC voltage, a symmetrical AC operating voltage is recommended to maintain the rated life of the lamp. Sinusiodal voltage and current lamp waveforms are also recommended to achieve optimal electrical to light conversion and to reduce high voltage electromagnetic interference (EMI). A topology that provides these requirements while maintaining efficient operation is presented in Fig. 1.

Circuit Operation

A current fed push-pull topology is used to power the CCFL backlight shown in Fig. 1. This topology accommodates a wide input voltage and dimming range while retaining sinusoidal operation of the lamp. The converter consists of a resonant push-pull stage, a high voltage output stage, and a buck pre-stage used to regulate current in the converter.

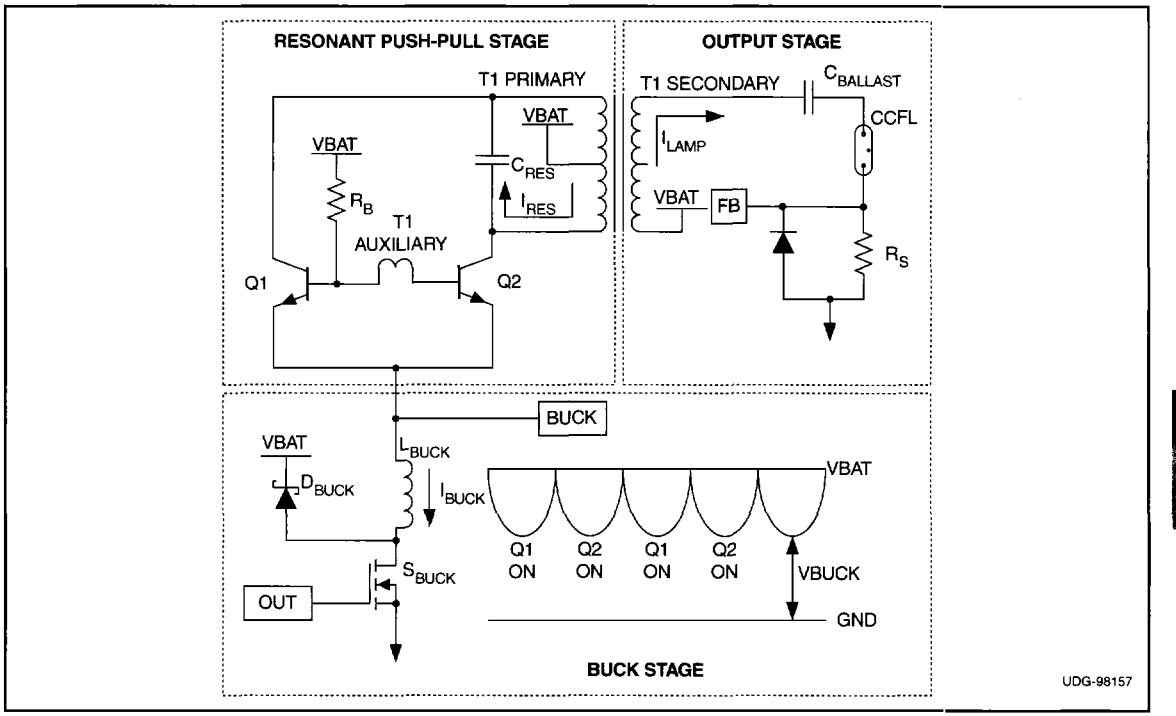


Figure 1. Push-pull, output and buck stages.

Referring to Fig. 1, the push-pull stage consists of C_{RES}, Q1, Q2, Rb, and T1's primary and auxiliary windings. The output stage consists of $C_{BALLAST}$, the lamp, the current sense resistor Rs, and T1's secondary. The resonant frequency of the tank is set by the primary inductance of T1, along with the resonant capacitor (C_{RES}), and the reflected secondary impedance. The secondary impedance includes the lamp, the ballast capacitor ($C_{BALLAST}$), the distributed winding capacitance of T1, and the stray capacitance which forms between the lamp, lamp wires, and the backlight reflector. Since the lamp impedance is nonlinear with operating current, the tank resonant frequency will vary slightly with load (typically 1.5:1).

The primary resonant tank consisting of T1's primary inductance and C_{RES} produces a sinusoidal current (I_{RES}) and is fed by a controlled DC current (I_{BUCK}) from the buck stage. Note that the BUCK node voltage is 1/2 the primary

APPLICATION INFORMATION (cont.)

tank voltage, as VBAT is located at the center tap of the transformer. The high turns ratio transformer (T1) amplifies the sinusoidal tank voltage to produce a sinusoidal secondary voltage that is divided between the lamp and ballast capacitor. Due to the winding construction of T1, the secondary voltage has a small DC offset (VBAT). This DC component is blocked by $C_{BALLAST}$ and has no effect on lamp operation. $C_{BALLAST}$ also provides high output impedance, allowing the secondary current (I_{LAMP}) to remain sinusoidal driving the highly nonlinear lamp load.

Transistors Q1 and Q2 are driven out of phase at 50 percent duty cycle with an auxiliary winding on T1. The winding provides a floating AC voltage source at the resonant frequency that is used to drive the transistor bases alternately on and off. One leg of the auxiliary winding is tied to the input voltage through base resistor Rb, which is sized to provide sufficient base current to the transistors. The transistors channel the buck inductor current into opposing ends of the tank at the resonant frequency, supplying energy for the lamp and system losses.

The buck power stage consists of inductor L_{BUCK}, MOSFET switch S_{BUCK}, and flyback diode D_{BUCK}. In order to prevent interactions between multiple switching frequencies, the UCC3972 synchronizes the buck frequency to the frequency of the push-pull stage. The traditional buck topology is inverted to take advantage of the lower R_{dsON} characteristics of an N-Channel MOSFET switch (S_{BUCK}). With a sinusoidal voltage across the tank, the resulting output of the buck stage (V_{BUCK}) becomes a full-wave rectified voltage referenced to VBAT as shown in Fig. 1.

Lamp current is sensed directly with Rs and a parallel diode on each half cycle. The resulting voltage across the sense resistor Rs is kept at a 1.5V average by the error amplifier, which in turn controls the duty cycle of S_{BUCK}. The buck converter typically operates in continuous current mode but can operate with discontinuous current as the CCFL is dimmed.

Typical Design Procedure

A notebook computer backlight circuit will be presented here to illustrate a design based on the UCC3972 controller. The converter will be designed to drive a single cold cathode fluorescent lamp (CCFL) with the following specifications:

Table 1. Lamp Specifications

Lamp Length	250mm (10")
Lamp Diameter	6mm
Striking Voltage (20C)	1000V (peak)
Operating Voltage (5mA)	375V (rms)
Full Rated Current	5mA
Full Rated Power	1.9 watt

Input Voltage Range

The notebook computer will be powered by a 4 cell Lithium-Ion battery pack with an operational voltage range of 10V to 16.8V. When the pack is being charged, the back light converter is powered from an AC adapter whose DC output voltage can be as high as 22V.

Resonant Tank and Output Circuit

The selection of components to be used in the resonant tank of the converter is critical in trading off the electrical and optical efficiencies of the system. The value of the output circuit's ballast capacitor plays a key role in this tradeoff. The voltage across the ballast capacitor is a function of the resonant frequency and secondary lamp current:

$$V_{CB} = \frac{I_{LAMP}}{2 \bullet \pi \bullet C_{BALLAST} \bullet F_{RESONANT}} \quad (1)$$

A voltage drop across $C_{BALLAST}$ many times the lamp voltage will make the secondary current insensitive to distortions caused by the non-linear behavior of the lamp, providing a high impedance sinusoidal current source with which to drive the CCFL. This approach improves the optical efficiency of the system, as capacitive leakage effects are minimized due to reduced harmonic content in the voltage waveforms. Unfortunately, from an electrical efficiency standpoint, an increased tank voltage produces increased flux losses in the transformer and increased circulating currents in the tank. In practice, the voltage drop across the ballast capacitor is selected to be approximately twice the lamp voltage (750Vin our case) at rated lamp current. Assuming a 50kHz resonant frequency and 5mA operating current, a ballast capacitance of 22pF is selected. Since the lamp and ballast capacitor impedances are 90 degrees out of phase, the vector sum of lamp and capacitor voltages determine the secondary voltage on the transformer.

$$V_{SEC} = \sqrt{(V_{CB})^2 + (V_{LAMP})^2} \quad (2)$$

The resulting secondary voltage at rated lamp current is 840V. Since the capacitor dominates the secondary impedance, the lamp current maintains a sinusiodal shape despite the non-linear behavior of the lamp. As the CCFL is dimmed, lamp voltage begins to dominate the secondary

APPLICATION INFORMATION (cont.)

impedance and current becomes less sinusiodal. Transformer secondary voltage is reduced, however, so high frequency capacitive losses are less pronounced. The value of ballast capacitor has no effect on current regulation since the average lamp current is sensed directly by the controller.

Once the ballast capacitor is selected, the resonant frequency of the push-pull stage can be determined from the transformer's inductance (L), turns ratio (N), and the selection of resonating capacitor (C_{RES}).

$$F_{RESONANT} = \frac{1}{2\pi\sqrt{L_{PRIMARY}\left(C_{RES} + \left(N^2 \bullet C_{BALLAST}\right)\right)}} \quad (3)$$

Output distortion is minimized by keeping the independent resonant frequencies of the primary and secondary circuits equal. This is achieved by making the resonant capacitor equal to the ballast capacitance times the turns ratio squared:

$$C_{RES} = N^2 \bullet C_{BALLAST} = (67)^2 \bullet 22pF = 0.1\mu F \quad (4)$$

The Coiltronics transformer selected for this application produces a of primary inductance of 44µH.

The resulting resonant frequency is about 50kHz, this frequency will vary depending upon the lamp load and amount of stray capacitance in the system.

Efficiency Considerations for the Resonant Tank and Output Circuit

Since high efficiency is a primary goal of the backlight converter design, the selection of each component must be carefully evaluated. Losses in the ballast capacitor are usually insignificant, however, its value determines the tank voltage which influences the losses in the resonant capacitor and transformer. Since the resonant capacitor has high circulating currents, a capacitor with low dissipation factor should be selected. Power loss in the resonant tank capacitor will be:

$$C_{RES\_LOSS}(watts) = (C_{TANK})^2 \bullet 2\pi \bullet F_{RESONANT} \bullet C_{RES} \bullet Dissipation\,Factor \quad (5)$$

Polypropylene foil film capacitors give the lowest loss; metalized polypropylene or even NPO ceramic may give acceptable performance in a smaller surface mount (SMT) package. Table 2 gives possible choices for the resonant and high voltage ballast capacitors.

The transformer is physically the largest component in the converter, making the tradeoff of transformer size and efficiency a critical choice. The transformer's efficiency will be determined by a combination of wire and core losses. A Coiltronics transformer (CTX110600) was chosen for this application because of its small size, low profile, and overall losses of about 5% at 1W.

Wire losses in the transformer are determined by the RMS current and the ESR of the windings. The primary winding resistance for the Coiltronics transformer is 0.16Ω. The RMS current of the primary winding includes the sinusoidal resonant current and the DC buck current on alternate half cycles (i.e. only 1/2 of the primary winding sees the buck current depending upon which transistor is on). Maximum resonant current is equal to:

$$I_{RES} = \frac{V_{PRIMARY}}{\sqrt{\frac{L_{PRIMARY}}{C_{RES}}}} = \frac{840}{67 \bullet \sqrt{\frac{44}{0.1}}} = 600\,mA \quad (6)$$

Buck inductor current is calculated in the next section. The secondary winding has 176Ω of resistance.The secondary current is simply the lamp current

Transformer core losses are a function of core material, cross sectional area of the core, operating frequency, and

Table 2. Capacitor Selection

Manufacturer	Capacitance Type	Series	Dissipation Factor (1kHz)
Ballast Capacitor			
Cera-Mite (414) 377-3500	High Voltage Disk Capacitor (3kV)	564C	
NOVA-CAP (805) 295-5920	SMT 1808 (3kV)	COG	
Murata Electronics	SMT 1808 (3kV)	GHM	
Resonant Capacitor			
Wima (914)347-2474	Polypropylene foil film FKP02	FKP02	0.0003
	Metalized Polypropylene	MKP2	0.0005
	SMT Metalized polyphenylene-sulfide	MKI	0.0015
Paccom (800)426-6254	SMT Metalized polyphenylene-sulfide	CHE	0.0006
NOVA-CAP	SMT Ceramic	COG	0.001

APPLICATION INFORMATION (cont.)

voltage. For ferrite material, the hysteresis core losses increase with voltage by a cubed factor; for a given core cross sectional area, doubling the tank voltage will cause the losses to increase by a factor of 8.

Other elements influencing the resonant tank and output circuit efficiency include the push-pull transistors, the base drive and sense resistors, as well as the lamp. High gain, low VCESAT bipolar transistor such as Zetek's FZT849 allow high efficiency operation of the push-pull stage. These SOT223 package parts have a typical current transfer ratio (hFE) of 200 and a forward drop (VCE-SAT) of just 35mV at 500mA. Rohm's 2SC5001 transistors provide similar performance. For low power, size sensitive applications, a SOT23 transistor is available from Zetek (FFMT619) with approximately twice the forward drop at 500mA. The base drive resistor R_B is sized to provide full VCE saturation for all operating conditions assuming a worst case hFE. For efficiency reasons, the base resistor should be selected to have the highest possible value. A 1kΩ resistor was selected in this application. Losses scale with buck voltage as:

$$LOSS_{RB(watts)} = \frac{(V_{BUCK})^2}{R_B} \quad (7)$$

The current sense resistor Rs provides direct control of lamp current. Since the current sense resistor voltage is controlled to a 1.5V reference, its power loss is inversely proportional to its value at a given lamp current. Finally, the efficiency of the lamp is typically not included in discussions about the electrical efficiency of the system. Electrical to optical efficiency of the lamp is discussed in a later section titled *Cold Cathode Fluorescent Lamp Characteristics.*

Synchronizing the Stages

An internal comparator at the BUCK node is used to synchronize the PWM buck frequency to twice the resonant tank frequency. Synchronization is accomplished with a sync pulse that is generated each time the BUCK node voltage is within 0.75Vof VBAT; the UCC3972 uses this sync pulse to reset the PWM oscillator's saw-tooth ramp. The sync circuit will operate with PWM frequencies between 66kHz and 200kHz, corresponding to a 33kHz to 100kHz tank frequency. If the resonant frequency of the tank is outside of this range, the PWM frequency will run asynchronous.

Buck Stage

The PWM output controls current in the buck inductor. The UCC3972's buck power stage differs from a traditional buck topology in a few respects:

- The topology is inverted using a ground referenced N-Channel MOSFET rather than a VDD referenced P-Channel.
- The output voltage is a full wave rectified sinewave at the switching frequency, rather than DC.

Referring back to Fig. 1, when OUT turns S_{BUCK} on, the buck node voltage VBUCK is placed across the inductor. This voltage is typically positive and current ramps up in the inductor (it is possible for the BUCK node voltage to go negative if VBAT is low and the lamp current is near maximum). When S_{BUCK} is turned off, VBAT--VBUCK+VDBUCK is placed across the inductor with opposite polarity. As with any buck converter, the volt-seconds across the inductor must be reversed on each switching cycle to maintain constant current. The duty cycle (D) relationship is complicated somewhat by the fact the output voltage is changing within a switching cycle. The equations below determine the relationship between on and off times in continuous conduction mode where T is the switching period, D = t_{ON}/T, and t_{OFF} = T–t_{ON}.

$$\int_0^{t_{ON}} V_{BUCK} \bullet dt = \int_{t_{ON}}^{T} (VBAT - V_{BUCK} + V_D) \bullet dt \quad (8)$$

Selecting the Buck Inductor

Maximum ripple current on the inductor occurs when lamp current and input voltage are at a maximum.

$$V_{BUCK(avg)} = V_{BAT} - \frac{V_{SEC} \bullet \sqrt{2}}{N \bullet \pi} \quad (9)$$

$$= V_{BAT} - \frac{840 \bullet \sqrt{2}}{67 \bullet \pi} = V_{BAT} - 5.6 \bullet Volts$$

The approximate on time using the maximum 22V input voltage ($V_{BUCK\ (avg)}$=16.4), a 100kHz switching frequency (two times the resonant frequency), and ignoring the diode drop can be calculated from the following:

$$\frac{t_{ON}}{T - t_{ON}} = \frac{VBAT - V_{BUCK(avg)}}{V_{BUCK(avg)}} \quad (10)$$

The resulting on time is 2.5 microseconds. A 150µH inductor will result in a peak to peak ripple current of 280mA. Average inductor current (with maximum lamp current) can be calculated by taking the lamp power divided by the tank efficiency and the RMS buck voltage.

APPLICATION INFORMATION (cont.)

$$I_{BUCK} = \left(\frac{V_{LAMP} \bullet I_{LAMP}}{Efficiency}\right) \bullet \frac{2 \bullet N}{V_{SEC}} = \frac{375 \bullet 0.005 \bullet 2 \bullet 67}{0.9 \bullet 840} \quad (11)$$

$$= 330\,mA$$

The resulting inductor ripple is less than 50%. A list of possible inductors are given below along with ESR and current rating (losses in the inductor are calculated with RMS current).

Table 3. Inductor Suppliers

Vendor	L	Part Number	ESR	Current Rating
Coilcraft (847) 639-6400	150µH	DO3316-154	0.38	1A
Coiltronics (407) 241-7876	150µH	CTX150-4	0.175	0.72A
Sumida (847) 956-0666	150µH	CDR125-151	0.4	0.85A

The choice of a MOSFET for the buck switch should take into consideration conduction and switching losses. The Rds_{ON} and gate charge are typically at odds, however, where minimizing one will typically result in the other increasing. An International Rectifier IRFL014 was selected (SOT-223 package) in this application with a gate charge of 11nC and Rds_{ON} of 0.2Ω. A Schottky diode should be used for the buck diode in order to minimize forward drop.

Dimming Techniques

Analog Dimming

A control circuit that implements analog dimming with a potentiometer (R_{ADJ}) is shown in Fig. 2. Average lamp current is controlled by adjusting R_{ADJ} to the appropriate value. Resistor R_L sets the low end dimming level of the lamp. When the secondary has a positive polarity current, D1 is reversed biased and lamp current is sensed directly through R_L and R_{ADJ}. When the current reverses direction, D1 conducts and the voltage on the sense node V is clamped to the forward drop of the diode. The resulting waveform at V_X is a half wave rectified sinusoid whose voltage is proportional to lamp current. This voltage is averaged by the feedback components (R_{FB}, C_{FB}) and held to 1.5V by the error amplifier when the control loop is active. The resulting voltage at the output of the error amplifier (COMP) sets the duty cycle of PWM stage.

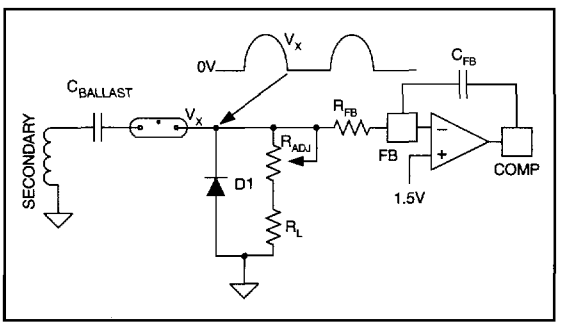


Figure 2. Analog dimmer with potentiometer.

Digitally Controlled Analog Dimming

Analog dimming control of the lamp can be achieved by providing a digital pulse stream from the system microprocessor as shown in Fig. 3. In this case the lamp current sense resistor (R1) is fixed and the VX node voltage

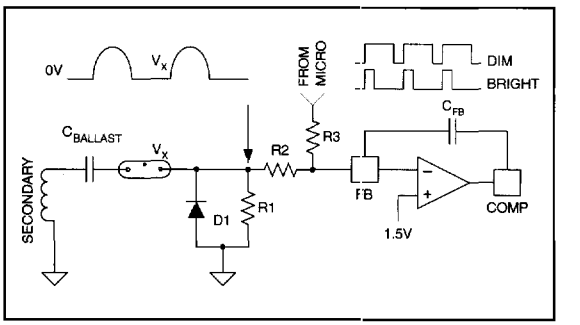


Figure 3. Analog dimming control from microprocessor

is averaged against the digital pulse stream of the microprocessor. The averaging circuit consists of R2, R3, and C_{FB}. A higher average value from the pulse stream will result in less average lamp current. If a D/A converter is available in the system, a DC output can be used in place of the pulse stream.

Low Frequency Dimming

Analog dimming techniques described previously can provide excellent dimming over a 10 1 range, depending upon the physical layout and the amount of stray capacitance in the backlight's secondary circuitry. Beyond this level the lamp may begin to exhibit the "*thermometer effect*" causing uneven illumination across the tube.

Low frequency dimming is accomplished by operating the lamp at rated current and gating the lamp on and off at a low frequency. Since the lamp is operated at full intensity when on, the system layout has little effect on dimming performance. The average lamp intensity is a function of the duty cycle and period of the gating signal.

APPLICATION INFORMATION (cont.)

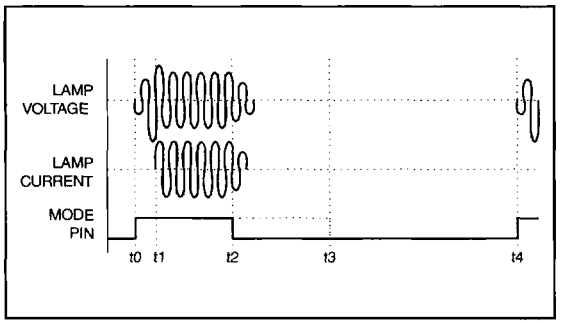


Figure 4. Low frequency dimming with the UCC3972 MODE pin.

The duty cycle can be controlled to a low minimum value, allowing a very wide dimming range. Low frequency dimming can be implemented by using the MODE pin on the UCC3972 as shown in Fig. 4.

Referring to Fig. 4, at time t0 the MODE pin is brought high, the UCC3972 is enabled and the voltage in the resonant tank begins to build. At time t1 there is sufficient voltage for the lamp to strike and the feedback loop controls the lamp at rated current using a fixed current sense resistor. When the mode pin is brought low at time T2, the feedback loop opens (retaining the voltage on CFB) and the PWM output is disabled. The resonant tank voltage decays until the lamp extinguishes. If the on time were extended to t3 the average lamp intensity would be increased accordingly, the next low frequency cycle begins at time t4. The time relationship between the resonant and gating frequency has been exaggerated so that the sinusoidal waveforms can be depicted. In order to avoid visible lamp flicker, the low frequency gating rate (t0-t4) should be greater than 100Hz. To prevent "beat" frequency interference, it may be advantageous to synchronize the gating frequency to a multiple of the monitor scan rate of the LCD display. This can be accomplished by controlling the MODE pin's duty cycle with a timer routine within the LCD's software program.

Depending on the striking characteristics of the lamp, the open lamp detection circuit may need to be altered to accomodate low frequency dimming. The open lamp threshold can be increased by adding a resistive divider at the buck node. An RC delay network can be added to the MODE pin to slow the slew rate between 1V and 3V. Finally, the open lamp protection can be disabled by restricting the MODE pin to toggle between 0V and 2V during frequency dimming.

Striking the Lamp

Before the lamp is struck, the lamp presents an impedance much larger than the ballast capacitor and the full output voltage of the transformer secondary is across the lamp. Since the buck converter must reverse the volt -seconds on the buck inductor, the average tank voltage at the primary can be no greater than the DC input voltage. This constraint along with the turns ratio of the push-pull transformer sets the peak voltage available to strike the lamp:

$$V_{STRIKE} = N_{S:P} \bullet \pi \bullet V_{INPUT} \qquad (12)$$

The Coiltronics transformer has a 67:1 turns ratio, giving 2100 peak volts available to strike the lamp with the minimum 10V input. In our example this is more than sufficient for the 1000V required to strike the lamp. With the 22V maximum charger input, the available striking voltage could theoretically reach 5000V! The possibility of breaking down the transformer's secondary insulation becomes a real concern at this voltage. Fortunately, in practice the lamp will strike within the first few cycles once sufficient voltage is developed on the secondary. Difficulty with striking the lamp usually results from one or a combination of the following:

- Insufficient transformer turns ratio or input voltage.
- Increase in required striking voltage at cold temperature.
- Transformer secondary voltage is reduced due to voltage division between parasitic secondary capacitance and the ballast capacitor.

Open Lamp Protection / Detection

Open lamp protection provides safety and will often protect the transformer and converter circuitry in the event of a broken or open circuited lamp. Referring to the Block Diagram, the UCC3972 monitors the BUCK pin voltage with respect to VBAT to determine if an open lamp has occurred. If this voltage exceeds 10V for seven consecutive PWM cycles, an open lamp will be declared and the converter will latch off until power to the part is cycled off and on. If the open lamp fault level needs to be increased, an appropriate resistive divider from VBAT to BUCK can be added.

A capacitor on the MODE pin of the UCC3972 can be used to blank the open lamp protection circuitry during the initial lamp start-up. When the backlight is initially powered-up, a 20μA current out of the MODE pin charges the capacitor CMODE from ground potential. Since the PWM output is disabled when the MODE pin is between 0V and 1V, open lamp blanking occurs as CMODE is charged from 1V to 3V, giving a soft start period of:

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$$T_{SS} = \frac{C_{MODE}}{10^{-6}} \text{ Seconds} \quad (13)$$

Voltage Regulator

The UCC3972 controller contains an internal 18V shunt regulator that provides a 5% accurate voltage clamp for the MOSFET gate drive while allowing the controller to operate in applications with input voltages up to 25V. Since only the VBAT and BUCK pins are rated for 25V, the shunt regulator limits the voltage on the VDD and OUT pins to 18V. The MODE, CS, and COMP pin voltages are typically less than 5V. If the UCC3972 is to be used in an application with input voltages greater than 18V, a resistor from VBAT to VDD is required to limit the current into the VDD pin. The resistor should be sized to allow sufficient current to operate the controller and drive the external MOSFET gate, while minimizing the voltage drop across the resistor. A bypass capacitor should be connected at the VDD pin to provide a constant operating voltage.

Selecting the Shunt Resistor

The first step in selecting the shunt resistor is to determine the current requirements for the application. With a 100kHz switching frequency and a maximum gate charge of 11nC for the IRFL014 MOSFET, the gate drive circuit requires 1.1mA of average current. The UCC3972 requires an additional maximum quiescent current of 1.5mA. The shunt resistor must therefore supply 2.6mA of current over the operating voltage of the part.

The application's maximum input voltage is 22V. With a regulator clamp voltage of 18V, the maximum value for the shunt resistor becomes 1.5kΩ [(22-18)V/2.6mA]. This resistor will minimize losses at maximum input voltage, but could produce a 4V drop (from VBAT to VDD) even when the regulator is not clamped. This drop reduces the available gate drive voltage, leaving only 6V with the minimum input voltage of 10V. Since the efficiency of the shunt regulator is not of primary importance when the charger is running, a smaller value of shunt resistor is selected to improve the available gate drive voltage. A 470Ω shunt resistor will produce a maximum 1.2V drop from VBAT to VDD when the shunt regulator is not clamped. When the regulator is clamped at 18V and the charger voltage is at its maximum of 22V, the power across the shunt resistor will be 35mW [(4V x 4V)/470].

Lamp Current Control Loop

The control loop for the CCFL circuit is discussed in detail in Unitrode Application Note U-148 and is briefly repeated here for completeness. A block diagram for the current control loop is shown in Fig. 5.

The PWM modulator small signal gain is inversely proportional to the internal saw tooth ramp and proportional to the input voltage (the inductor's current slope increases as VBAT increases). The resonant tank and buck inductor form a RLC filter at the center point of the push pull transformer. The effective L of the filter is dominated by buck inductor and the effective C is approximately 8 times the resonant capacitor (C_{RES}) value. This occurs because the reflected ballast capacitance is equal

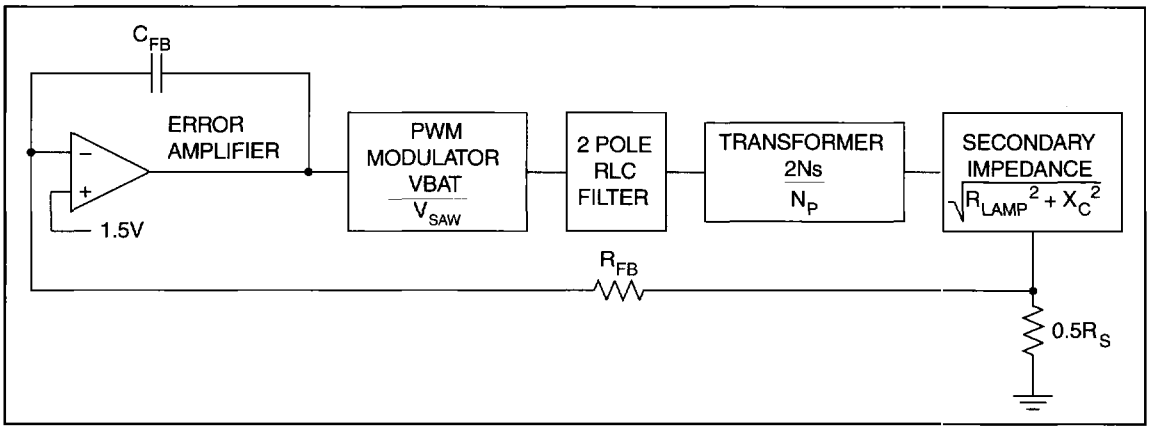

Figure 5. Current control loop block diagram.

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to C_{RES} and the equivalent capacitance at the push-pull center point is four times the capacitance across the tank. The equivalent resistance at the push-pull center point is equal to 1/4 the tank voltage squared divided by the lamp power. The corner frequency and Q of the filter are:

$$F_{CORNER} = \frac{1}{2\pi\sqrt{L_{BUCK} \bullet 8 \bullet C_{RES}}} \quad (14)$$

$$Q = \frac{2 \bullet \pi \bullet f_{FILTER} \bullet L_{BUCK}}{R_{FILTER}} \quad (15)$$

The resulting gain of the RLC filter is unity below the 15kHz corner frequency, peaking up at the corner frequency with Q, and rolling off with a 2-pole response above the corner frequency. As shown in Fig. 5, the transformer turns ratio provides a voltage gain and the output circuit (whose impedance includes the lamp and ballast capacitor) converts the voltage into a current. The current sense resistor produces a voltage on each half cycle, leaving the error amplifier as the final gain block.

Loop gain is greatest at minimum lamp current and maximum input voltage. With a 22V input, 2V sawtooth, 375V lamp voltage, 1mA lamp current, and Rsense at 1kΩ, the DC gain of the circuit is 2. The error amplifier is configured as an integrator, giving a single pole roll-off and a high gain at DC. The 200k feedback resistor and 1.8nF feedback capacitor give a total loop crossover of 1kHz, avoiding any possible stability problems with the Q of the resonant tank.

Cold Cathode Lamp Characteristics

Before beginning a CCFL converter design, it is important to become familiar with the characteristics of the lamp. The lamp presents a non-linear load to the converter resulting in unique voltage -vs- current (VI) characteristics. The length, diameter, and physical construction of the lamp determine its performance, and thus impact the design of the converter. Fig. 6 shows the VI characteristics collected from various lengths of 6mm diameter lamps, where Fig. 7 shows the characteristics of several 3mm-diameter lamps.

It is interesting to note how the operating and striking voltages (V_{STRIKE}) of the lamps are related to length as well as lamp diameter. Since equal length CCFLs of different diameters have about the same lumens per watt efficiency, the smaller diameter lamps actually produce more light when driven at a given current since they operate at a higher voltage. The lamps have regions of positive and negative resistance with the voltage peaking at 4mA for the 6mm diameter lamps and at 1mA for the 3mm diameter lamps.

In order to successfully dim the lamp, the converter's resonant tank and step up transformer must provide enough voltage to keep the lamp operating over the whole range of operating current, this requirement becomes more difficult with longer length and smaller di-

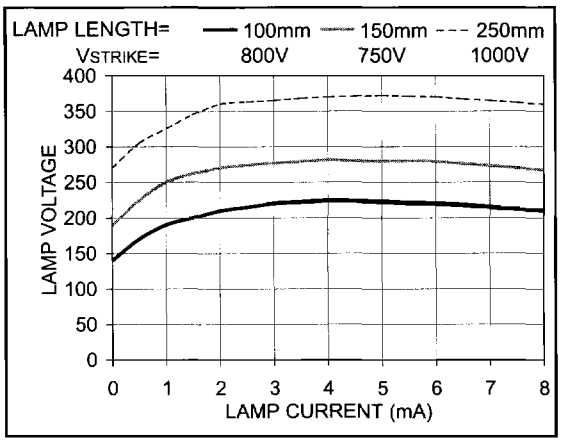

Figure 6. 6mm lamp characteristics.

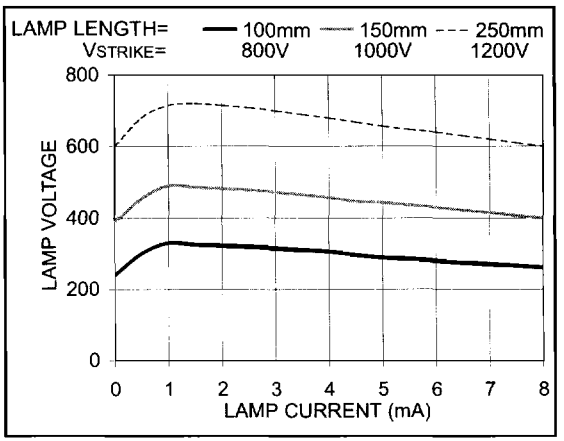

Figure 7. 3mm lamp characteristics.

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ameter lamps. Since the lamp characteristics will vary with the manufacturing technique, it is a good idea to collect data from several lamp manufacturers and to include design margin for process variations.

Since a fluorescent lamp is a pressurized gas filled tube (usually Argon and Mercury vapor), it shouldn't be surprising that temperature plays a major role in the lamp characteristics. Fig. 8 depicts the variations in striking and operating voltage for a 150 x 3mm lamp over temperature, illustrating the importance of taking temperature effects into account when designing the converter. The lumen output of the backlight system is temperature dependent as well, and may need to be accounted for in applications requiring tight lumens regulation over a wide temperature range. Fig. 9 shows the temperature effects on lumens for the lamp operated at 5mA.

Since lamp current is roughly proportional to luminosity, it may be tempting to operate the lamp at a RMS current higher than specified in the manufacturer's data sheet. While the lamp will continue to operate tens of percent above the rated current, the luminosity gain becomes

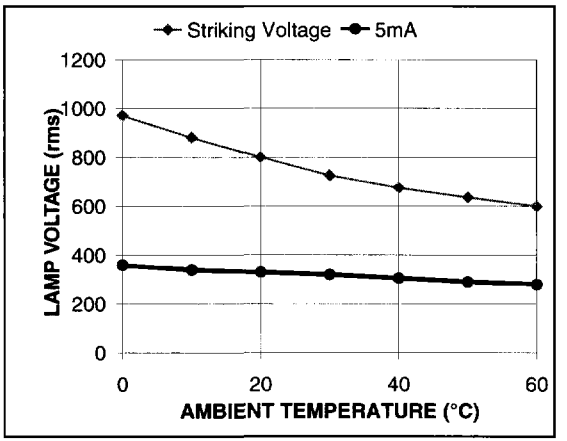

Figure 8. Temperature effects on voltage.

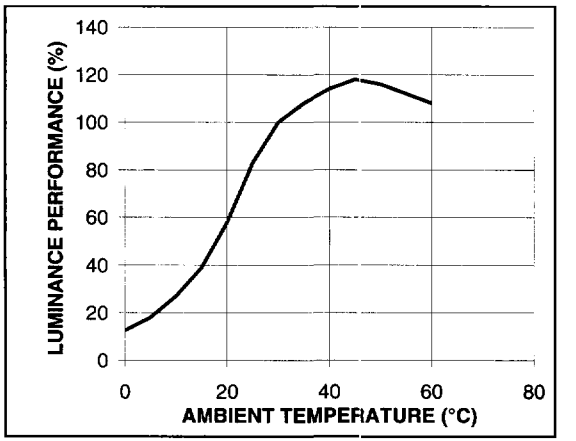

Figure 9. Temperature effects on lumens.

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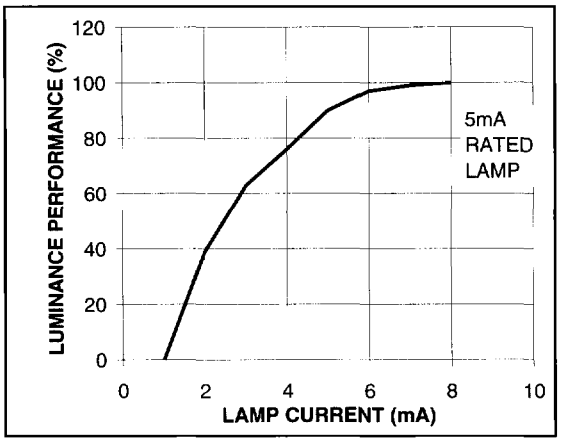

Figure 10. Lumens output vs. current.

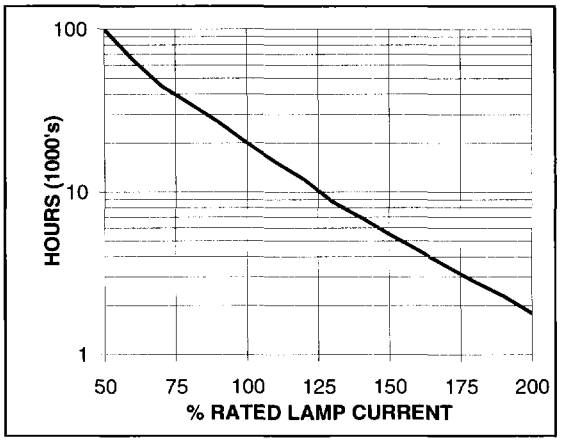

Figure 11. Lamp life vs. current.

less pronounced as the lamp is over-driven as shown in Fig. 10. The expected life of the lamp will also degrade, as illustrated in Fig. 11, when the lamp is operated above rated current.

Cold Cathode Fluorescent Lamp Efficiency

Although CCFLs offer high output light efficiency compared to other lamp types such as incandescent, only a percentage of the input energy is converted to light. As illustrated in Fig. 12, 35% of the energy is lost in the electrodes, 26% as conducted heat along the tube. A portion of the Ultra Violet energy gets converted into visible light by the lamp phosphor, where the remainder is converted into radiated heat. Finally, Mercury atoms convert 3% of the initial energy into visible light. The result is typically 15% overall electrical to optical energy conversion in the lamp.

In a practical backlight design, the physical spacing between the lamp and high voltage secondary wiring with respect to the foil reflector and LCD frame can be tight. With this tight spacing, distributed stray capacitance will form as shown in Fig. 12. The stray capacitance causes leakage currents from the high voltage secondary to circuit ground. Although the current through stray capacitance doesn't directly translate into losses, the extra current through the transformer, primary resonant tank, and switching devices does. A poor layout with excessive stray capacitance can reduce system efficiency by tens of percent.

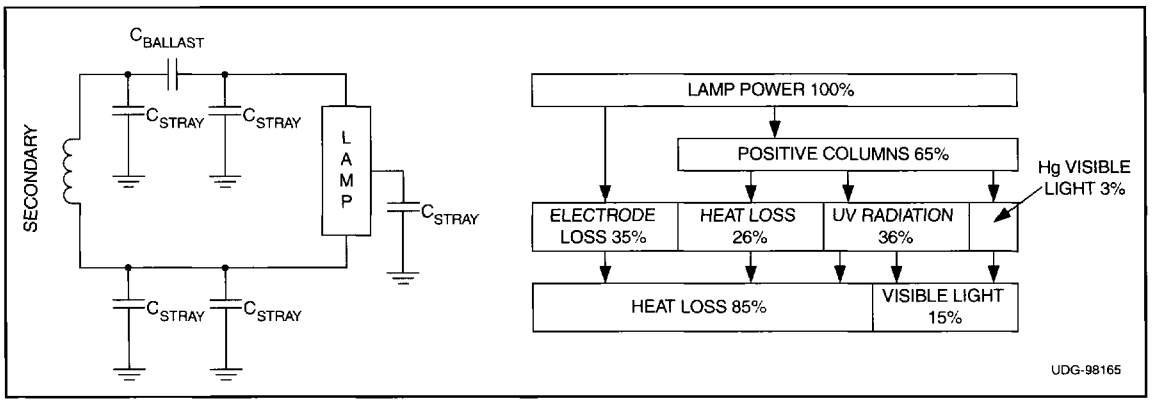

Figure 12. Lamp life vs. current.

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