HM4816

16384-word×1-bit Dynamic Random Access Memory

The HM4816 is a new generation MOS dynamic RAM circuit organized as 16,384 words by 1 bit. As a state-of-the art MOS memory device, the HM4816 (16K RAM) incorporates advanced circuit techniques designed to provide wide operating margins, both internally and to the system user, while achieving performance levels in speed and power previously seen only in MOSTEK's high performance MK4027 (4K RAM).

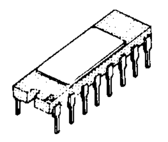
The technology used to fabricate the HM4816 is HITACHI's double-poly, N-channel silicon gate process.

This process, coupled with the use of a single transistor dynamic storage cell provides the maximum possible circuit density and reliability, while maintaining high performance capability.

The use of dynamic circuitry throughout, including sense amplifiers, assures that power dissipation is minimized without any sacrifice in speed or operating margin. These factors combine to make the HM4816 a truly superior RAM product.

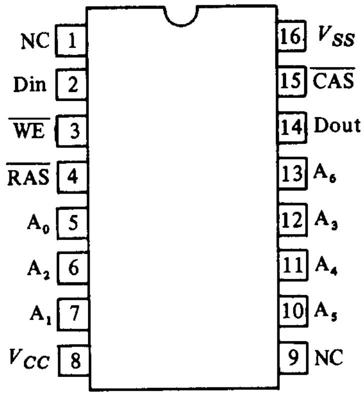
Multiplexed address inputs (a feature pioneered by MOSTEK for its 4K RAMs) permits the HM4816 to be packaged in a standard 16-pin DIP.

This recognized industry standard package configuration, while compatible with widely available automated testing and insertion equipment, provides highest possible system bit densities and simplifies system upgrade from 4K to 16K RAMs Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.



(DC-16)

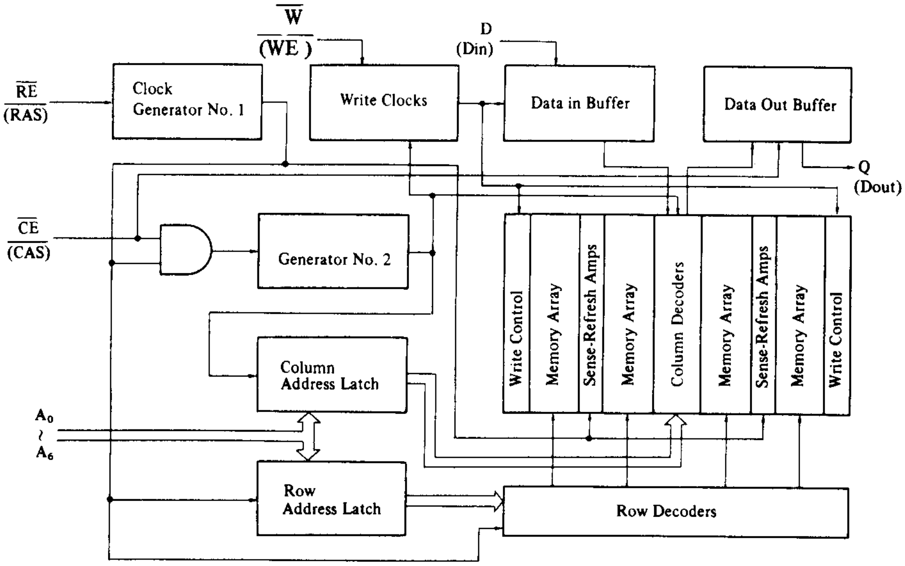
■ PIN ARRANGEMENT



(Top View)

■ FEATURES

- Single 5V supply
- Low power standby and operation
  (Standby: 55mW max, operation: 440mW max)
- Fast access time & cycle time
  (access time: 100ns max, cycle time: 200ns min)
- Directly TTL compatible: All inputs & outputs
- Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow two dimensional chip selection and extended page boundary
- Common I/O capability using "early write" operation
- Read modify write, $\overline{RAS}$ only refresh and page mode capability



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM4816	Unit
Voltage on any pin relative to GND	V_T	−1.0~+7.0	V
Power supply voltage relative to GND	V_{CC}	−0.5~+7.0	V
Short-circuit Output Current	I_{out}	50	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0~+70	°C
Storage Temperature	T_{stg}	−65~+150	°C

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Units	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
	V_{SS}	0	0	0	V	1, 2
Input high (logic 1) voltage $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	V_{IHC}	2.7	—	6.0	V	1
Input high (logic 1) voltage except $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	V_{IH}	2.7	—	6.0	V	1
Input low (logic 0) voltage all inputs	V_{IL}	−1.0	—	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}.
2. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

■ DC ELECTRICAL CHARACTERISTICS

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Operating current	I_{CC1}	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling, t_{RC}=200ns, Note 2	—	—	80	mA
Standby current	I_{CC2}	$\overline{\text{RAS}}$=V_{IHC}, Dout = high impedance	—	—	10	mA
Refresh current	I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}}$=V_{IHC}; t_{RC}=200ns	—	—	55	mA
Page mode current	I_{CC4}	$\overline{\text{RAS}}$=V_{IL}, $\overline{\text{CAS}}$ cycling, t_{PC}=120ns; Note 2	—	—	55	mA
Input leakage current	$I_{I(L)}$	V_{IN}=0 to 6V, all other pins=0V	−10	—	10	μA
Output leakage current	$I_{O(L)}$	V_{OUT}=0 to 5.5V, Dout is disabled	−10	—	10	μA
Output high voltage	V_{OH}	Note 1, I_{out} = −5mA	2.4	—	V_{CC}	V
Output low voltage	V_{OL}	I_{OUT}=4.2mA	—	—	0.4	V

Notes: 1. Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading.

2. I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

■ A.C. ELECTRICAL CHARACTERISTICS (Ta=0 to 70℃, V_{CC}=5.0V±10%)

Item	Symbol	min.	typ.	max.	Unit	Note
Random read or write cycle Time	t_{RC}	200	—	—	ns	3
Read-write Cycle Time	t_{RWC}	200	—	—	ns	3
Page Mode Cycle Time	t_{PC}	120	—	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	—	100	ns	4, 6
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	—	65	ns	5, 6
Output Buffer Turn-off Delay	t_{OFF}	0	—	25	ns	7
Transition Time (rise & fall)	t_T	3	—	25	ns	2
$\overline{\text{RAS}}$ Precharge	t_{RP}	65	—	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	100	—	10000	ns	
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	65	—	—	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	65	—	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	15	—	35	ns	8
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	40	—	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	—	ns	
Row Address Hold Time	t_{RAH}	15	—	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	—	ns	
Column Address Hold Time	t_{CAH}	35	—	—	ns	
Column Address Hold Time reference to $\overline{\text{RAS}}$	t_{AR}	70	—	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	—	ns	
Read Command Hold Time	t_{RCH}	10	—	—	ns	
Write Command Hold Time	t_{WCH}	40	—	—	ns	
Write Command Hold Time reference to $\overline{\text{RAS}}$	t_{WCR}	75	—	—	ns	
Write Command Pulse Width	t_{WP}	30	—	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	45	—	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	45	—	—	ns	
Data-in Set-up Time	t_{DS}	0	—	—	ns	9
Data-in Hold Time	t_{DH}	40	—	—	ns	9
Data-in Hold Time reference to $\overline{\text{RAS}}$	t_{DHR}	75	—	—	ns	
$\overline{\text{CAS}}$ Precharge Time (for page mode cycle only)	t_{CPP}	40	—	—	ns	
Refresh Period	t_{REF}	—	—	2	ns	
$\overline{\text{WE}}$ Command Set-up Time	t_{WCS}	−10	—	—	ns	10
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t_{CWD}	45	—	—	ns	10
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	t_{RWD}	80	—	—	ns	10
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	100	—	—	ns	

NOTES:

1. AC measurements assume t_T = 5ns.
2. V_{IHC}(min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
3. The specification for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range ($0°C + T_a \leqq 70°C$) is assured.
4. Assumes that $t_{RCD} \leqq t_{RCD}$ (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
5. Assumes that $t_{RCD} \geqq t_{RCD}$ (max).
6. Measured with a load equivalent to 2 TTL loads and 100pF.
7. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
8. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; If $t_{WCS} \geqq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geqq t_{CWD}$ (min) and $t_{RWD} \geqq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

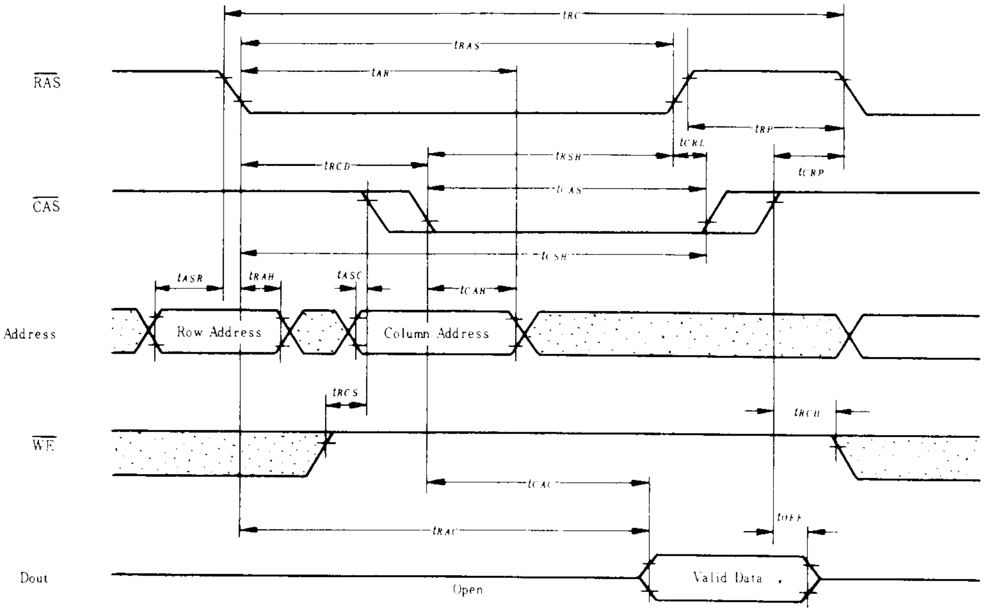
■ CAPACITANCE (Ta=0 to 70℃, V_{CC}=5.0V±10%)

Item	Symbol	min.	typ.	max.	Unit	Note
Input Capacitance (A_0 to A_6), Din	C_{I1}	—	4	6	pF	1
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}	—	5	7	pF	2
Output Capacitance (Dout)	C_O	—	5	7	pF	2, 3

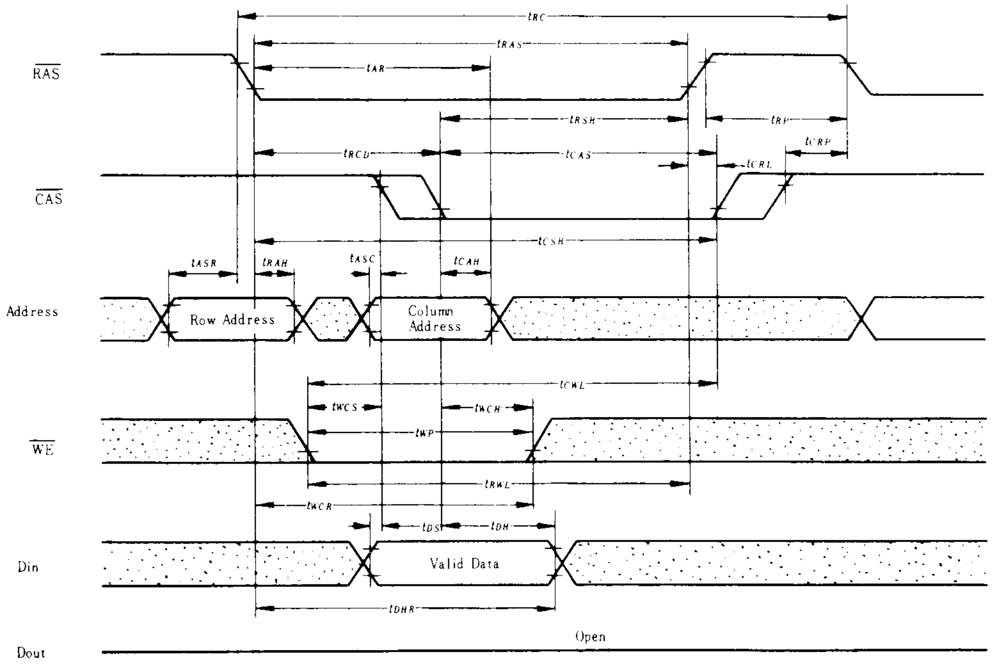
Notes: 1. Effective capacitance calculated from the equation $C = I \cdot \Delta t / \Delta V$ with ΔV = 3V and power supplies at nominal levels.

2. $\overline{CAS} = V_{IHC}$ to disable D_{OUT}.

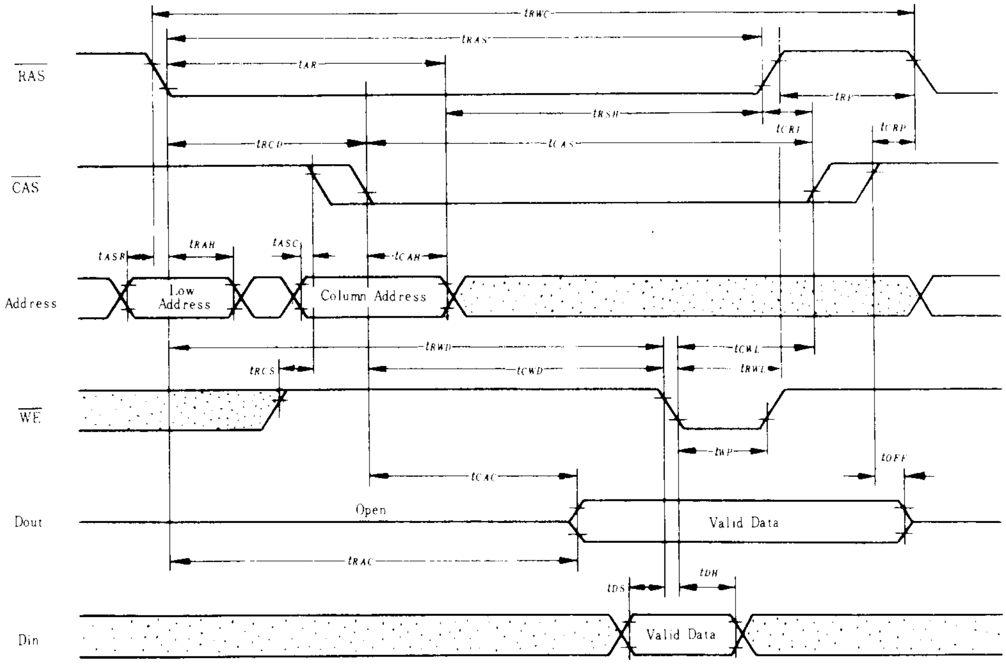
• READ CYCLE



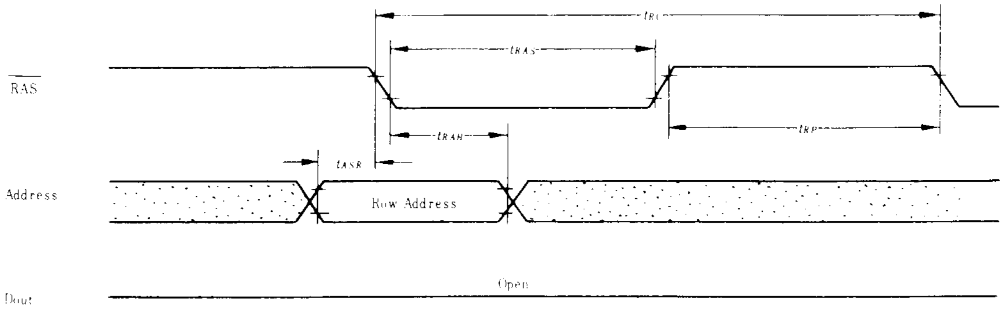
• WRITE CYCLE



● READ-WRITE/READ-MODIFY-WRITE CYCLE

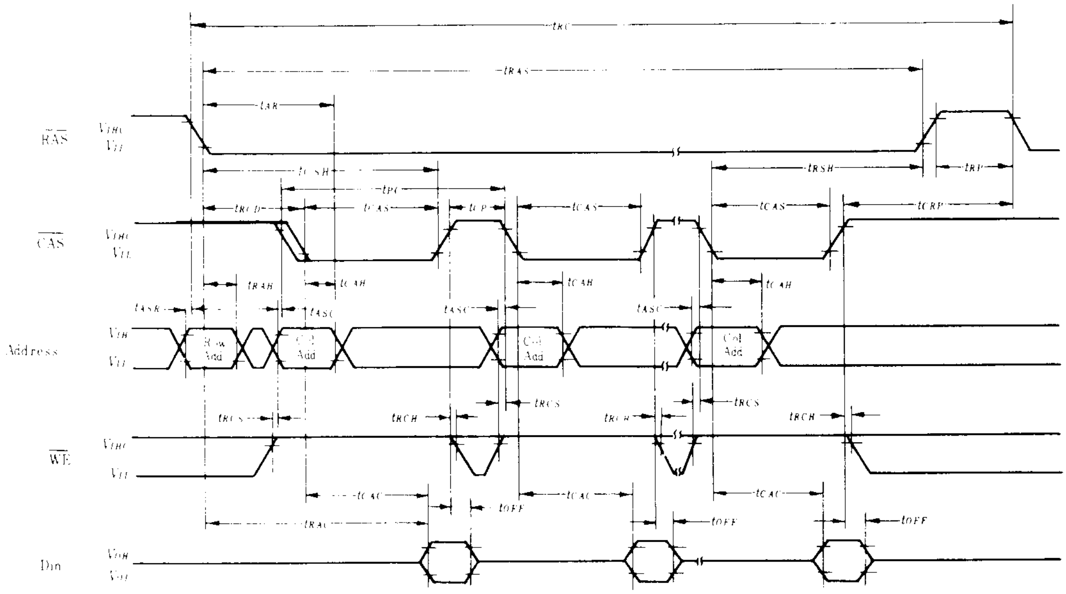


● RAS-ONLY" REFRESH CYCLE



Note: $\overline{CAS} = V_{IHC}$

• PAGE MODE READ CYCLE



• PAGE MODE WRITE CYCLE