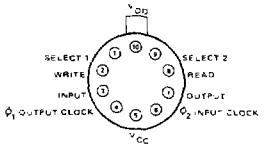
2505/1405-K

DESCRIPTION

The 2505/1405 512-bit recirculating dynamic shift registers consist of enhancement mode P-channel MOS devices integrated on a single monolithic chip. Internal recirculation logic plus write and read controls, together with two chip select controls are included on the chip.

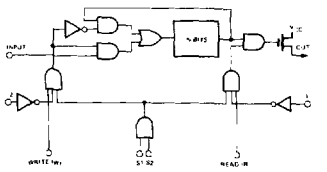
BLOCK DIAGRAM



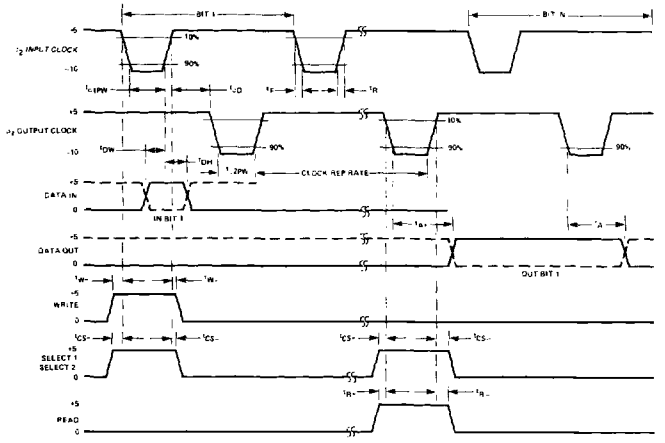
NOTES:
N = 512 '0' = OV, '1' = +5V.
When S1 or S2 is '0' Data Recirculates
When S1 and S2 are '1' see truth table

PIN CONFIGURATION

K PACKAGE



TIMING DIAGRAM



NOTE:
1. N=512
2. Note that the Read Input is AND'ed with $\overline{\Phi}_1$; therefore this function is not valid until Φ_1 occurs.

TRUTH TABLE

WRITE	READ	FUNCTION
0	0	Recirculate, Output is '0'
0	1	Recirculate, Output is Data
1	0	Write Mode, Output is '0'
1	1	Read/Write, Output is Data

MEMORIES