PBM 3936 Subscriber Line Audio-processing Circuit

Advance Information

Description

The Subscriber Line Audio-processing Circuit (SLAC) performs the coding, decoding and filtering functions necessary in digital voice switching machines. In this application, the SLAC processes voiceband analog signals into Pulse Code Modulated (PCM) outputs and processes PCM-inputs into analog outputs. The SLAC's performance is compatible with applicable AT&T and CCITT specifications. The device consists of three main sections: transmit processor, receive processor and control logic.

The transmit section contains an anti-aliasing filter, interpolative A/D converter and a digital signal processor. The analog signals received are converted and digitally processed to generate either 8-bit μ-law or A-law codes . Either one of two output ports may be selected for PCM data transmission.

The receive section contains a digital signal processor and a D/A converter. Either 8-bit μ-law codes or 8-bit A-law codes are received, processed and converted to analog signals. Either one of two input ports may be selected for reception of PCM data.

The control I/O provides a microprocessor-compatible serial interface and allows the user bidirectional access to many programmable features and capacity to completely control the operation of the device via a comprehensive set of 32 commands.

PBM 3936 is fully compatible with AMD SLAC AM7905 A.

The PBM 3936 package is 24-pin dual-in-line. Also available in a 32-pin leadless chip carrier.

Key Features

- Combination CODEC and Filter
- No trimming or adjustment required
- Uses digital signal processing
- Six user-programmable digital filters
- Dynamic Time Slot assignment
- Only 2 external components (non-precision)
- Dual PCM ports
- 4.096 MHz, 64-channel expanded mode operation
- Built-in test modes
- Microprocessor-compatible serial interface
- Control interface to SLIC
- Low standby power
- Selectable μ-law or A-law

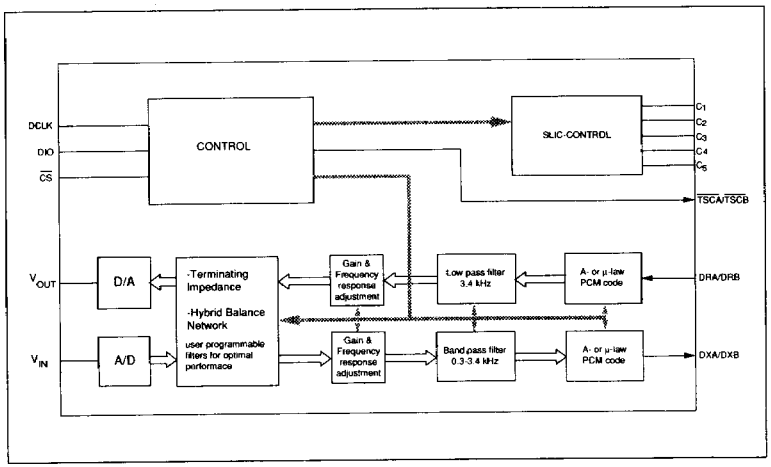
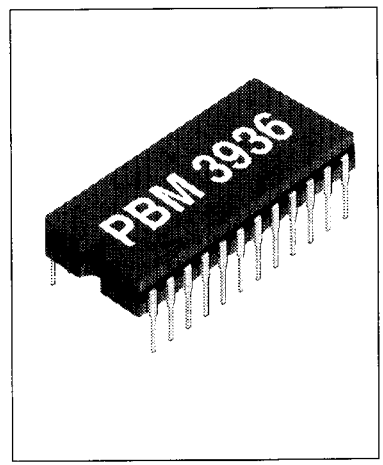


Figure 1. Functional diagram



Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Ambient temperature, under Bias	T_{Am}	0	25	70	°C
Case temperature	T_{Case}	0		85	°C
V_{CC} with respect to DGND	V_{CC}	-0.4	5	6	V
V_{BB} with respect to AGND	V_{BB}	-6.0	-5	0.4	V
V_{IN} with respect to AGND	V_{IN}	V_{BB}		V_{CC}	V

Pin Description

Refer to figure 2. (24-pin dual-in-line package)

DIP	Symbol	Description
1	V_{CC}	+5 V power supply
2	FS	Frame Sync. The Frame Sync pulse is an 8 kHz signal which identifies the beginning of a frame. The SLAC references individual time slots with respect to the frame sync pulse. The FS pulse must not be longer than 8 clock periods.
3	C_2	C_1 (pin 4), C_3 (pin 11), C_4 (pin 10 and C_5 (pin 12) are latched outputs. The serial interface may be used to write data to a register whose outputs are brought out to C_1-C_5. These 5 inputs/outputs are TTL-compatible and may be used to control the operation of a SLIC or any other device associated with the subscriber line.
4	C_1	Refer to pin 3 description.
5	V_{OUT}	Analog output. The received PCM data is digitally processed and converted to an analog signal at the V_{OUT} pin.
6	AGND	Analog ground.
7	V_{IN}	Analog input. The analog input is applied to the transmit path of the SLAC. The signal is sampled, digitally processed and encoded for the PCM output.
8	CAP 1	An external series resistor and capacitor are connected to pins 8 and 9. These components are part of the integrator in the A/D converter. The recommended values of these non-precision components are 1 kΩ ±5 % and 2 nF ±20 %.
9	CAP 2	Refer to pin 8 description.
10	C_4	Refer to pin 3 description.
11	C_3	Refer to pin 3 description.
12	C_5	Refer to pin 3 description.
13	DRA	PCM inputs. The receive PCM data is serially received from either the DRA or the DRB port. The port selection is under user program control. For μ-law and A-law 8 bits are received in 8-bit bursts every 125 μs at the MCLK rate.
14	DRB	Refer to pin 13 description.
15	DXB	PCM outputs. The transmit PCM data is serially fed to either the DXA or the DXB port. The port selection is under user program control. The output is available every 125 μs and the data is shifted out in 8-bit bursts at the MCLK rate. DXA and DXB are high impedance in between bursts and also in the stand-by mode.
16	DXA	Refer to pin 15 description.
17	$\overline{TSCA}$	Time slot control. The time slot control outputs are open drain outputs and are normally high. $\overline{TSCA}$ is low when PCM data is present on the DXA output and $\overline{TSCB}$ is low when PCM data is present on the DXB output.
18	$\overline{TSCB}$	Refer to pin 17 description.
19	DGND	Digital ground
20	DCLK	Data clock. The data clock shifts control data either into or out of the SLAC. The maximum clock rate is 2.048 MHz and the minimum clock rate is 2 kHz.

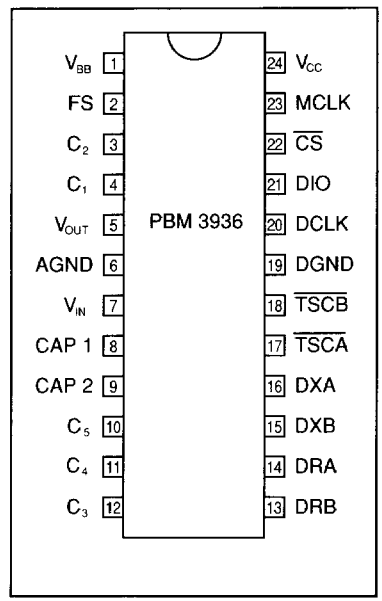


Figure 2. Pin description

DIP	Symbol	Description
21	DIO	Data input/output. Control data is serially written and read via the data input/output port. The input rate is determined by the data clock. DIO is high impedance when control data output is completed and CS is high.
22	$\overline{CS}$	Chip Select. A logic low at the Chip Select input enables the device to either input or output control data.
23	MCLK	Master clock. The master clock must be a 2.048 MHz +50 ppm or 4.096 MHz + 50 ppm clock input. If 4.096 MHz is used, the clock is divided internally (under command control) to all logic except the PCM transmit and receive logic. When 4.096 MHz is used, the first command after power on, must be to program it for operation with a 4.096 MHz clock.
24	V_{CC}	+5 V power supply

Functional Description

Refer to figure 3.

Introduction

The PBM 3936 SLAC performs the codec and filtering functions associated with the 4-wire section of the subscriber line circuitry in a digital switch. When used with e.g. any of Ericsson Components Subscriber Line Interface Circuit (SLIC), the pair provide a complete solution to the BORSCHT functions.

The SLAC contains auto-zeroed A/D and D/A converters. A microprocessor-compatible interface is provided to program the device into a variety of modes. These operating modes include, but are not limited to companded operation, dynamic time-slot assignment, and PCM-port-selection.

The SLAC samples the analog signal at the V_{IN} -pin and digitally processes it to produce a companded PCM code at the DXA or DXB output. Conversely, it receives companded PCM code at the DRA or DRB input and digitally processes it to produce an analog output at the V_{OUT} -pin. The processing is accomplished at the frame rate (8 kHz), and the digital output/input is available for transmission/reception every 125 µs.

Transmit Digital Signal Processor

In the transmit path, the analog signal is filtered, converted, compressed and made available for output.

The prefilter is an integrated anti-aliasing filter which prevents signals near the sample rate from folding back into the voiceband during decimation. The A/D is designed to have a wide dynamic range and excellent signal-to-noise performance. It uses a modified sigma delta loop with a D/A converter to track the input signal at a 512-kHz sampling rate.

The signal processor contains an ALU, RAM, ROM and control logic and implement the filter sections.

Transmit PCM Interface

The Transmit PCM Interface receives an 8-bit compressed code from the digital compressor. This code is loaded into the output register.

The Frame Sync (FS) pulse identifies the beginning of the Transmit frame and all channels (time slots) are referenced to it.

The PCM data may be user-programmed to be output via one of two ports, DXA or DXB.

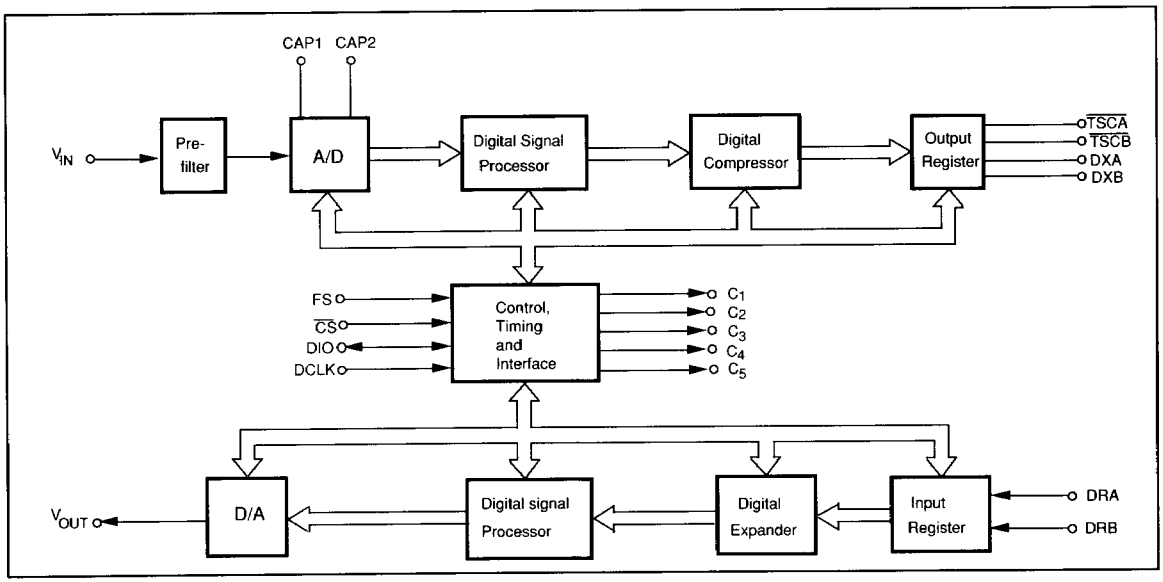


Figure 3. SLAC block diagram

Receive PCM Interface

The receive PCM interface logic controls the reception of data from the PCM highway and transfers it for expansion to the Receive Digital Signal Processor. The operation of this interface is identical to the Transmit section.

The Frame Sync (FS) pulse identifies the beginning of a Receive frame and all channels (time slots) are referenced to it.

The PCM data may be user-programmed to be input from one of two ports, DRA or DRB.

Receive Signal Processor

In the receive path the digital signal is expanded, filtered, converted to analog and output onto the V_{OUT} -pin.

Serial I/O Interface

A microprocessor may be used to program the SLAC and control its operation using the Serial I/O Interface. Additionally, data programmed previously may be read out for verification.

The interface consist of 3 pins, $\overline{CS}$, DCLK and DIO. The device is accessed by $\overline{CS}$ and data is serially written via DIO pin or read via DIO pin under control of DCLK.

Product information

This short form data sheet is made available to provide advance information. The product is under development.

Please contact our factory for availability information.

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