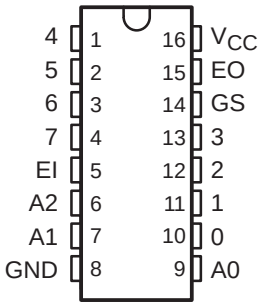
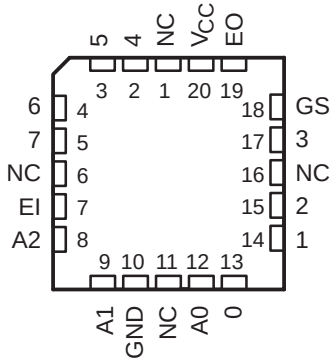
- **Encode Eight Data Lines to 3-Line Binary (Octal)**
- **Applications Include:**
  - **n-Bit Encoding**
  - **Code Converters and Generators**
- **Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs**

SN54HC148 . . . J OR W PACKAGE
SN74HC148 . . . D OR N PACKAGE
(TOP VIEW)



SN54HC148 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

description

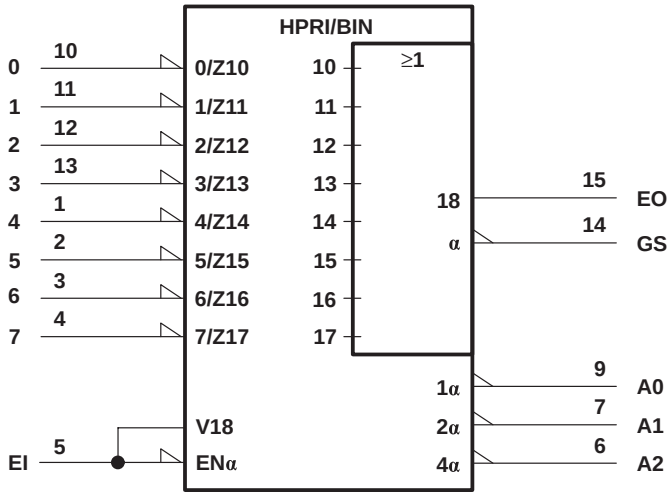
The ’HC148 feature priority decoding of the inputs to ensure that only the highest-order data line is encoded. These devices encode eight data lines to 3-line (4-2-1) binary (octal). Cascading circuitry (enable input EI and enable output EO) has been provided to allow octal expansion without the need for external circuitry. Data inputs and outputs are active at the low logic level.

The SN54HC148 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74HC148 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

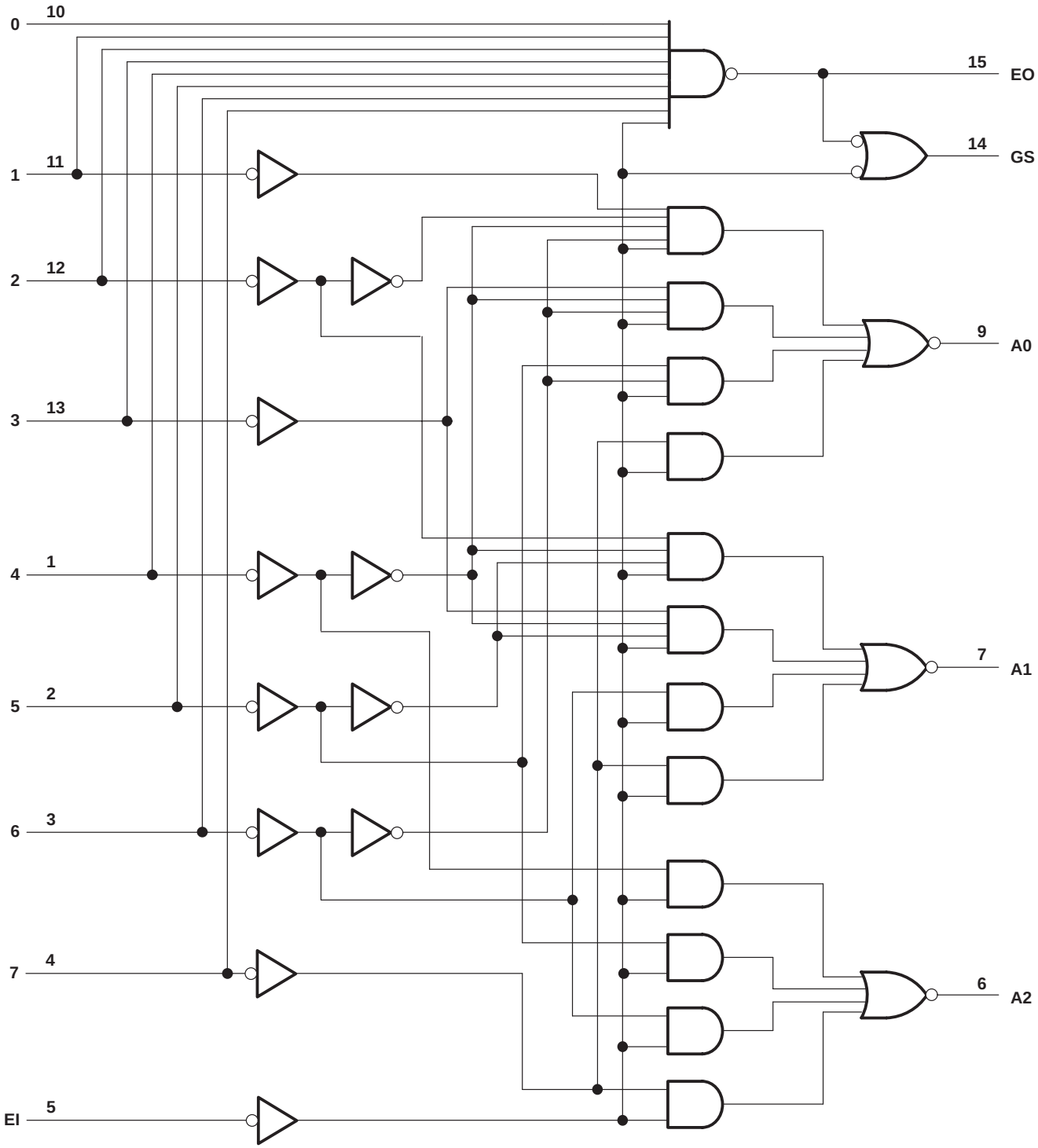
INPUTS									OUTPUTS				
EI	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**A2**	**A1**	**A0**	**GS**	**EO**
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, N, and W packages.

logic diagram (positive logic)



Pin numbers shown are for the D, J, N, and W packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) (see Note 1) . . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) (see Note 1) . . . . . ±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC}) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package . . . . . 113°C/W
N package . . . . . 78°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace length of zero.

recommended operating conditions

			SN54HC148			SN74HC148			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		2	5	6	2	5	6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5			1.5			V
		V_{CC} = 4.5 V	3.15			3.15			
		V_{CC} = 6 V	4.2			4.2			
V_{IL}	Low-level input voltage	V_{CC} = 2 V	0		0.5	0		0.5	V
		V_{CC} = 4.5 V	0		1.35	0		1.35	
		V_{CC} = 6 V	0		1.8	0		1.8	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0		1000	0		1000	ns
		V_{CC} = 4.5 V	0		500	0		500	
		V_{CC} = 6 V	0		400	0		400	
T_A	Operating free-air temperature		–55		125	–40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			SN54HC148		SN74HC148		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}	V_I = V_{IH} or V_{IL}	I_{OH} = –20 μA	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		I_{OH} = –4 mA	4.5 V	3.98	4.3		3.7		3.84		
		I_{OH} = –5.2 mA	6 V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} or V_{IL}	I_{OL} = 20 μA	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		I_{OL} = 4 mA	4.5 V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2 mA	6 V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} or 0		6 V			±0.1		±100		±1000	nA
I_{CC}	V_I = V_{CC} or 0,	I_O = 0	6 V			8		160		80	μA
C_i			2 V to 6 V		3	10		10		10	pF

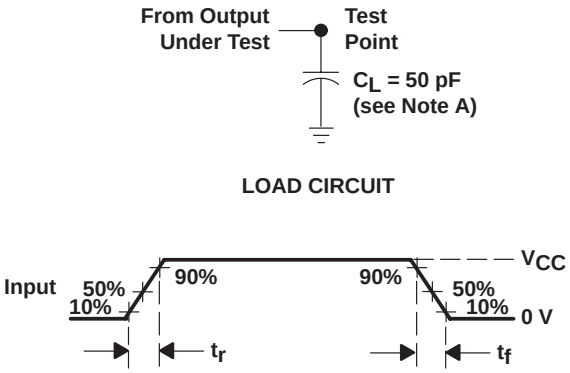
switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HC148		SN74HC148		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	1–7	A0, A1, or A2	2 V		69	180		270		225	ns
			4.5 V		23	36		54		45	
			6 V		21	31		46		38	
	0–7	EO	2 V		60	150		225		190	
			4.5 V		20	30		45		38	
			6 V		17	26		38		33	
		GS	2 V		75	190		285		240	
			4.5 V		25	38		57		48	
			6 V		21	32		48		41	
	EI	A0, A1, or A2	2 V		78	195		295		245	
			4.5 V		26	39		59		49	
			6 V		22	33		50		42	
		GS	2 V		57	145		220		180	
			4.5 V		19	29		44		36	
			6 V		16	25		38		31	
		EO	2 V		66	165		250		205	
			4.5 V		22	33		50		41	
			6 V		19	28		43		35	
t_t		Any	2 V		28	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

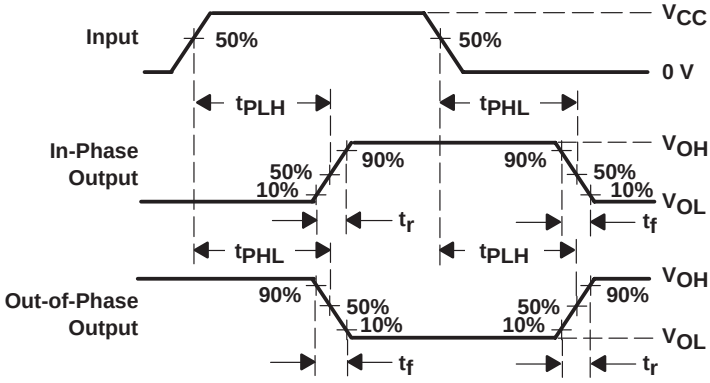
operating characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load	35	pF

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORM
INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
C. The outputs are measured one at a time with one input transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

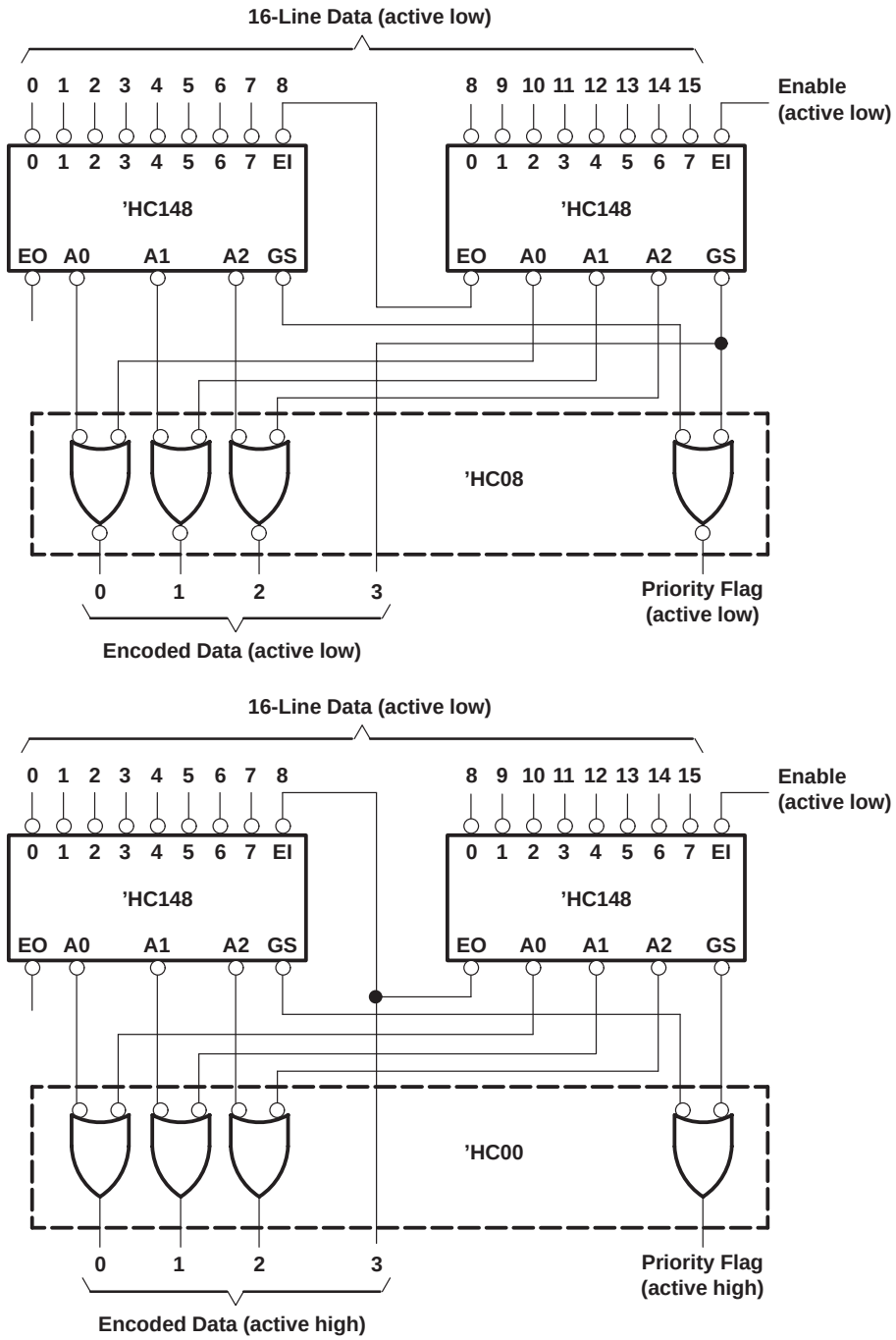


Figure 2. Priority Encoder for 16 Bits

Since the 'HC148 is a combinational logic circuit, wrong addresses can appear during input transients. Moreover, a change from high to low at EI can cause a transient low on GS when all inputs are high. This must be considered when strobing the outputs.

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SN74HC148, 8-Line To 3-Line Priority Encoders

DEVICE STATUS: **ACTIVE**

PARAMETER NAME	SN54HC148	SN74HC148
Voltage Nodes (V)	6, 5, 2	6, 5, 2
Vcc range (V)	2.0 to 6.0	2.0 to 6.0
Input Level	CMOS	CMOS
Output Level	CMOS	CMOS
Output Drive (mA)		-4/4
Output	2S	2S
From	8	8
To	3	3

FEATURES

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- Encode Eight Data Lines to 3-Line Binary (Octal)
- Applications Include:
  - n-Bit Encoding
  - Code Converters and Generators
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

DESCRIPTION

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TECHNICAL DOCUMENTS

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To view the following documents, Acrobat Reader 4.0 is required.
To download a document to your hard drive, right-click on the link and choose 'Save'.

DATASHEET

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Full datasheet in Acrobat PDF: sn74hc148.pdf (127 KB,Rev.D) (Updated: 05/01/1997)

APPLICATION NOTES

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View Application Notes for Digital Logic

- CMOS Power Consumption and CPD Calculation (Rev. B) (SCAA035B - Updated: 06/01/1997)
- Designing With Logic (Rev. C) (SDYA009C - Updated: 06/01/1997)
- Evaluation of Nickel/Palladium/Gold-Finished Surface-Mount Integrated Circuits (SZZA026 - Updated: 06/20/2001)

- Implications of Slow or Floating CMOS Inputs (Rev. C) (SCBA004C - Updated: 02/01/1998)
- Input and Output Characteristics of Digital Integrated Circuits (SDYA010 - Updated: 10/01/1996)
- Live Insertion (SDYA012 - Updated: 10/01/1996)
- SN54/74HCT CMOS Logic Family Applications and Restrictions (SCLA011 - Updated: 05/01/1996)
- Selecting the Right Texas Instruments Signal Switch (SZZA030 - Updated: 09/07/2001)
- Using High Speed CMOS and Advanced CMOS in Systems With Multiple Vcc (SCLA008 - Updated: 04/01/1996)

RELATED DOCUMENTS

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View Related Documentation for Digital Logic

- Logic Reference Guide (SCYB004, 1032 KB - Updated: 10/23/2001)
- Logic Selection Guide Second Half 2002 (Rev. R) (SDYU001R, 4274 KB - Updated: 07/19/2002)
- Military Semiconductors Selection Guide 2002 (Rev. B) (SGYC003B, 1648 KB - Updated: 04/22/2002)

SAMPLES

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ORDERABLE DEVICE	PACKAGE INDUSTRY (TI)	PINS	TEMP (°C)	STATUS	PRODUCT CONTENT	SAMPLES
SN74HC148D	SOP (D)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples
SN74HC148N	PDIP (N)	16	-40 TO 85	ACTIVE	View Product Content	Request Samples

PRICING/AVAILABILITY/PKG

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DEVICE INFORMATION							TI INVENTORY STATUS AS OF 3:00 PM GMT, 26 Sep 2002			REPORTED DISTRIBUTOR INVENTORY AS OF 3:00 PM GMT, 26 Sep 2002		
ORDERABLE DEVICE	STATUS	PACKAGE TYPE|PINS	TEMP (°C)	PRODUCT CONTENT	BUDGETARY PRICING QTY | $US	STD PACK QTY	IN STOCK	IN PROGRESS QTY|DATE	LEAD TIME	DISTRIBUTOR COMPANY|REGION	IN STOCK	PURCHASE
SN74HC148D	ACTIVE	SOP (D) | 16	-40 TO 85	View Contents	1KU | 0.45	40	19	3320 | 03 Oct	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								>10k | 10 Oct		DigiKey | AMERICA	>1k	BUY NOW
								>10k | 17 Oct				
SN74HC148DR	ACTIVE	SOP (D) | 16	-40 TO 85	View Contents	1KU | 0.80	2500	N/A*	7500 | 03 Oct	2 WKS			
								>10k | 07 Oct				
								>10k | 14 Oct				
SN74HC148DW	OBSOLETE	SOP (DW) | 16	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HC148DWR	OBSOLETE	SOP (DW) | 16	-40 TO 85	View Contents	1KU |		N/A*		Not Available			
SN74HC148N	ACTIVE	PDIP (N) | 16	-40 TO 85	View Contents	1KU | 0.45	25	N/A*	>10k | 23 Sep	2 WKS	Avnet | AMERICA	>1k	BUY NOW
								986 | 26 Sep		DigiKey | AMERICA	812	BUY NOW
								2575 | 03 Oct				

								>10k | 08 Oct						
								>10k | 15 Oct						
SN74HC148NSR	ACTIVE	SOP (NS) | 16		View Contents	1KU | 0.77	2000	N/A*	212 | 23 Sep	3 WKS					
								2302 | 11 Oct						
								>10k | 18 Oct						

Table Data Updated on: 9/26/2002