TRW

Image Manipulation Sequencer

40MHz

The TMC2302 is a high-speed self-sequencing VLSI circuit address generator which supports image resampling, rotation, rescaling, warping, and filtering. It generates input bit plane, interpolation coefficient lookup table, and output bit plane memory addresses along with pixel interpolator control signals.

Similar in architecture to the TRW TMC2301 Image Resampling Sequencer, the TMC2302 features numerous enhancements. In addition to an increase in the maximum clock rate to 40MHz, the device offers three-dimensional address generation and implements two-dimensional image transformation polynomials of up to third order.

The TMC2302 can process image data fields with up to 24 bits of binary resolution (2^{24} pixels) per dimension, with 0 to 16-bit subpixel resolution.

A system based on two TMC2302s can nearest-neighbor resample a two-dimensional 512 x 512 pixel image in 6.5 milliseconds, translating, rotating, or warping it, depending on the user-selected transformation parameters. A complete bilinear interpolation of the same image can be completed in 26 milliseconds, while a nearest-neighbor resampling of a 3D image 128 pixels on a side takes only 53 milliseconds with three TMC2302s. Image resampling speed is independent of angle of rotation, degree of warp, or amount of zoom specified.

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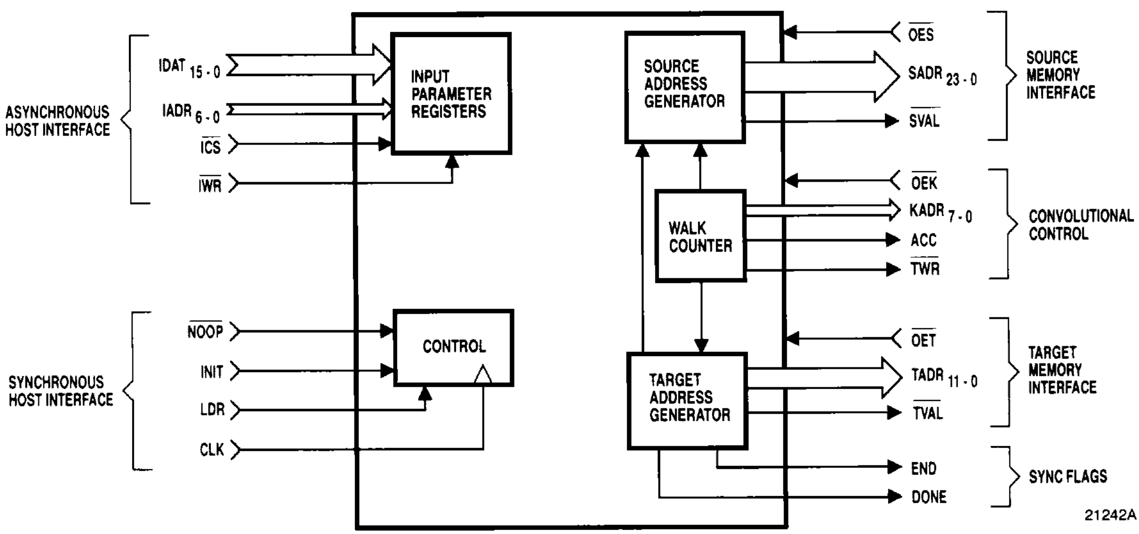
Simplified Block Diagram



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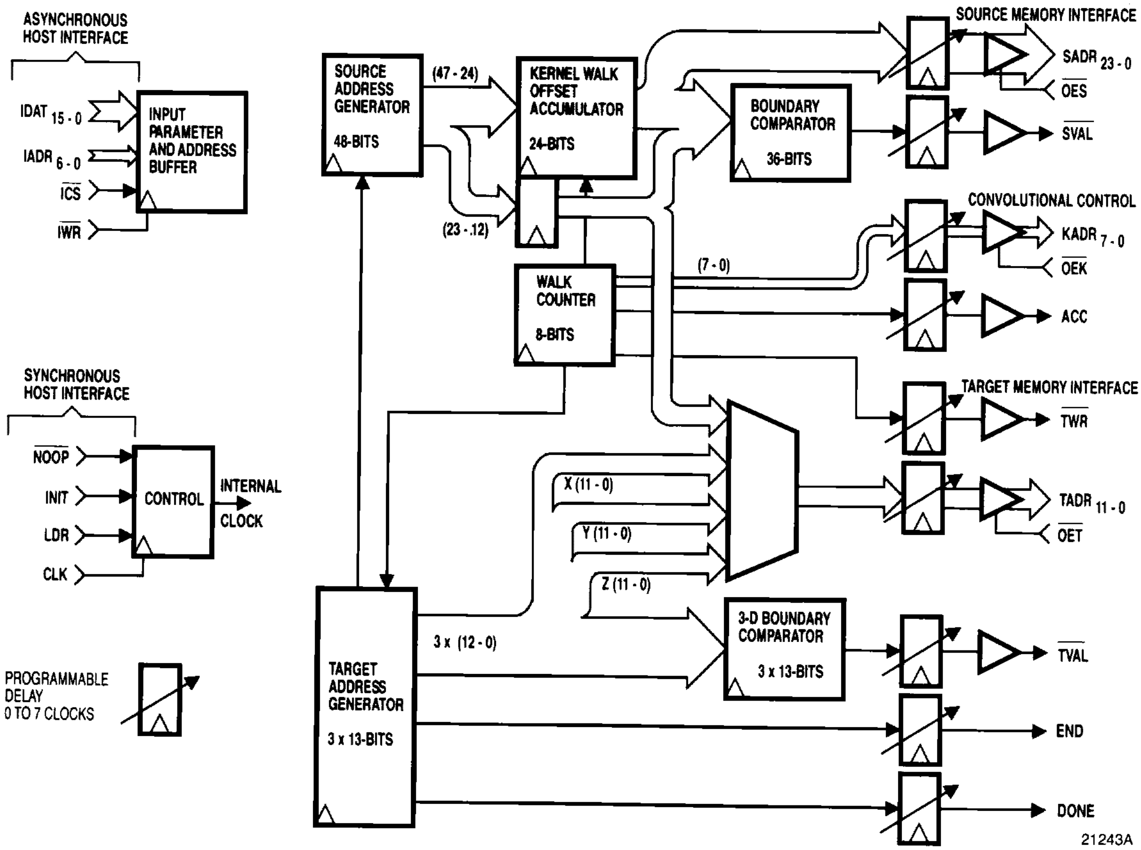
Features

- Asynchronous Loading Of Control Parameters
- Rapid (25ns Per Pixel) Rotation, Warping, Panning, And Scaling Of Images
- Three-Dimensional Image Addressing Capability
- General Third-Order Polynomial Transformations In Two Dimensions Implemented On-Chip; Three-Dimensional Transformation Of Up To Order 1.5 Also Supported
- Flexible, User-Configurable Pixel Datapath Timing Structure
- Static Convolutional Filtering Of Up To 16 x 16 Pixel (One-Pass), 256 x 256 Pixel (Two-Pass) Or 256 x 256 x 256 Pixel (Three-Pass) Windows
- User-Selectable Source Image Subpixel Resolution of 2^{-8} to 2^{-16}
- 24-Bit (Optional 36-Bit) Positioning Precision Within The Source Image Space, 48-Bit Internal Precision
- Low Power One-Micron OMICRON-C™ CMOS Process
- Available In A 120 Pin Plastic Pin Grid Array

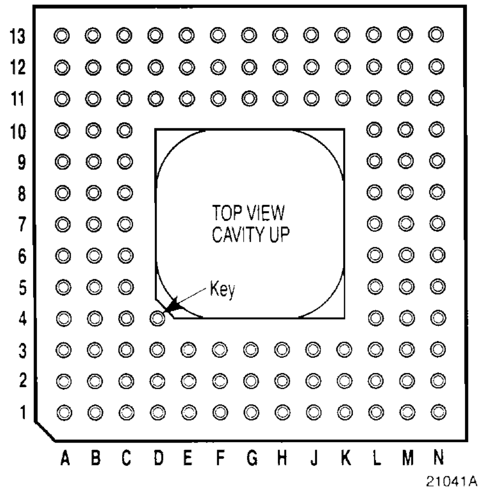
Applications

- High-Performance Video Special-Effects Generators
- Guidance Systems
- Image Recognition, Robotics
- High-Precision Image Registration (LANDSAT Processing)

Functional Block Diagram



Pin Assignments – 120 Pin Plastic Pin Grid Array, H5 Package



Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
C3	V_{DD}	G3	V_{DD}	L3	NC	L7	V_{DD}	L11	V_{DD}	G11	GND	C11	GND	C7	$IADR_5$
B2	$SADR_{15}$	G1	$SADR_6$	M2	$\overline{OEK}$	N7	$TADR_1$	M12	GND	G13	$IDAT_0$	B12	$IDAT_8$	A7	$IADR_6$
B1	$SADR_{14}$	H1	$SADR_5$	N2	$KADR_7$	N8	$TADR_2$	M13	$\overline{TVAL}$	F13	$IDAT_1$	A12	$IDAT_9$	A6	$\overline{OES}$
D3	GND	H2	$SADR_4$	L4	V_{DD}	M8	$TADR_3$	K11	V_{DD}	F12	GND	C10	$IDAT_{10}$	B6	$SADR_{23}$
C2	V_{DD}	H3	GND	M3	$KADR_6$	L8	$TADR_4$	L12	GND	F11	V_{DD}	B11	$IDAT_{11}$	C6	$SADR_{22}$
C1	$SADR_{13}$	J1	$SADR_3$	N3	$KADR_5$	N9	$TADR_5$	L13	$\overline{NOOP}$	E13	$IDAT_2$	A11	$IDAT_{12}$	A5	$SADR_{21}$
D2	$SADR_{12}$	J2	$SADR_2$	M4	$KADR_4$	M9	$TADR_6$	K12	INIT	E12	$IDAT_3$	B10	$IDAT_{13}$	B5	$SADR_{20}$
E3	GND	K1	$SADR_1$	L5	GND	N10	$TADR_7$	J11	V_{DD}	D13	$IDAT_4$	C9	$IDAT_{14}$	A4	V_{DD}
D1	$SADR_{11}$	J3	V_{DD}	N4	$KADR_3$	L9	$TADR_8$	K13	GND	E11	GND	A10	$IDAT_{15}$	C5	$SADR_{19}$
E2	$SADR_{10}$	K2	$SADR_0$	M5	$KADR_2$	M10	$TADR_9$	J12	CLK	D12	$IDAT_5$	B9	$\overline{ICS}$	B4	$SADR_{18}$
E1	$SADR_9$	L1	$\overline{SVAL}$	N5	$KADR_1$	N11	$TADR_{10}$	J13	$\overline{IWR}$	C13	$IDAT_6$	A9	$IADR_0$	A3	$SADR_{17}$
F3	V_{DD}	M1	ACC	L6	$KADR_0$	N12	$TADR_{11}$	H11	GND	B13	$IDAT_7$	C8	$IADR_1$	A2	$SADR_{16}$
F2	$SADR_8$	K3	GND	M6	$\overline{OET}$	L10	DONE	H12	V_{DD}	D11	V_{DD}	B8	$IADR_2$	C4	GND
F1	$SADR_7$	L2	V_{DD}	N6	$\overline{TWR}$	M11	GND	H13	SYNC	C12	GND	A8	$IADR_3$	B3	V_{DD}
G2	GND	N1	GND	M7	$TADR_0$	N13	ENDD	G12	V_{DD}	A13	V_{DD}	B7	$IADR_4$	A1	GND

Functional Description

General Information

The TMC2302 is a versatile, high-performance address generator which can control, under user direction, filtering or remapping of two or three-dimensional images by resampling them from one set of Cartesian coordinates (x, y, z) into a new, transformed set (u, v, w). Most applications utilize two identical devices for two-dimensional, or three devices for three-dimensional, image processing. The host CPU initializes the system by loading the input image buffer RAM with the source image pixel data and the TMC2302s with the image transformation and system configuration control parameters. These parameters are loaded by a separate, asynchronous input clock. The IMS-based system then executes the entire transformation as programmed, generating a DONE flag upon completion of the transform. The user can program the chip to repeat the transform continuously or to halt at the end.

General Information (cont.)

The IMSs continuously compute the target bit plane (u, v) or bit space addresses (u, v, w) in typical line-by-line, raster-scan serial sequence. For each output pixel address, they compute the corresponding remapped source image coordinates, each of whose upper 24 bits become the source bit plane addresses (x, y). An additional lower twelve bits are available through the target address port in the optional extended address mode. Source image addresses may be generated at up to 40MHz, with the corresponding target image addresses then appearing at up to (40/k)MHz, where "k" is the size of the interpolation kernel implemented. In the two-device system, one TMC2302 computes the horizontal coordinates x and u while the other generates the y and v (vertical) addresses. In a three-dimensional system, one additional device would provide the z and w (depth or time) coordinates.

To support a wide range of image transformations, the "row" or x/u device implements a 16-term polynomial of the form:

$$x = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3$$

where a through p are the user-defined image transformation parameters. The TMC2302 steps sequentially through the pixels within a user-defined rectangle in the target image space, computing the "old" source image address (x, y, z) corresponding to each "new" target image pixel (u, v, w). User-programmable flags are available to indicate when the source and target image addresses have fallen outside of a defined rectangular area, simplifying the generation of complex images or image windows.

In the three-dimensional mode, the x/u transformation equation is:

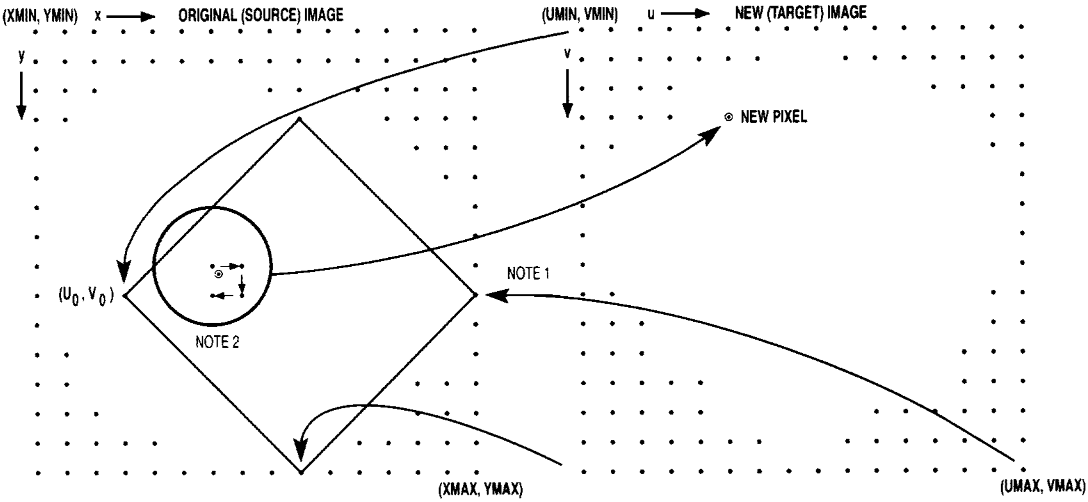
$$x = a + bu + ev + kw + fuv + ivw + luw + juvw$$

See "The Image Transformation Polynomial" section of the *Applications Discussion* .

The TMC2302 utilizes an external multiplier-accumulator or interpolator, connected to the system clock, to calculate the interpolated pixel value for each color. The products of the original source image pixel values surrounding the remapped pixel location (interpolation kernel) and the appropriate weights stored in the coefficient lookup table are summed. The resulting new interpolated image pixel value is then stored in the corresponding (U, V, W) memory location in the target image memory buffer. Next, the target image address is incremented by one in the "u" direction until UMAX is reached (end of line), when U is reset to UMIN, and the V counter is incremented to give the first pixel location in the next line. The process is repeated, proceeding line-by-line through the image, until VMAX is reached. In the case of three-dimensional images, the IMS system also steps through each page in the image, incrementing in the "w" direction with the completion of each image plane until WMAX is reached, and the transformation is complete.

The Image Manipulation Sequencer can support any nearest-neighbor, bilinear interpolation, or cubic convolution resampling, according to the user's requirements. Interpolation kernels of more than one pixel require an external interpolation coefficient lookup table and multiplier-accumulator. One, two, and three-pass algorithms are supported. For each output point in a typical two-dimensional single-pass static image filter, the TMC2302 implements a spiralling pixel resampling algorithm, "walking" around the resampling neighborhood in two dimensions and generating the appropriate coefficient table addresses to sum up the interpolated pixel value in the external pixel interpolator. At the end of each walk, the TMC2302 will advance one pixel along the output scan line and then execute the walk for that next pixel. When performing multiple-pass interpolation, the TMC2302 system proceeds along only one dimension per pass, which requires dimensionally separable, preferably orthogonal, coefficients.

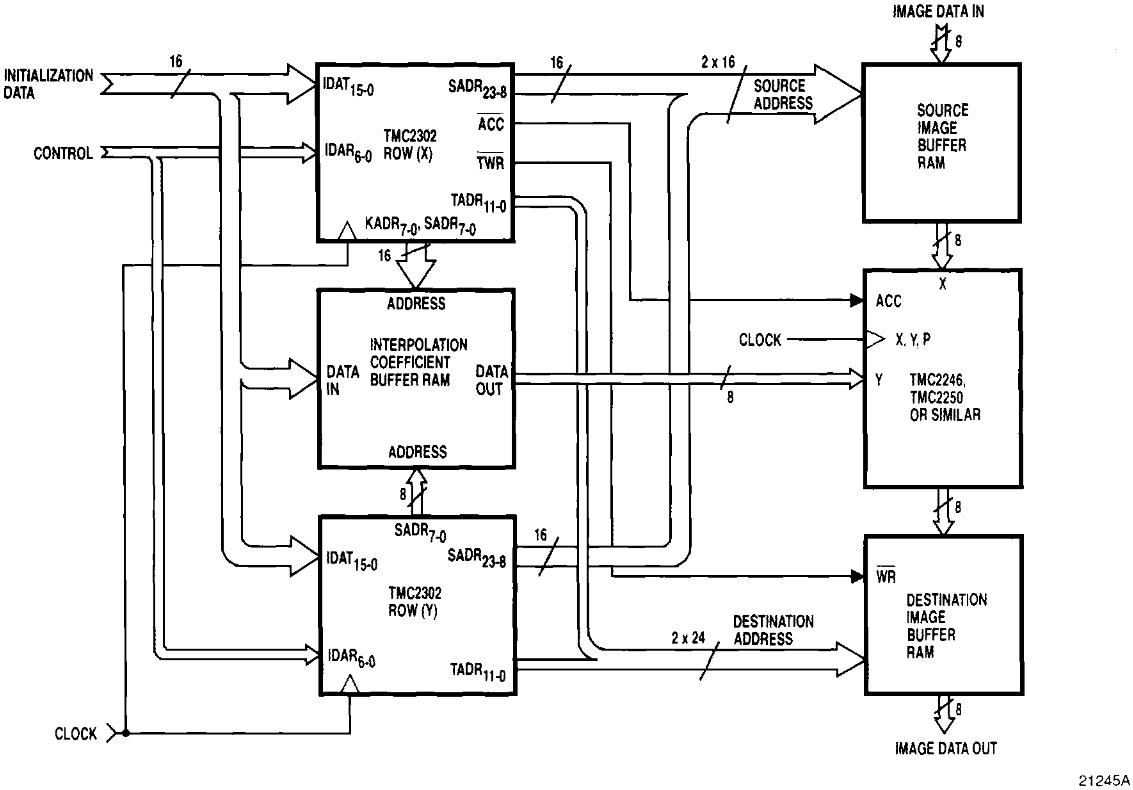
Figure 1. Image Resampling Geometry Showing Two-Dimensional Image Rotation and Expansion



NOTES: 1. Coordinate transformation U, V pixel mapped into X, Y coordinates. 2. Bilinear pixel interpolation walk. New U, V pixel intensity calculated from surrounding X, Y pixel neighborhood. 21244A

A basic, two-dimensional TMC2302-based system is shown in *Figure 2*. In this typical arrangement, two Image Manipulation Sequencers process the image. The only other components needed beyond the source and target image buffer memories are a multiplier-accumulator or pixel interpolator such as the TRW TMC2246 Image Mixer or TMC2250 Matrix Multiplier, and the Interpolation Coefficient Lookup Table RAM or ROM.

Figure 2. Basic Two-Dimensional Image Convolver Using TMC2302 IMS with Typical 8-Bit Data Path



Signal Definitions

Power

V_{DD}, GND — The TMC2302 operates from a single +5V supply. All pins must be connected.

Clock

CLK — The pixel clock of the TMC2302 strobes all internal registers except the control parameter preload registers. All timing specifications except those are referenced to the rising edge of CLK.

$\overline{IWR}$ — The internal image transformation and configuration control parameter registers are double buffered to simplify interfacing with system controllers. Depending on the state of the chip select $\overline{ICS}$, control words input to $IDAT_{15-0}$ and the corresponding input parameter register addresses presented to $IADR_{6-0}$ are strobed into the outer preolad registers on the rising edge of the Input parameter Write clock $\overline{IWR}$. See *Figure 3*.

Inputs

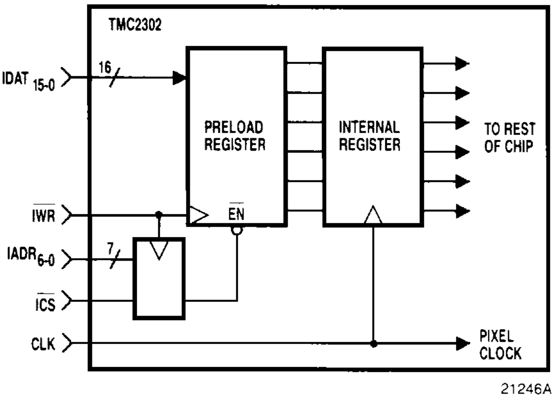
$IADR_{6-0}$ — The input parameter preload register currently indicated by the Input parameter register Address $IADR_{6-0}$ is loaded with the data presented to input port IDAT on the rising edge of $\overline{IWR}$, as demonstrated in *Figure 3*.

$IDAT_{15-0}$ — Configuration and transformation parameter Input Data is presented, along with the appropriate input register address word $IADR_{6-0}$, to the parameter Input Data port

Inputs (cont.)

$IDAT_{15-0}$ (cont.) $IDAT_{15-0}$ and is latched into the preload registers on the next rising edge of $\overline{IWR}$. Preload register updates are disabled by the chip select control $\overline{ICS}$. See *Figure 3*.

Figure 3. Image Transformation and Configuration Control Parameters Register Structure



Outputs

$SADR_{23-0}$ The 24-bit address of one dimension (X, Y, Z) of the source image pixel value currently being resampled is output through the Source Address port $SADR_{23-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OES}$.

$KADR_{7-0}$ The integer address steps for each dimension of the spiral interpolation walk performed by the TMC2302, as determined by the transform parameter KERNEL, are generated by the internal walk counter and output at the Coefficient Address output port $KADR_{7-0}$. This port can be forced to the high-impedance state by the enable control $\overline{OEK}$.

$TADR_{11-0}$ The 12-bit address of one dimension (U, V, W) of the target image pixel value just resampled is output through the Target Address Port $TADR_{11-0}$. This port is forced into the high-impedance state by the enable control $\overline{OET}$. $TADR_{11-0}$ can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by utilization of the pipeline delay parameter PIPTAD. For systems requiring greater spatial resolution in the source image than that offered by the $SADR_{23-0}$ alone, the Target Address Port can be reconfigured to output 12 additional LSBs of the source address by placing the device into the Extended mode, in which case the pipeline delay parameter must be set to 0 to maintain alignment with the current source address port output. See the *Device Configuration and Control Parameters* section.

Controls

$\overline{ICS}$ The input parameter preload register write clock $\overline{IWR}$, and thus the preloading of all configuration and transformation parameters, is disabled on the next clock when the registered Input parameter Chip Select input is HIGH. When $\overline{ICS}$ returns LOW, they are enabled on the next clock. See *Figure 3*.

INIT The TMC2302 control logic is cleared and initialized for the start of a new image transformation, and the internal working registers are updated with the contents of the current control parameter preload registers when the registered control input INIT is HIGH. The image transformation then commences with the first source image pixel address nine clocks later.

SYNC The user can select between continuous or one-frame operation with the registered input control SYNC. Assuming that INIT remains LOW and $\overline{NOOP}$ remains HIGH, if SYNC remains HIGH at the end of a transform the TMC2302 will begin the next image transformation without interruption. This assumes either that the user is not changing the parameter set, or that a new set of parameters has already been loaded into the preload registers midframe, prior to the beginning of the last line in the transform.

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Controls (cont.)

SYNC (cont.) If SYNC is LOW during the last clock cycle of a transform, the device will complete the image, having loaded the new transform parameter set during the first clock of the final line of the transform, and halt in the state set on the first clock cycle of the next transform. These outputs are held until SYNC is again brought HIGH, and operation resumes on the next clock. See *Figure 5*.

ACC The external pixel interpolator or multiplier-accumulator is initialized for a new accumulation of products by the registered Accumulator Control output ACC. On the first cycle of each interpolation walk, this output goes LOW for one cycle, effectively clearing the register by loading in only the first new resampled pixel value. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPACC. See the *Device Configuration and Control Parameters* section.

$\overline{\text{TWR}}$ On the last cycle of each interpolation walk, the Target Write Enable goes LOW for one clock cycle, returning HIGH for all but the last cycle of the next walk. When performing nearest-neighbor resampling, this control will remain LOW throughout the entire transform. This output can be forced to the high-impedance state by the enable control $\overline{\text{OET}}$, and can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPTWR. See the *Device Configuration and Control Parameters* section.

$\overline{\text{NOOP}}$ Assuming that INIT remains LOW, the internal system clock of the TMC2302 will be disabled on the next clock, halting the current transform, when the registered control input $\overline{\text{NOOP}}$ goes LOW. When $\overline{\text{NOOP}}$ returns HIGH, normal operation resumes on the next clock. This control does not affect the loading of the configuration and transformation parameter preload registers.

$\overline{\text{OES}}$ The source address port SADR$_{23\text{-}0}$ is enabled when the asynchronous output enable $\overline{\text{OES}}$ is LOW. When $\overline{\text{OES}}$ is HIGH, the port is in the high-impedance state.

$\overline{\text{OEK}}$ The interpolation coefficient address port KADR$_{7\text{-}0}$ is enabled when the asynchronous output enable $\overline{\text{OEK}}$ is LOW. When $\overline{\text{OEK}}$ is HIGH, the port is in the high-impedance state.

$\overline{\text{OET}}$ The target address port TADR$_{11\text{-}0}$ and target write enable $\overline{\text{TWR}}$ are enabled when the asynchronous Target Output Enable $\overline{\text{OET}}$ is LOW. When $\overline{\text{OET}}$ is HIGH, these outputs are in the high-impedance state. This control functions in both the normal and extended addressing modes.

Flags

$\overline{\text{SVAL}}$ When the current source image address component output is within the working space defined by the parameters XMIN and XMAX (or YMIN, YMAX for the column (Y/V) device or ZMIN, ZMAX for the page (Z/W) device), the Source Address Valid flag $\overline{\text{SVAL}}$ for that device is LOW. This flag will go HIGH on the clock in which the corresponding component address falls outside the defined region. In a typical system, the $\overline{\text{SVAL}}$ outputs of all IMS devices are OR'ed together to generate a global boundary violation flag. The user might then insert zeroes into the pixel interpolator to ignore that portion of the image outside the defined space, or insert a background color or image. This output can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPSVA. See the *Device Configuration and Control Parameters* section.

Flags (cont.)

$\overline{TVAL}$ — When the current target image addresses are within the working space defined by the parameters UMINI and UMAXI, and VMINI and VMAXI (and WMINI and WMAXI for systems processing three-dimensional images), the Target Address Valid flag $\overline{TVAL}$ for that device is LOW. This flag will go HIGH on the clock in which the current target address outputs fall outside the defined region. Since each TMC2302 device is programmed with distinct MINI/MAXI parameters and generates a separate $\overline{TVAL}$ flag, the user may define separate two or three-dimensional target space windows for each device. $\overline{TVAL}$ can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPTVA. See the ***Device Configuration and Control Parameters*** section.

ENDD — During the last pixel interpolation walk of a row (X/U device), the last row in a page (Y/V device), or the last page in a three-dimensional transform (Z/W device), the flag ENDD goes HIGH for the entire walk, indicating End of the transform in that dimension. It remains LOW otherwise. This output can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPEND. See the ***Device Configuration and Control Parameters*** section.

DONE — On the last clock cycle of the current image transform, the DONE flags on all TMC2302s go HIGH for one clock cycle. On the next clock cycle, all devices output the first addresses and control signals for the next image transform. If SYNC is LOW, the IMS system halts. If SYNC is HIGH, operation continues without interruption. See "SYNC," in the ***Controls*** section. This flag can be delayed up to seven clock cycles after the nominal sequence shown in *Table 1* by the pipeline delay parameter PIPDON. Also see "PFLS," in the ***Device Configuration and Control Parameters*** section.

Package Interconnections

Signal Type	Signal Name	Function	H5 Package Pins
Power	V_{DD}	Supply Voltage	C3, C2, F3, G3, J3, L2, L4, L7, L11, K11, J11, H12, G12, F11, D11, A13, A4, B3
	GND	Ground	D3, E3, G2, H3, K3, N1, L5, M11, M12, L12, K13, H11, G11, F12, E11, C12, C11, C4, A1
Clocks	CLK	System Clock	J12
	$\overline{IWR}$	Input Parameter Write Clock	J13
Inputs	$IDAT_{15-0}$	Input Parameter Data	A10, C9, B10, A11, B11, C10, A12, B12, B13, C13, D12, D13, E12, E13, F13, G13
	$IADR_{6-0}$	Input Parameter Address	A7, C7, B7, A8, B8, C8, A9
Outputs	$SADR_{23-0}$	Source Address	B6, C6, A5, B5, C5, B4, A3, A2, B2, B1, C1, D2, D1, E2, E1, F2, F1, G1, H1, H2, J1, J2, K1, K2
	$KADR_{7-0}$	Coefficient Address	N2, M3, N3, M4, N4, M5, N5, L6
	$TADR_{11-0}$	Target Address	N12, N11, M10, L9, N10, M9, N9, L8, M8, N8, N7, M7
Controls	INIT	Initialize	K12
	SYNC	Run/Halt	H13
	$\overline{ICS}$	Input Parameter Chip Select	B9
	ACC	Accumulate	M1
	$\overline{TWR}$	Target Memory Write Enable	N6
	$\overline{NOOP}$	No Operation	L13
	$\overline{OES}$	Source Address Output Enable	A6
	$\overline{OEK}$	Coefficient Address Output Enable	M2
	$\overline{OET}$	Target Address Output Enable	M6
Flags	$\overline{SVAL}$	Source Address Valid	L1
	$\overline{TVAL}$	Target Address Valid	M13
	ENDD	End of Dimension	N13
	DONE	Done	L10
No Connects	NC	No Connect	L3
		Index Pin	D4

Table 1. Nominal Output Signal Timing

$SADR_{23-0}$ [1]	ACC	$TADR_{11-0}$	$\overline{TWR}$	END	DONE
$X_{I-1,J,0}$	0	$U_{L-1,M}$	1	0	0
$X_{I-1,J,1}$	1	$U_{L-1,M}$	1	0	0
$X_{I-1,J,2}$	1	$U_{L-1,M}$	1	0	0
• • •					
$X_{I-1,J,K}$	1	$U_{L-1,M}$	0	1	0
$X_{I,J,0}$	0	$U_{L,M}$	1	1	0
$X_{I,J,1}$	1	$U_{L,M}$	1	1	0
$X_{I,J,2}$	1	$U_{L,M}$	1	1	0
• • •					
$X_{I,J,K}$	1	$U_{L,M}$	0	1	1

Note: 1. $KADR_{7-0}$ timing identical.

The nominal sequence of address and control signals of a two-dimensional, single-pass-programmed TMC2302 system, with all PIPE parameters set to 0, is shown in *Table 1*. Here, the values of the last two new target image pixels $U_{L-1,M}$ and $U_{L,M}$ are being calculated, and the beginning and end of the interpolation walks of length K which sample source image pixels in the neighborhod of locations ($X_{I-1,J}$, $X_{I,J}$) can be seen. Utilizing the arrival of the source image address ($SADR_{31-0}$) as a reference point, the other signals shown can be delayed up to seven clock cycles from the nominal timing shown here, allowing the user to configure these outputs to match the timing latencies of his pixel data path structure. Considerable speed and timing variations in image buffer memory, data register, and pixel interpolator structure can thus be accomodated, with minimal corresponding support hardware. Also see "PFLS," in the *Device Configuration and Control Parameters* section.

Transformation Coefficient and Configuration and Control Parameters

The TMC2302 is intended to act as a co-processor, requiring only that the user program the device to perform the image transformation desired by loading in the appropriate device configuration and transformation control parameters discussed in this section. The user then issues an "Init" command, allowing his system to run unattended until the completion of the image when a "Done" flag is generated to inform the host system.

The capabilities and flexibility of the TMC2302 Image Manipulation Sequencer are apparent when reviewing the following tables which define the transformation coefficient and configuration and control parameters. These tables are broken up into two separate groups. The first parameters discussed are the control words which select the dimension calculated, the functional configuration of each device, the working space in which they will operate, the size of the interpolation kernel desired, and the timing of the various address and control signals involved in handling the pixel data pipeline. The second parameters are the polynomial transform coefficients used in performing image manipulation. The TMC2302 utilizes three levels of internal 48-bit accumulators to calculate these values by forward difference accumulation, generating no significant cumulative spatial error for most applications. The user must be aware that all internal parameter and coefficient registers must be set by the user, including resetting after powerup any unused control words or coefficients.

A major difference between the TMC2302 and the TMC2301 is that elimination of the device interconnects. Instead, the user programs all X, U, V, and W boundaries into all TMC2302 devices. The system's progress through the image is monitored by each device independently and in parallel.

Transformation Coefficient and Configuration and Control Parameters (cont.)

The boundary values are usually identical in all devices in order to maintain synchronous operation.

As mentioned above, the TMC2302 also features user-programmable image data pipeline configuration controls. All output signals except the source and coefficient address outputs can be individually delayed by the user up to seven clocks after the nominal system timing illustrated in *Table 1*. This allows the user to software-configure the TMC2302s in his system to match his pixel interpolator, image buffer, and interpolation coefficient RAM structure timing.

The user can also program the device to continue into the next image for a set number of clock cycles after the Done flag has appeared. First, this "flushes" the final resampled pixel data word through the interpolation pipeline, all the way to the target image RAM. Also, valid pixel data will then appear on the first clock of the next transform independent of the length of the pixel pipeline, incurring no lost clock cycles.

Device Configuration and Control Parameters

UMIN, VMIN, WMIN	The memory addresses of the target image boundaries corresponding to the top, left side, and front page of the new image being generated are defined in all devices of the user's system by the parameters UMIN, VMIN, and WMIN, respectively. At the beginning of the transformation, the initial source image coordinate (X_0, Y_0, Z_0) will be mapped to this coordinate set. The numeric format assumed is 12-bit unsigned binary integer.
UMAX, VMAX, WMAX	The memory addresses of the target image boundaries corresponding to the bottom, right side, and last page of the image being generated are defined in all devices by the parameters UMAX, VMAX, and WMAX, respectively. These values should be greater than the UMIN/VMIN/WMIN values defined above. Numeric format assumed is unsigned 12-bit binary integer.

Note: The parameter UMAX must exceed UMIN so as to ensure that a minimum of 5 system clock cycles in two-dimensional operation, or 15 clock cycles in three-dimensional operation, pass between the periods in which these two target address values are generated. Thus in 2D nearest neighbor operation UMAX must be 5 greater than UMIN. In 2D bilinear interpolation mode (4-pixel two-dimensional kernel), the distance must be two pixels in the target image (actually enforcing a spacing of 8 system clocks).

UMINI, VMINI, WMINI	The target image addresses corresponding to those of the top, left side, and front page of the 2 or 3 dimensional region indicated by the valid target address flag $\overline{TVAL}$ are UMINI, VMINI, and WMINI, respectively. Thus, to define a valid region beginning at "m," the MINI parameter value is "m." These parameters are assumed to be in 12-bit unsigned binary integer format.
UMAXI, VMAXI, WMAXI	The target image addresses one more than those of the right side, bottom and back page of the region indicated by the valid target address flag $\overline{TVAL}$ are UMAXI, VMAXI, and WMAXI, respectively. Thus, to define a valid region ending at "n," the MAXI parameter value is "n+1". These parameters are assumed to be in 12-bit unsigned integer format.
XMIN, XMAX	The source image boundaries are defined for each device by the parameters XMIN and XMAX, in the case of the row device. The column device then contains YMIN and YMAX, and the page device (in systems performing three-dimensional operations) ZMIN and ZMAX. The value of XMAX should be greater than XMIN if the boundary violation flag $\overline{SVAL}$ is to operate correctly. These values are assumed to be in 32-bit unsigned binary integer format.
PFLS	The user can set the number of clock cycles that the TMC2302 continues in to the next image following the DONE flag, allowing his system to Flush all control and data pipeline paths and halt after a maximum of seven cycles. The numeric format assumed is three-bit unsigned binary integer.

Device Configuration and Control Parameters (cont.)

PTAD, PDON, PEND, PTVA, PSVA, PTWR, PACC As mentioned above, the control signals and target image pixel addresses generated by the TMC2302 can be delayed up to seven clock cycles after the nominal timing shown in *Table 1* by setting the appropriate Pipeline delay word. The numeric format assumed for all delay words is three-bit unsigned binary integer.

XTND When the user sets the control bit XTND to 1, the TMC2302 operates in an extended-resolution source address bus configuration. Assuming that the user has his own raster scan generator available elsewhere to manage the flow of output pixels from the TMC2302 system, the target address output bus $TADR_{11-0}$ is reconfigured internally into an extension of the source address bus, as $SADR_{11-0}$. The original source address bus $SADR_{23-0}$ is then $SADR_{35-12}$, providing 36 bits of spatial resolution in the source address space. An XTND of 0 puts the device in the standard 24-bit source, 12-bit target address configuration.

E3D Setting this control bit to 0 indicates a two-dimensional image transform is to be performed. When the E3D is set to 1, a three-dimensional image is assumed, using three TMC2302 devices.

DIM The user sets each TMC2302 to operate in a specific dimension as follows:

$DIM_{1,0}$	Dimension
00	X/U (Row) Device
01	Y/V (Column) Device
10	Z/W (Page) Device
11	No Operation

MODE In systems performing the standard two-dimensional spiral interpolation walk, MODE is set to 11, indicating single-pass operation. When performing multiple-pass resampling, the user must set this two-bit control word pass-by-pass in all IMSs, to implement each pass direction. For instance, setting MODE to 00 causes the TMC2302 system to increment only in the X-direction, holding the Y (and Z) addresses constant until the end of that pixel walk. On the next pass through the image, the user sets MODE=01, with the kernel increment in Y only. In 3D, the IMS system then proceeds again through the (U, V) target image space, walking kernels only along the Z direction.

$MODE_{1,0}$	Resampling Performed
00	X-Pass
01	Y-Pass
10	Z-Pass
11	Two-Dimension Spiral Walk

KERNEL This parameter determines the size of the interpolation walk performed. To implement a convolutional sum of K+1 pixels, the parameter KERNEL is set to K, up to a maximum of 255. In single-pass operation, this value must be identical in all devices, giving a square interpolation kernel. In multiple-pass operation, however, non-square kernels may be implemented, with different K values in each dimension. Or, the user could utilize a banded memory architecture in two-pass mode to access an entire row or column of a kernel in one clock, completing the entire sum in a single pass through the other dimension of the kernel. Numeric format is 8-bit unsigned integer.

FOV The user determines the size of each step in an interpolation walk, in terms of the number of source image pixels, by setting the Field Of View control. The binary weighting of the image transformation parameters and source address must be taken into account when determining this value. See *Table 6* and the *Applications Discussion* section. The numeric format assumed is unsigned 16-bit integer.

Table 2. Control Parameter Registers Binary Format (Row, Column or Page Device)

Name	Addr Hex	MSB (Format)															LSB	Limits Dec	Limits Hex
UMIN	30					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMAX	31					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMINI	32					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
UMAXI	33					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMIN	34					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMAX	35					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMINI	36					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
VMAXI	37					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMIN	38					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMAX	39					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMINI	3A					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
WMAXI	3B					2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	4095 0	FFF 000
XMINL	3C	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	00000000
XMINM	3D	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
XMAXL	3E	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	0	00000000
XMAXM	3F	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}	$2^{32}-1$	FFFFFFFF
PFLS	40		2^2	2^1	2^0													7 0	7 0
PTAD	40					2^2	2^1	2^0										7 0	7 0
PDON	40								2^2	2^1	2^0							7 0	7 0
PEND	40											2^2	2^1	2^0				7 0	7 0
PTVA	40														2^2	2^1	2^0	7 0	7 0
PSVA	41		2^2	2^1	2^0													7 0	7 0
PTWR	41					2^2	2^1	2^0										7 0	7 0

Note: Table 1 continues on the following page.

Table 2. Control Parameter Registers Binary Format (cont.)

Name	Addr Hex	MSB	Format														LSB	Limits Dec	Limits Hex
PACC	41								2^2	2^1	2^0							7 0	7 0
XTND	41											XTND							
E3D	41												E3D						
DIM	41													DIM_1	DIM_0				
MODE	41															$MODE_1$	$MODE_0$		
KERNEL	42									2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	255 0	FF 00
FOV	43	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^9	2^8	2^7	2^6	2^5	2^4	2^3	2^2	2^1	2^0	$2^{16}-1$ 0	FFFF 0000

Transformation Parameter Registers

The Transformation Parameter Word storage register addresses for the X/U device are listed in *Table 3*, along with the differential terms for each polynomial coefficient for both two and three-dimensional transforms. The polynomial terms for the other IMS device(s) are found by replacing every "X" in the table with a Y (or Z). A TMC2302-based system can perform image manipulations of up to third order in two dimensions, and three-dimensional transforms of up to order 1.5 ("first-and-a-half order"). Also, see "The Image Transformation Polynomial", in the *Applications Discussion* section.

The notation used to define each polynomial coefficient term in *Table 3* is easily interpreted. Each differential is of course defined by a differential in X, followed by the corresponding dependent U, V, or W terms. Thus,

DXUV is equivalent to $d^2X/dUdV$

and DXUUUV to d^4X/dU^3dV.

Table 3. Transformation Polynomial Coefficient Register Addresses

Name	Parameter: 2D Term	Parameter: 3D Term	Coefficient Word Addresses (hex): MSW	CSW	LSW
A	X_0	X_0	00	01	02
B	DXU	DXU	03	04	05
C	DXUU		06	07	08
D	DXUUU		09	0A	0B
E	DXV	DXV	0C	0D	0E
F	DXUV	DXUV	0F	10	11
G	DXUUV	X_0	12	13	14
H	DXUUUV	DXU	15	16	17
I	DXVV	DXVW	18	19	1A
J	DXUVV	DXUVW	1B	1C	1D
K	DXUUVV	DXW	1E	1F	20
L	DXUUUVV	DXUW	21	22	23
M	DXVVV		24	25	26
N	DXUVVV		27	28	29
O	DXUUVVV		2A	2B	2C
P	DXUUUVVV		2D	2E	2F

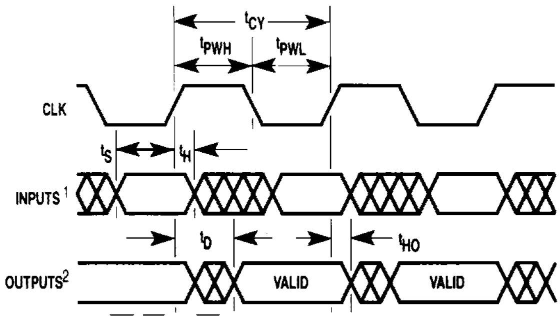
Note: The X_0 and DXU terms must each be loaded into two different registers when performing 3D transforms. Table 3 shows the binary weighting of all of the Transformation Parameter words, which are 48-bit signed fractional binary.

Table 4. Integer Binary Weighting of Transformation Parameters

	Format MSB															LSB	Limits Dec	Hex
MSW	-2^{47}	2^{46}	2^{45}	2^{44}	2^{43}	2^{42}	2^{41}	2^{40}	2^{39}	2^{38}	2^{37}	2^{36}	2^{35}	2^{34}	2^{33}	2^{32}	$2^{48}-1$	FFFFFFFFFFFF
CSW	2^{31}	2^{30}	2^{29}	2^{28}	2^{27}	2^{26}	2^{25}	2^{24}	2^{23}	2^{22}	2^{21}	2^{20}	2^{19}	2^{18}	2^{17}	2^{16}		
LSW	2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	0	000000000000

Note: A minus sign indicates a sign bit.

Figure 4a. Timing Diagram, Pixel Clock, Control, and Outputs



NOTES: 1. Except OES, OET, and OEK.
2. Assumes OES, OET, and OEK = LOW. All pipeline latency parameters set to 0.

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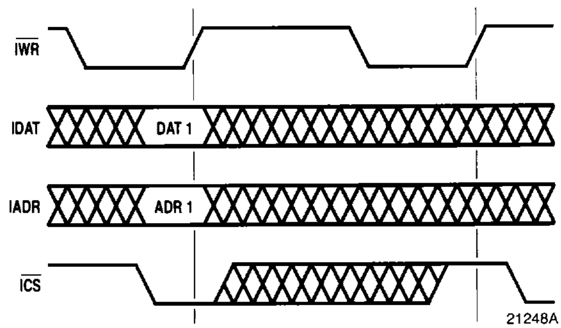
Figure 4b. Timing Diagram, Preload Parameters



Value "DAT 1" is loaded into address "ADR 1" on the first rising edge of IWR, since ICS = 0. Nothing happens on the second rising edge of IWR, when ICS = 1.

Figure 5. Equivalent Input Circuit

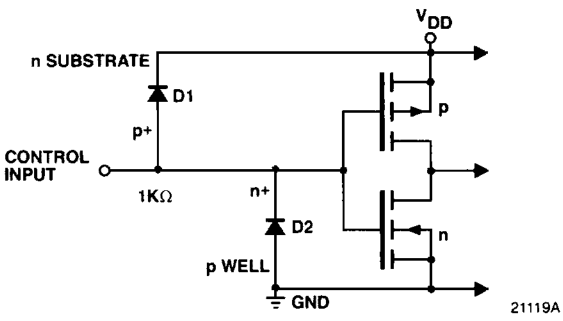


Figure 6. Equivalent Output Circuit

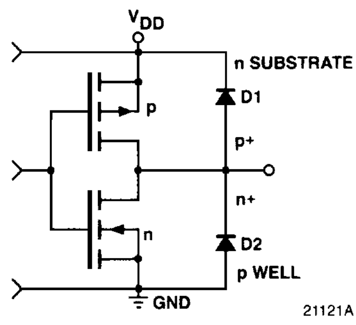
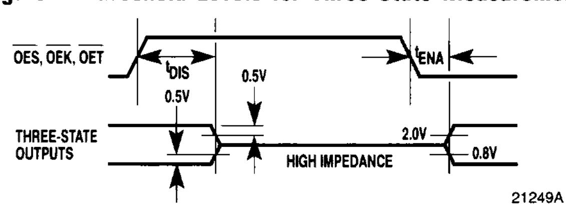


Figure 7. Threshold Levels for Three-State Measurements



Absolute maximum ratings (beyond which the device may be damaged)[1]

Supply Voltage	−0.5 to +7.0V
Input Voltage	−0.5 to (V_{DD}+0.5)V
Output	
Applied voltage[2]	−0.5 to (V_{DD}+0.5)V
Short-circuit duration (single output in HIGH state to ground)	1 Second
Temperature	
Operating, case	−60 to +130°C
junction	175°C
Lead, soldering (10 seconds)	300°C
Storage	−65 to +150°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.

Operating conditions

			Temperature Range						
			Standard			−1			
Parameter		Test Conditions	Min	Nom	Max	Min	Nom	Max	Units
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IL}	Input Voltage, Logic LOW				0.8			0.8	V
V_{IH}	Input Voltage, Logic HIGH		2.0			2.0			V
I_{OL}	Output Current, Logic LOW				8.0			8.0	mA
I_{OH}	Output Current, Logic HIGH				−4.0			−4.0	mA
t_{CY}	Cycle Time	V_{DD}=Min	33			25			ns
t_{PWL}	Clock Pulse Width, LOW	V_{DD}=Min	15			12.5			ns
t_{PWH}	Clock Pulse Width, HIGH	V_{DD}=Min	15			10			ns
t_S	Input Setup Time		10			8			ns
t_H	Input Hold Time		2			2			ns
T_A	Ambient Temperature, Still Air		0		70	0		70	°C

Electrical characteristics within specified operating conditions [1]

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	-1 Min	-1 Max	Units
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = 0V		10		10	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, f = 20MHz, $\overline{OES} = \overline{OEK} = \overline{OET}$ = 5V		70		70	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = 0V	−10		−10		µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, $V_{IN} = V_{DD}$		10		10	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min, I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = 0V	−40		−40		µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, $V_{IN} = V_{DD}$		40		40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max.	−20	−70	−20	−70	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_O	Output Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note: 1. Actual test conditions may vary from those shown, but guarantee operation as specified.

Switching characteristics within specified operating conditions

Parameter		Test Conditions	Temperature Range Standard Min	Standard Max	-1 Min	-1 Max	Units
t_{DO}	Output Delay	V_{DD} = Min, C_{LOAD} = 25pF		15		12	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 25pF	4		4		ns
t_{ENA}	Three-State Output Enable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		12		12	ns
t_{DIS}	Three-State Output Disable Delay [1]	V_{DD} = Min, C_{LOAD} = 25pF		15		15	ns

Note: 1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Applications Discussion

The Image Transformation Polynomial

On any given clock cycle, when performing a two-dimensional geometric transformation the addresses output by the row (X/U) TMC2302 are generated by forward difference accumulation according to the following third-order polynomial:

$$x(u,v) = a + bu + cu^2 + du^3 + ev + fvu + gvu^2 + hvu^3 + iv^2 + jv^2u + kv^2u^2 + lv^2u^3 + mv^3 + nv^3u + ov^3u^2 + pv^3u^3 + FOV \bullet CAX(ca) + FOV \bullet u \bullet CAX(Ker)$$

The polynomial utilized for three-dimensional transforms is:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw + FOV \bullet CAX(ca) + FOV \bullet u \bullet CAX(Ker),$$

where UMIN ≤ u ≤ UMAX, VMIN ≤ v ≤ VMAX, WMIN ≤ w ≤ WMAX, and the polynomials for the column or page devices are obtained by replacing the x by a y or z, as appropriate.

The Image Transformation Polynomial (cont.)

FOV is the 16-bit field-of-view parameter, normally set so that the spiral walk proceeds in single-pixel steps. FOV can be increased to expand the step size and thus the spiral walk, subsampling the image. See *Table 2* and *Table 6*. Also, CAX(ca) is the current value of the coefficient address, and CAX(Ker) is the terminal value of each pixel walk in that dimension. See the *Interpolation Coefficient Lookup Table Addressing*. The CAX(Ker) term arises because the IRS computes each new walk's starting point from the previous spiral walk's end point, rather than its starting point.

We can reform the two-dimensional polynomial as:

$$x(u,v) = (a + ev + iv^2 + mv^3) + (b + fv + jv^2 + nv^3)u + (c + gv + kv^2 + ov^3)u^2 + (d + hv + lv^2 + pv^3)u^3,$$

and retain the simpler three-dimensional form:

$$x(u,v,w) = a + bu + ev + kw + fuv + ivw + luw + juvw$$

and define each of the polynomial coefficients in arithmetic terms, as shown in *Table 5*.

Table 5. Transformation Polynomial Coefficients

Name	Parameter: Two-Dimensional Term	Two-Dimensional Coefficient	Three-Dimensional Term	Three-Dimensional Coefficient
A	X_0	a	X_0	a
B	DXU	b+c+d	DXU	b
C	DXUU	2c+6d	—	0
D	DXUUU	6d	—	0
E	DXV	e+i+m	DXV	e
F	DXUV	f+g+h+j+k+l+n+o+p	DXUV	f
G	DXUUV	2(g+k+o)+6(h+l+p)	X_0	a
H	DXUUUV	6(h+l+p)	DXU	b
I	DXVV	2i+6m	DXVW	i
J	DXUVV	2(j+k+l)+6(n+o+p)	DXUVW	j
K	DXUUVV	4k+12l+12o+36p	DXW	k
L	DXUUUVV	12l+36p	DXUW	l
M	DXVVV	6m	—	0
N	DXUVVV	6(n+o+p)	—	0
O	DXUUVVV	12o+36p	—	0
P	DXUUUVVV	36p	—	0

Understanding The Polynomial Coefficients An Overview

As the formulae indicate, the source address is a polynomial function of the two (or three) dimensions of the target address. Each of the 16 terms of the equation is of the form:

$$\frac{d^{m+n+p}x}{du^m\, dv^n\, dw^p},$$

and may be treated approximately as a mixed partial difference of order m, n, and p.

The simplest term, X_0, is a zeroeth (non-) function of the target addresses; it specifies the source address point corresponding to the upper left point in the target space.

The next-simplest terms, dX/dU and dY/dV, govern the relative scales of the source and target images, i.e., how large a step in source space corresponds to a unit step in the corresponding direction in the target space. As long as the cross-terms, dX/dV and dY/dU, are zero, this is a straight scale operation, without rotation or shear.

Understanding the Polynomial Coefficients (cont.)

The first-order cross terms, dX/dV and dY/dU, generate source space displacements perpendicular to unit displacements in the target space, thereby causing shearing of the image. In conjunction with the parallel source terms described above, they govern rotation, shear, and scaling of the image.

Although the actions of the higher-order terms become progressively difficult to describe, all terms behave essentially as partial differences of various orders, and a little thought and common sense will generally lead the user to the proper conclusions. For example, the term dXUU (using the notation of *Table 3*) is a horizontal scale factor which increases as one progresses across each row, causing a quadratic horizontal warp. In fact, all terms of the form dmX/dUm or dnY/dVn cause only stretching of the image, never rotation.

Interpolation Coefficient Lookup Table Addressing

The external coefficient lookup table RAM stores the interpolation coefficient values used to calculate the value of the new pixel. These values are selected by the user, allowing maximum filtering flexibility. In simple filtering applications, the source and target pixel addresses map one-to-one, and only one interpolation coefficient set is required. These integer addresses are generated for each dimension by the internal walk counters of each TMC2302.

However, applications performing a coordinate transformation will almost always generate non-integer source pixel addresses; that is, the U (or V) locations will not map to the X (or Y) addresses exactly, and fractional source address components are generated. The user must then expand the interpolation coefficient lookup table to include spatially-corrected values, as determined by the subpixel resolution of the system.

The TMC2301 Image Resampling Sequencer allows the user to trade subpixel resolution against interpolation step size by obtaining the interpolation coefficient addresses directly from the fractional part of the source address. The TMC2302 gives the user 16 different interpolation bit weighting positions. The complete Interpolation Coefficient Address for that dimension then consists of both the 8-bit interpolation walk address $KADR_{7-0}$, weighted to match the source address binary point by the parameter FOV, and the fractional portion of the source pixel address $SADR_{23-0}$, to the desired subpixel resolution. See *Table 6*.

Internal and External Data Formats

The source address value output by the TMC2302 is a 24-bit two's complement number, with binary point assignable by the user anywhere in the 16 lower bits. The Extended mode appends 12 additional fractional bits for greater output precision. All internal computations include these 24 plus 12 bits, plus an additional 12 lower bits, for 48-bit precision. See *Table 6*.

Internally, each TMC2302's source address (X, Y, or Z) generator computes a 48-bit address through a mode-specific accumulation of the sixteen 48-bit user-specified resampling parameters. The 24 most significant bits of the final accumulation emerge via the source address port, whereas the "extend" mode makes the 12 next-most-significant bits available at the target address port. The 12 least significant bits are truncated internally.

Source Address Bit Weighting and Setting the Binary Point

When performing nearest-neighbor resampling, the user may arbitrarily trade source image size against subpixel resolution merely by adhering to a single binary point position for all resampling parameters. For example, if the binary point follows the 16 most significant bits in each resampling parameter, then it will appear following the source address' 16 most significant bits, leaving 8 (20 in extended mode) bits of subpixel resolution.

In any filtering or resampling operation performing an interpolation walk, the user should set the Field of View (FOV) parameter according to the desired binary point position determined above, as follows. To provide 2^{24} integral pixel positions per dimension, with no subpixel resolution, set FOV=0001 (hex). For 2^{23} positions with 1-bit (0.5) subpixel resolution, FOV=0010 (hex). Similarly, for 2^9 positions and 15-bit subpixel resolution, FOV=8000 (hex). As shown in *Table 6*, using the parameter FOV the user effectively "shifts" the bit weight of the coefficient address word $KADR_{7-0}$ to match the established location of his source address binary point. In each case, the EXTEND mode provides 12 additional bits of subpixel resolution but eliminates the separate target or raster address, which must then be generated elsewhere in the user's system.

Table 6. Relative Bit Weighting – Source Address

Word \ Weight	2^{47} 2^{46} ... 2^{40}	2^{39} 2^{32}	2^{31} ... 2^{25} 2^{24}	2^{23} ... 2^{16}	2^{15} ... 2^{12} ... 2^{8}	2^{7} ... 2^{0}
Transform Parameters	−47 46					0
Internal Source Address Generator	−47 46					0
Source Address Output $SADR_{23-0}$	−23 22 ... 16	15 8	7 ... 1 0			
Extended Mode Only $TADR_{11-0}$				11 ... 4	3 ... 0	
$KADR_{7-0}$						
FOV = 0001			2^7 ... ... 2^0			
FOV = 0002		2^7	2^6 ... 2^0			
• • •						
FOV = 8000	2^7 ... 2^1	2^0				

Note: A minus sign indicates a sign bit.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$

As mentioned above, the TMC2302 provides two programmable valid address, or boundary flags. The source valid flag $\overline{SVAL}$ is asserted when the current source image address output for that device's source image dimension is within the space defined by the configuration parameters XMIN and XMAX, or YMIN and YMAX, or ZMIN and ZMAX, as appropriate. Also, the target valid flag $\overline{TVAL}$ is available to indicate when the current target image address values fall within the space defined by the configuration parameters UMINI, UMAXI, VMINI, VMAXI, and also WMINI and WMAXI in three-dimensional systems. Note that all of these parameters are each programmed into each individual TMC2302. Thus, the user could define two (or three) different working spaces, one indicated by each IMS device.

Figure 8 may help clarify the relationships among (X_0, Y_0, Z_0), (UMIN, VMIN, WMIN), and (UMAX, VMAX, WMAX), for the two-dimensional case. With positive first derivatives, (X_0, Y_0) and (UMIN, VMIN) represent the upper left corners of the original image and the new destination field, respectively. The lower right corner of the new transformed image is located at (UMAX, VMAX); the location of the corresponding corner of the original image depends on the values of the derivatives.

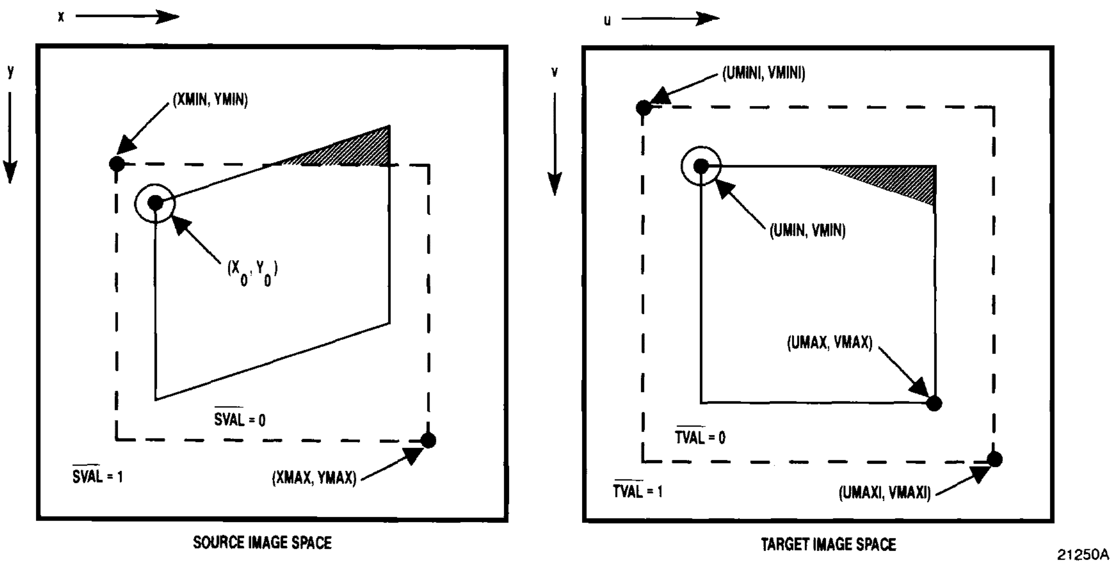
Not to be confused with (X_0, Y_0), the points (XMIN, YMIN) and (XMAX, YMAX) define the "usable" rectangular portion of the original image which is indicated by the valid address flag $\overline{SVAL}$; points (X, Y) lying outside this region are ignored in most resampling and filtering applications. Specifically, the point (X_0, Y_0) is the location from which the TMC2302 system begins the image resampling sequence. Every step beyond that point in the source image space is defined by the address generators implementing the image transformation polynomials.

The valid source address flag feature permits one to construct a mosaic of several abutting subimages in the (X, Y) plane, without danger of edge effect interference between adjacent subimages. Note in the figure that the upper right corner of the resampled source image lies outside the admissible region; in practice, the values fetched at these locations will not be included in the convolutional sums. One might, for instance, program these boundary values to alert the system that an edge is being approached and to modify the interpolation coefficients appropriately, or simply to ignore pixel values outside the defined space.

Utilization of the Image Boundary Flags $\overline{SVAL}$ and $\overline{TVAL}$ (cont.)

The flag $\overline{TVAL}$ however is utilized somewhat differently. Working in unison with the target address working space defined by UMIN/UMAX, etc, the target address valid flag could be programmed to delineate image areas other than the immediate working space, and the flag of each TMC2302 to indicate unique regions anywhere within the target image. With this flexibility, the user can generate windows, composite multiple images, or simply switch to a background image or border color.

Figure 8. Pixel Maps Demonstrating Source and Destination Image Boundaries, Violation Flags, and Image Clipping (Note Shaded Areas)



Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2302H5C [1]	STD – T_A = 0°C to 70°C	Commercial, 30MHz	120 Pin Plastic PGA	2302H5C
TMC2302H5C1 [1]	STD – T_A = 0°C to 70°C	Commercial, 40MHz	120 Pin Plastic PGA	2302H5C1

Note: 1. Consult factory for availability.

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