

9097248 TOSHIBA (LOGIC/MEMORY)

CCD DRIVER
(Si-Monolithic)

T3854

67C 09607

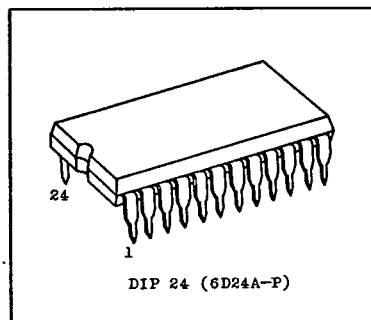
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T-41-55

T3854 is a clock driver for TDC201C (CCD Area Image Sensor) with all drive outputs inclusive.

FEATURES:

- . CMOS Device
- . Low Power Dissipation
- . +8V Single Supply Operation
- . On-chip DC Bias Circuit
- . On-chip Blanking Pulse and Pulse Generator
- Capable of TTL Interface by External Resistor.

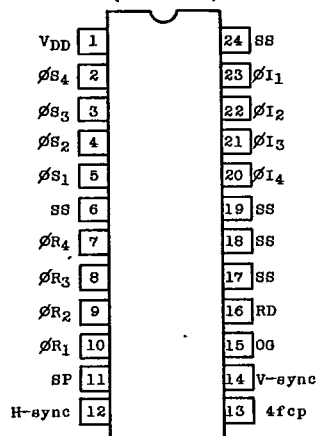


MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply Voltage	V _{DD}	-0.5 ~ 10	V
Input Voltage	V _{IN}	-0.5 ~ V _{DD} +0.5	V
Power Dissipation	P _D	600	mW
Operating Temperature	T _{opr}	-10 ~ 60	°C
Storage Temperature	T _{stg}	-55 ~ 150	°C
Lead Temp./Time	T _{sol}	260	°C
		10	sec

PIN ASSIGNMENT

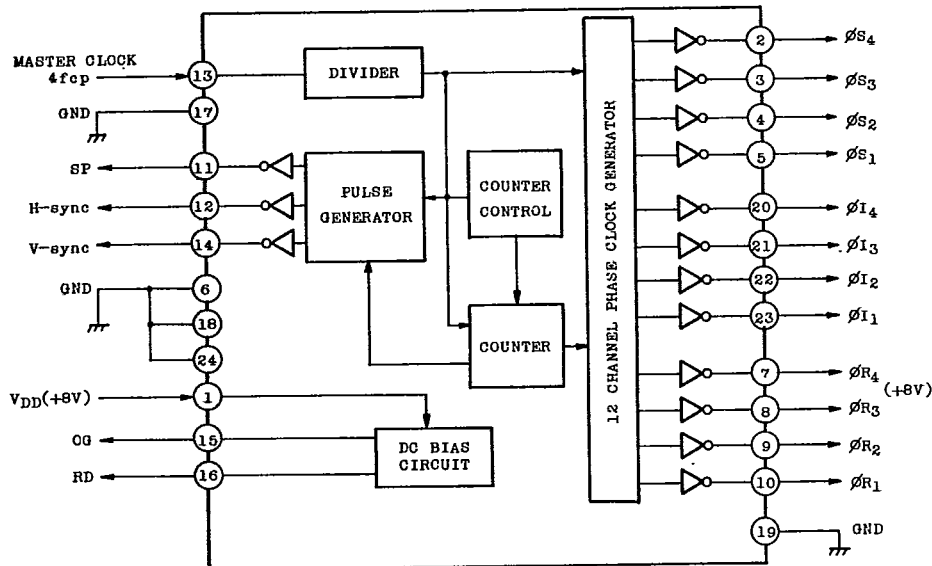
(TOP VIEW)



9097248 TOSHIBA {LOGIC/MEMORY}
67C 09608 D T-41-55

T3854

BLOCK DIAGRAM



PIN DESCRIPTION

ϕR_1		(Phase 1)	SP	Sampling Pulse
ϕR_2	Clock (Read Out Register)	(Phase 2)	H-sync	Horizontal Synchronize Pulse
ϕR_3		(Phase 3)	V-sync	Vertical Synchronize Pulse
ϕR_4		(Phase 4)	RD	Reset Drain
ϕI_1		Clock (Imaging Area)	(Phase 1)	OG
ϕI_2	(Phase 2)		4 fcp	Master Clock Pulse
ϕI_3	(Phase 3)		SS	Substrate (GND)
ϕI_4	(Phase 4)			
ϕS_1	Clock (Storage Area)	(Phase 1)		
ϕS_2		(Phase 2)		
ϕS_3		(Phase 3)		
ϕS_4		(Phase 4)		

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67C 09609 D T-41-55

T3854

ELECTRICAL CHARACTERISTICS (Ta=25°C)

CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Clock Frequency	4 fcp	-	V _{DD} =8.0V	0.1	-	6.4	MHz
Input Voltage	"H" Level	V _{IH}	V _{DD} =8.0V	6.7	7.0	-	V
	"L" Level	V _{IL}	V _{DD} =8.0V	-	0.8	1.3	
Input Current	"H" Level	I _{IH}	V _{DD} =V _{IN} =8.0V	12	30	40	mA
	"L" Level	I _{IL}	V _{IL} =GND, V _{DD} =8.0V	-12	-30	-40	
Output Current	"L" Level	I _{OL1}	(Note 1)	2.7	-	-	mA
	"L" Level	I _{OL2}	(Note 2)	1.0	-	-	
Output Voltage	"H" Level	V _{OH}	V _{DD} =8.0V, I _{OH} =-2μA	7.6	7.8	-	V
DC Bias Output Voltage		V _{RD}	V _{DD} =8.0V, I _R =-3.6μA	-	6.5	-	V
		V _{OG}	V _{DD} =8.0V, I _R =-2.5μA	-	2.5	-	
Supply Current	I _{DD}	-	V _{DD} =8.0V, 4fcp=100kHz	-	25	50	mA

Note 1 : V_{DD}=8.0V, V_{OL}=0.4V
Pin 2,3,4,5,7,8,9,10,20,21,22,23

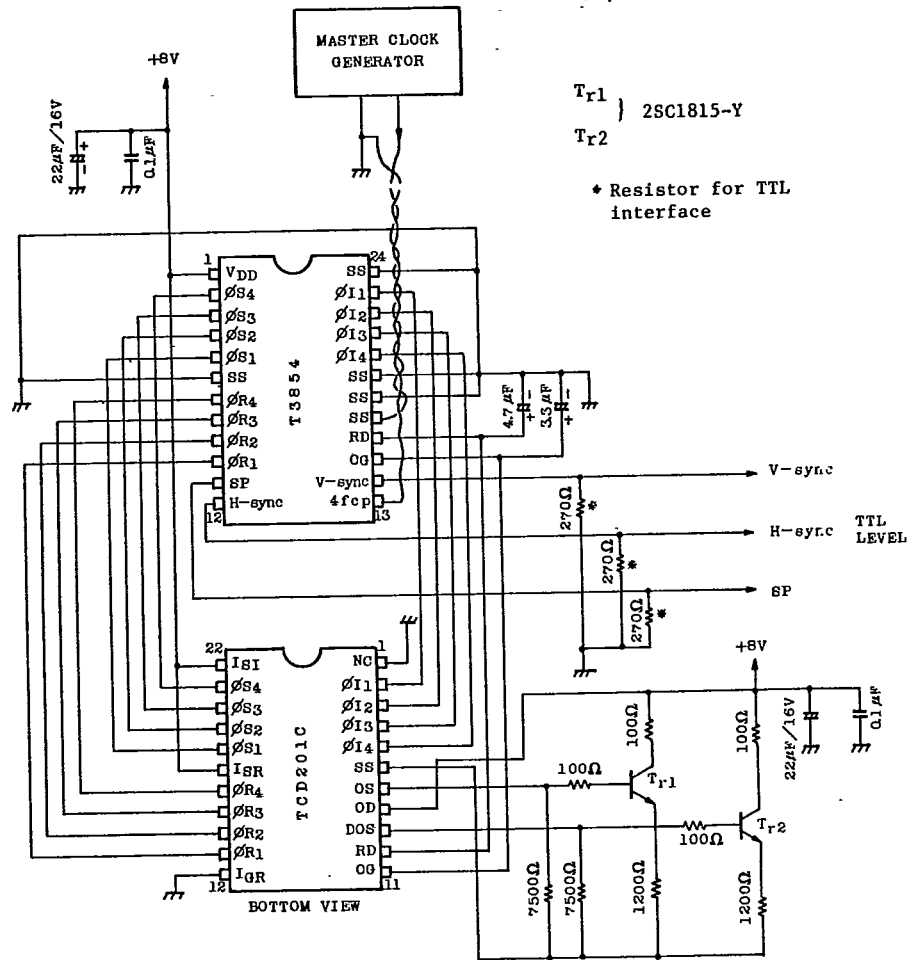
Note 2 : V_{DD}=8.0V, V_{OL}=0.4V
Pin 11,12,14

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67C 09611 D T-41-55

T3854

APPLICATION



9097248 TOSHIBA (LOGIC/MEMORY)

67C 09612

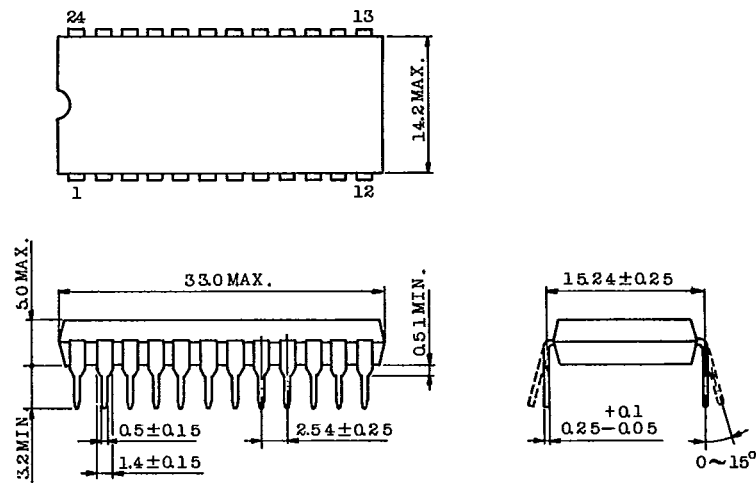
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T-41-55

T3854

PACKAGE OUTLINE (6D24A-P)

Unit in mm



Note) Lead pitch is 2.54 and tolerance is ± 0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.